Parallel Deterministic Solution of the Boltzmann Transport Equation for Semiconductors

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Clock frequencies and hence single-threaded processing power of modern processors have saturated because of power constraints. As a consequence, the overall processing power in modern processors mostly stems from parallelization and vectorization. However, parallel processors can only be used efficiently with suitable parallel algorithms. Unfortunately, the design and implementation of such parallel algorithms is often difficult and requires problem-specific knowledge for best performance. We present results of a successful parallelization of a semiconductor device simulator based on deterministic solutions of the Boltzmann transport equation.

Our results are obtained for the method of spherical harmonics expansions for solving the Boltzmann transport equation deterministically. The flux-conserving discretization scheme leads to large systems of sparsely coupled linear equations, which are solved with iterative solvers such as the generalized minimum residual method. As shown by Jungemann et al. ("Stable Discretization of the Boltzmann Equation based on Spherical Harmonics, Box Integration, and a Maximum Entropy Dissipation Principle", *J. Appl. Phys.*, **100**(2), 2006), good preconditioners are required for the spherical harmonics expansion method to ensure convergence of iterative solvers. Conventionally employed preconditioners from the family of incomplete LU factorizations are, however, purely sequential, hence using only a fraction of the computing power available in modern processors. We derived a domain-specific block-preconditioner and demonstrated up to ten-fold performance gains on a single workstation in earlier work (On the Feasibility of Spherical Harmonics Expansions of the Boltzmann Transport Equation for Three-Dimensional Device Geometries", *IEDM Techn. Digest*, 2011). In this work we refine these ideas based on a parallel variant of incomplete LU factorization preconditioners proposed by Chow and Patel ("Fine-Grained Parallel Incomplete LU Factorization", *SIAM J. Sci. Comp.*, **37**(2), 2015). Our results show that our proposed preconditioner is executed efficiently on current multi-core central processing units as well many-core architectures such as graphics processing units. Coupling the results of our earlier work with the results in this work, we sketch a domain-specific preconditioner suitable for compute clusters with hundreds of processors and thousands of cores.

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Electrothermal Simulation of Wide-Area Power Semiconductor Devices During Out-of-SOA Events

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The electro-thermal behaviour of power semiconductor devices is influenced not only by the temperature dependence of electrical quantities such as mobility and threshold voltages but also by the geometry of the device and by the mutual interaction of the many cell that are needed to give the device its capability of controlling very high currents. For this reason physical TCAD simulation of a limited number of cells rarely give quantitative information about the electro-thermal stresses. In this work we present the state-of-art of different simulation strategies apt to understand, from a 3D point of view and over the entire device area, the onset and evolution of critical phenomena such as current filamentation and hopping during short-circuit and avalanche operation of the device.

To this purpose we introduce Thermal Feedback Blocks. Thermal Feedback Blocks (TFBs) are a viable alternative to perform thermal and electrothermal (ET) simulations of electronics systems with very fast-switching inputs, for which the coupling of a finite-element method (FEM) thermal solver with a physics-based or a circuit simulator cannot be