

Temperature-dependent hysteresis in black phosphorus FETs

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Black phosphorus, also known as phosphorene in the few layer limit, is an almost unexplored “beyond graphene” material which is now considered a promising candidate for next-generation 2D FETs with good I_{on}/I_{off} ratios [1-4]. One issue that has not been explored in detail yet is the hysteresis in the I_d - V_g characteristics, which can severely limit the usability of these devices. Here we examine the hysteresis of back-gated black phosphorus FETs with SiO_2 gate insulator and Al_2O_3 encapsulation [4]. We measure the I_d - V_g characteristics of our devices using different sweep rates $S = V_{step}/t_{step}$ at different temperatures and monitor variations of the hysteresis width ΔV which is proportional to the charged trap density shift ΔN_T . As shown in Fig. 1, the I_d - V_g curves contain electron and hole conduction regions with the Dirac point in between. Each of these regions exhibits some hysteresis, which becomes more pronounced at higher temperatures and for lower sweep rates. Fig. 2(left) shows the dependence of ΔV vs. S extracted closely to V_{th} at four different temperatures. Clearly, slower traps are frozen out at -193°C and become dominant at 165°C . This means that charge trapping at the black phosphorus/ SiO_2 interface is thermally activated, similarly to Si technologies [5]. As shown in Fig. 2(right), at higher temperature the number of charged traps increases within the whole range of gate voltages.

Since the typical ΔN_T values in black phosphorus FETs are considerably larger than in their Si counterparts, we conclude that further efforts are needed to make this technology competitive.

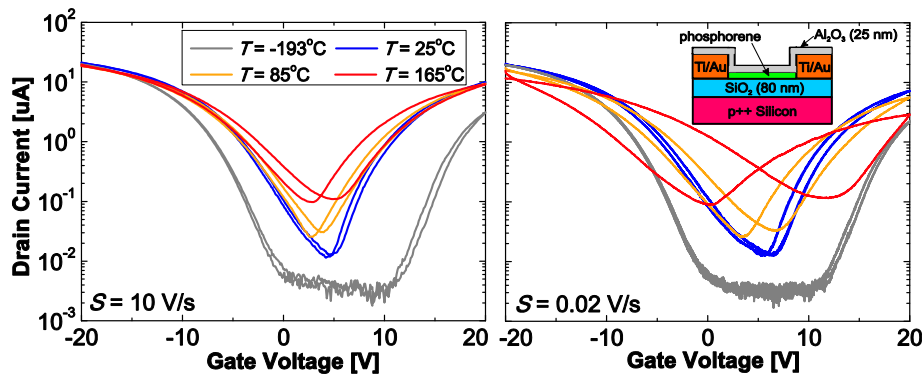


Fig. 1. The I_d - V_g characteristics of our black phosphorus FETs measured using $S = 10$ V/s (left) and $S = 0.02$ V/s (right) at different temperatures. The inset shows the device configuration.

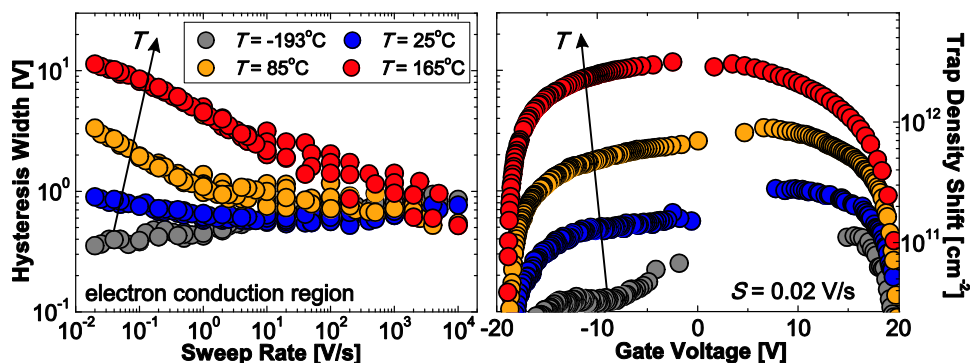


Fig. 2. Left: The hysteresis width vs. S extracted for $V_g \approx V_{th}$. Right: The hysteresis width and resulting $\Delta N_T = C_{\text{SiO}_2} \Delta V / q$ measured for different V_g using $S = 0.02$ V/s. The results obtained at different temperatures suggest strong thermal activation of charge trapping by slower traps.

References

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