Effects of the Deposition Process Variation on the Performance of Open TSVs

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***Abstract*—Three-dimensional integration with through-silicon vias is becoming essential for the future of the micro- and nano-electronics industry. The ability to incorporate multiple wafers and systems in a single design is revolutionizing device packaging. However, the complexity in the fabrication of through-silicon via structures and the reliability concerns must be addressed. In this work the effects of the deep reactive ion etching of silicon and the chemical vapor deposition of tungsten for the fabrication of a tungsten-lined open TSV are analyzed. When a 10% variation in the available tungsten flux during CVD is introduced, the device resistance is found to also vary by 10%. The TSV inductance was shown to vary between 7% and 10%, while the capacitance remained unchanged. In addition, the thermo-mechanical stress through the tungsten layer was simulated and it was found that changing the tungsten flux, and thereby the metal thickness, has no major influence on the stress build-up.**

***Keywords*-Through silicon via; Deep reactive ion etching; chemical vapor deposition; TCAD; Process simulation; Finite element modeling**

I. Introduction

An ongoing demand in the semiconductor industry has been increasing the functionality of end-user products using ever more complex interconnect structures; however, there are reliability concerns and performance limitations of interconnects in multiple integrated circuit (IC) designs. The advent of system-on-chip (SoC) in the mid 1990s addressed the increased delay of the off-chip interconnect with two-dimensional (2D) integration [1]. The integration of multiple components on a single monolithic substrate improved the speed and power consumption of the system. This pursuit in the industry has been overshadowed by the aspiration of increasing transistor counts and miniaturization known as Moore's law [2]. Only recently the pursuit for the integration of applications beyond memory and logic has been introduced in the International Technology Roadmap for Semiconductors (ITRS) with the terminology More-than-Moore [3]. More-than-Moore is meant to provide additional value to the complete system and not only in the miniaturization and extreme scaling of digital logic and memory.

One of the pillars of More-than-Moore is three-dimensional (3D) integration, a means of stacking silicon wafers and dies vertically using through-silicon vias (TSVs) so that the system behaves as a single device. This type of integration scheme exploits the vertical direction in order to improve the electrical performance of devices, reduce RC delay, lower power consumption, and increase packaging density [4]. Using 3D integration and TSVs the functionality of a single IC will continue to broaden.

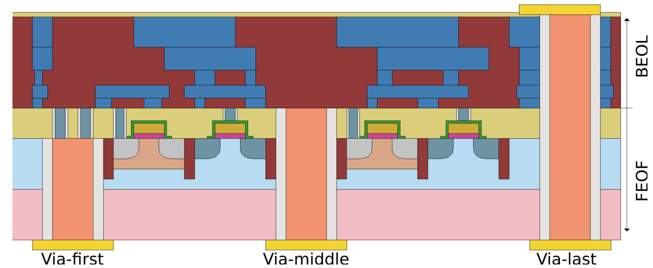

Figure 1. Illustration of the different TSV process technologies including via-first, via-middle, and via-last. The naming references whether the TSV is fabricated before the FEOL and BEOL steps, between the FEOL and BEOL steps, or after the FEOL and BEOL steps, respectively.

In order to harness the full potential of 3D integration, the manufacture of TSVs must be compatible with the CMOS process. Three potential techniques are being implemented today:

1) Via-first: In this process the basic silicon wafer is etched and the metal layer connecting the top and bottom of the wafer is deposited prior to the fabrication of the front end of line (FEOL) transistor devices.
2) Via-middle: For this process the TSV is fabricated after the FEOL transistors have been generated, but before the back end of line (BEOL) metal lines have been deposited.
3) Via-last: For this method the TSV is fabricated by etching the silicon from the back of the wafer after the FEOL transistors and BEOL metal layers have already been created. In many cases the BEOL metal interconnects serve as the etch stop layers in the silicon etch process.

In Fig. 1 the results of the three different techniques are shown. For via-last, the trench required in order to form the TSV is etched after FEOL and BEOL processing, meaning that the resulting TSV has the highest depth and aspect ratio.

A. Types of Through-Silicon Vias

The TSV is meant to connect the metal at the top of the wafer to a metal layer at the wafer bottom. This connection

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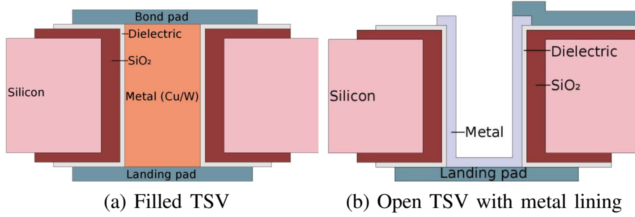


(a) Filled TSV (b) Open TSV with metal lining

Figure 2. Two TSV fabrication methods: (a) a filled-metal TSV where the metal is used to completely fill the trench connecting the top and bottom of the wafer, and (b) an open metal-lined TSV where only a layer of metal lines the walls of the TSV in order to connect the top and bottom wafer metal lines.

can be made by filling a trench with a metal, as is the case for metal-filled TSVs [5] or by providing a metal liner along the trench sidewalls, which is the case for open metal-lined TSVs [6], as shown in Fig. 2. Filled TSVs are usually thinner, with diameters down to below 2μm and aspect ratios up to 20 [7]. Open TSVs are wider, with diameters on the order of 50μm to 100μm and aspect ratios below 5 [8]. The two metals which are most commonly used in TSV connections are copper and tungsten.

The main advantage of the filled TSVs is the ability to fabricate very small structures. However, there are several concerns with regard to filled TSVs, mainly linked to stress build-up and device stability. Open TSVs are desired, when stress build-up due to material thermal expansion is a concern. The presence of a hole through the TSV gives the metal layer space to expand, avoiding the reliability concerns related to copper pumping [9]. Open TSVs are intended for applications where thermal budget is a concern and there is no need for fast digital switching. One such example for TSVs intended for use in high voltage applications with a 100μm diameter and 250μm depth is presented in [10]. A 200nm thick tungsten layer is deposited along the TSVs' sidewalls as the main conducting metal.

B. Gas Concentration during Deposition

The study presented by Roger et al. in [10] concerns itself with extracting electrical parameters from the TSV, while the scalloped sidewalls are ignored. The simulated structure is extracted from the TEM image of a manufactured TSV, making the inclusion of scallops along the sidewalls very complex. Since then, several studies attempted to describe the effects of a variety of processing steps on the TSV performance including the deep reactive ion etching (DRIE) of the silicon wafer [11] and the plasma enhanced chemical vapor deposition (PECVD) of the isolation oxide [12]. However, no studies until now dealt with the effects of the metal layer deposition on a scalloped open TSV structure. In this work the effects of tungsten lining deposition on an open TSV are analyzed through simulations. A variation of 10% in the relevant gas fluxes is assumed, as suggested in other chemical vapor deposition (CVD) equipment analysis [10], [12], [13], [14], while the effects of this variation on the electrical parameters and stress generation in the TSV are simulated.

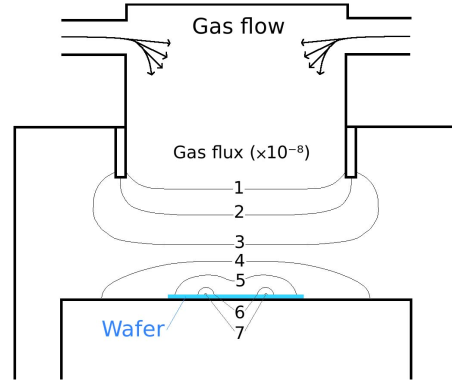


Figure 3. Illustration of a typical CVD chamber geometry, where gas is inserted into the chamber, influencing the available flux of the depositing species along the wafer surface [16].

In Fig. 3 a sample CVD chamber simulation geometry is given. The gas required for the chemical reaction is pushed into the chamber through valves at a desired concentration. However, this concentration varies depending on the equipment. The gas flows through the chamber, resulting in a flux distribution of several atoms and ions along the wafer surface. Through the variation in the input gas concentration, the wafer surface flux also varies. In this study an assumption is made that the relationship between the input gas concentration and gas flux is linear. This was found to be the case for plasma chambers studied in [11] and in [15]. It was similarly found that a linear relationship between the depositant flux and the deposition or etch rates also exists.

II. TSV Fabrication

The fabrication of open metal-lined TSVs is complex and requires several carefully executed steps. The TSV is fabricated as via-last with the CMOS sequence already performed to generate the FEOL devices. The BEOL metal lines are also deposited prior to the wafer etch in order to generate the TSV and the BEOL metal serves as the etch stop layer [6]. The wafer is subsequently thinned down to achieve the required thickness and bonded. The main steps which describe the fabrication process are: (1) the opening of the inter-metal dielectric; (2) the etching of the CMOS wafer using a DRIE process with an etch-stop metal layer; (3) the oxide isolation deposition described further in the sections to follow; (4) the deposition of the metal liner; and (5) the deposition of the oxide and nitride passivation layers [6]. In this study a TSV with a diameter of 80μm and a depth of 250μm is examined. An isolation oxide with 500nm thickness is deposited thereafter, followed by a thin

tungsten film with thicknesses ranging between 50nm and 100nm.

A. Etching Through the Silicon Wafer

After opening the inter-metal dielectrics on the top side of the wafer and the deposition of a metal etch-stop at the bottom side, the DRIE etching, also known as the Bosch process [17] is initiated. This process consists of a sequence of polymer deposition and etching cycles. The polymer is deposited using a plasma deposition in a C_4F_8 environment; a subsequent etching step in an ion-enhanced SF_6/O_2 plasma ensures that the bottom of the deposited polymer is etched away, while the presence of O_2 in the chamber ensures that the sidewalls are protected and that lateral etching is minimal. This step is a simultaneous chemical and physical process: The physical etching removes the polymer at the bottom, while the chemical component removes the silicon at the exposed trench bottom. After hundreds of deposition/etch cycles are executed, the trench remains with a sidewall roughness in the form of scallops which result from the cyclical nature of the process.

B. Oxide Isolation Deposition

After the etch process is complete, an oxide layer is deposited to ensure proper isolation between the silicon and the subsequent metal liner which will connect the top and bottom of the wafer. For a via-last process, the oxide must not be deposited using high-temperature CVD techniques. The maximum allowed temperature is in the order of 400°C, which is achieved using three deposition steps:

1) PECVD, performed at 350°C, is used to initiate oxide deposition;
2) sub-atmospheric chemical vapor deposition (SACVD) is used as a second spacer oxide deposition step; and
3) PECVD is used once again in order to get the optimal spacer layer thickness along the full TSV sidewall [6], [12].

Finally, the isolation oxide layer is a SACVD layer sandwiched by two PECVD layers [6]. The effect of the oxide deposition steps on the performance of the TSV is given in more detail by Baer et al. in [12], where statistical Monte Carlo simulations are performed on a similar TSV structure and the effects of the across-wafer variation of the oxide neutral and ion fluxes on the device performance are analyzed.

C. Metal Liner Deposition

After the deposition of the isolation oxide, a layer of Ti/TiN is deposited as liner, followed by a CVD of tungsten. The metalization is deposited using a CVD process over the entire wafer, followed by a selective removal of the metal everywhere except from the TSV area [6].

D. Passivation Deposition

Thin layers of silicon oxide and silicon nitride are deposited on top of the tungsten metal layer. These layers are essential to protect the wafers against moisture, but ensuring good coverage is challenging [6]. The oxide layer is deposited using a technique similar to the isolation oxide [18]. The full fabrication sequence is quite complex and several aspects of the fabrication have been analyzed in previous publications [11], [12], [18], [19].

III. Deep Reactive Ion Etching of Silicon

The two main methods to etch the silicon layer for TSV implementation are DRIE and plasma etching. Each process has its own pecularities and reliability concerns. Problems specific to the Bosch process are a rough, scalloped TSV sidewall, notch formation at the TSV bottom, and potential step coverage issues related to the deposition of thin layers on a scalloped sidewall [20]. Plasma etching of silicon results in angled sidewalls and an added wall curvature due to the via taper edge, but the rough scallops are avoided. When dealing with open TSVs, which usually have a larger diameter and depth than filled TSVs, a Bosch process is preferred. In order to simulate the etching and deposition steps, an in-house level set simulator is employed. The silicon etching step is performed using several deposition/etch cycles, known as the Bosch process. An oxide deposition step is then performed on the etched trench using an isotropic deposition compact model in order to deposit a 500nm thick SiO_2 layer. Finally, the tungsten layer is deposited using a CVD model, described further in the next section.

Bosch etching of deep vertical trenches in silicon proceeds using 3-step cycles, as suggested in [11]:

1) Deposition in C_4F_8 plasma: In this step a polymer layer is deposited which acts as a mask to the subsequent chemical etching steps. This is meant to provide protection to the sidewalls during the etching steps in order to create a highly vertical trench without lateral etching and with control over the sidewall tapering.
2) Etching in SF_6/O_2 plasma: The plasma etching in SF_6/O_2 gas mixtures is used when anisotropy is desired. The chemical reaction between Si and F results in significant lateral etching; however, the introduction of oxygen causes a thin silicon oxide passivation during the etch, inhibiting lateral etching [21]. This leads to an overall anisotropic, vertical etching step. During this step, the polymer deposited in the first step is removed at the trench bottom, while the sidewalls are protected.
3) Etching in SF_6 plasma: Plasma etching in a SF_6 gas relies on the chemical reaction between Si and F, which causes an isotropic reaction. During this step, the lateral etching is inhibited by the polymer deposited during the first step, while the etching proceeds

at the bottom of the trench, in near-equal part laterally and vertically [22].

In the section which follows, the models used to simulate the three steps are given.

A. Physical Modeling

The physical models used to generate the TSV trench structure are based on the level set and ray tracing techniques [23] in combination with several models for polymer deposition and silicon etching [24], [25], [26]. The model for the polymer deposition incorporates the presence of two fluxes at the wafer surface: neutral CF_x and ions. The CF_x flux is responsible for the isotropic chemical deposition, while the ions have little influence on the sidewall and deposit mainly along the flat horizontal surfaces. The influence of both fluxes on the growth rate of the deposited material are calculated and applied to the level set description of the wafer and trench surfaces.

For the etching cycle a more complex model is required for several reasons:

1) The etching in an oxygen environment cannot be represented with a simple neutral/ion flux, because the oxygen atoms effectively act as a coating agent reducing the amount of lateral etching which can proceed during each step, thereby promoting a more vertical etch.
2) Each material involved (oxide mask, polymer, silicon) has a different etch rate in the presence of the SF_6 and SF_6/O_2 plasmas.
3) During every simulated time step the fluoride and oxygen surface coverages must be calculated and only then can the etch rates along the surface be found.

A single physical model is used for etching in SF_6 and SF_6/O_2 plasmas: mainly, the SF_6/O_2 model [26]. Without oxygen, the oxygen flux is simply set to zero, reducing the model to SF_6 etching only [25]. The etch rate is expressed as a sum of three contributions: chemical etching due to the Si and F reaction, physical sputtering due to ions sputtering chunks of the silicon surface, and ion-enhanced etching

$$r = \frac{1}{\rho_{Si}} \left(\frac{k\sigma_{Si}\theta_F}{4} + Y_p\Gamma_i + Y_{si}\Gamma_i\theta_F \right), \quad (1)$$

where ρ_{Si} is the Si density, $k\sigma_{Si}$ is the chemical etch reaction rate constant, Γ_i is the total ion flux, and Y_p and Y_{Si} are the physical sputtering and ion-enhanced etching yields, respectively. θ_F is the steady-state fluoride surface coverage which depends on all involved fluxes: fluoride (Γ_F), ion (Γ_i), and oxide (Γ_O)

$$\theta_F = \frac{1}{1 + \left(\frac{k\sigma_{Si} + 2Y_{Si}\Gamma_i}{\gamma_F\Gamma_F} \right) \cdot \left(1 + \frac{\gamma_O\Gamma_O}{\beta\sigma_{Si} + Y_O\Gamma_i} \right)}, \quad (2)$$

Table I
TYPICAL POLYMER DEPOSITION AND SUBSEQUENT ETCHING PARAMETERS DURING A SINGLE DEEP REACTIVE ION ETCHING CYCLE.

Cycle step	Rate	Etch ratio		Time
Polymer deposition	16 nm/s	-	-	0.8 s
Silicon etch (isotropic)	60 nm/s	Si:mask	100:1	1.3 s
		Si:polymer	80:1	
Silicon etch (directional)	370 nm/s	Si:mask	10:1	
		Si:polymer	10:1	
Silicon etch (isotropic)	400 nm/s	Si:mask	100:1	1.5 s
		Si:polymer	80:1	
Silicon etch (directional)	50 nm/s	Si:mask	10:1	
		Si:polymer	10:1	

where γ_O and γ_F are the oxygen and fluoride sticking coefficients, respectively and $\beta\sigma_S i$ is the O recombination rate constant [26]. Using (1) and (2) in a SF_6 only plasma the rate is found by setting $\Gamma_O = 0$.

Precise simulations of TSV etching using the physical models described here require account for millions of particles at each time step. Unfortunately, this requires an unfeasible amount of processing power, memory, and time in order to generate a single structure.

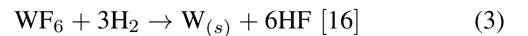
B. TSV Trench Generation

Instead of generating all structures using physical models, previous studies [11], [15], where the physical models were used to generate the respective deposition and etch rates, are used in the following. The structure is generated using simplified empirical rate calculations. Sample rates used to generate a scalloped TSV trench, such as the one used in this study, are given in Table I. The resulting structure has scallops with heights and widths of about 210nm and 1000nm, respectively.

In order to understand the influence of the scallops on the TSV performance, an additional structure with the same aspect ratio and flat sidewalls has been generated for the subsequent tungsten CVD and device simulations. The 2D profiles of both structures are shown in Fig. 4, where the red vertical lines represent the axis of rotational symmetry. Only the 2D profiles are used in this study, because 3D simulations are not feasible, when the geometry consists of materials with wide ranging thicknesses, some in the nanometer and others in the micrometer range.

IV. Chemical Vapor Deposition of Tungsten

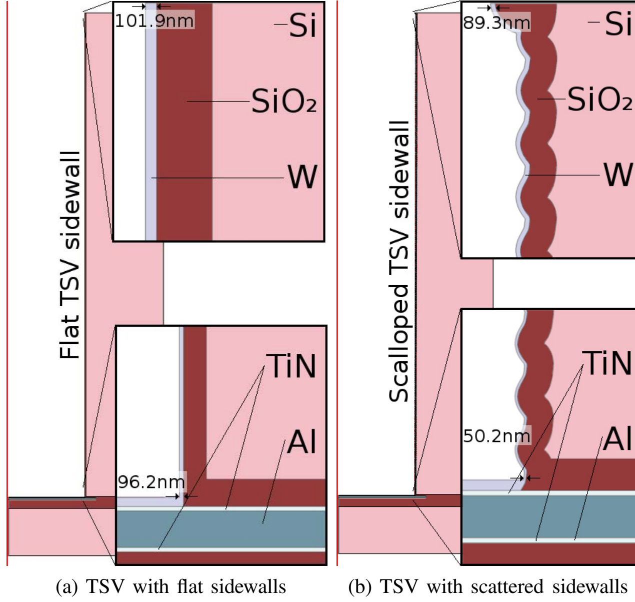
During tungsten CVD tungsten hexafluoride (WF_6) is used as a tungsten precursor and is injected into the chamber, while the reducing agent is either H_2 [16] or SiH_4 [27]. This causes one of the following chemical reactions to take place: namely



$$WF_6 + 3H_2 \rightarrow W_{(s)} + 6HF \ [16] \quad (3)$$

or

$$WF_6 + 2SiH_4 \rightarrow W_{(s)} + 2SiHF_3 + 3H_2 \ [27], \quad (4)$$



(a) TSV with flat sidewalls (b) TSV with scattered sidewalls

Figure 4. Profiles of the TSVs used in this study after the SiO_2 and tungsten layers have been deposited. The device simulations are performed using a 2D axis-symmetric model, because a 3D simulation is not feasible due to the large aspect ratio between the various material thicknesses. (a) The structure with the flat TSV and (b) the simulated structure using the etching parameters from Table I are shown.

respectively. The temperature and pressure ranges commonly used for the deposition process are 600-750K and 10^2-10^3Pa, respectively [16].

A semi-empirical equation which describes the deposition rate in nm/s is given by [28]

$$r = k_0 \cdot [P_{WF_6}]^{\rho} \cdot [P_{H_2}]^{0.5} \cdot e^{-E/k_B T}, \tag{5}$$

where k_0 is a pre-exponential factor, and $[P_{WF_6}]$ and $[P_{H_2}]$ are the partial pressures of WF_6 and H_2, respectively, E is the activation energy, k_B the Boltzmann constant, T the temperature, and ρ is assumed to be zero. The assumption that $\rho = 0$ is only valid for deposition on a flat sheet or in very shallow trenches with small aspect ratios. When deposition is required in higher aspect ratio trenches, the growth mechanism is determined, or limited, by the gas-phase diffusion of reactants to the surface.

However, when very high aspect ratio trenches are to be analyzed, the gas fluxes change at the trench bottom must also be taken into consideration [29], making the deposition rate reactant concentration limited. Therefore, the model for CVD must also be adjusted to include the variations expected with trench deposition.

A. Modeling Tungsten CVD

All the phenomena described in the above sections have been incorporated within a simple line-of-sight model for CVD, used to describe low pressure CVD and PVD processes as given in [30]. Instead of relying on a single

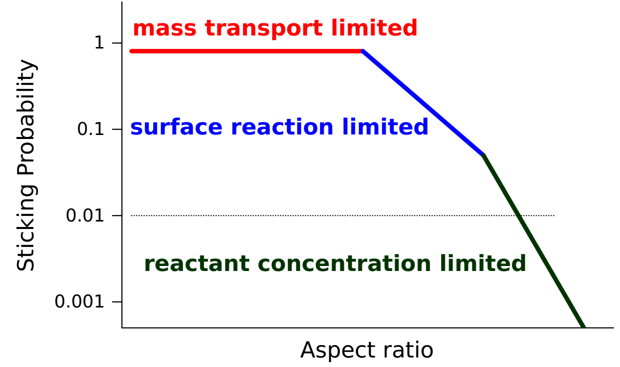


Figure 5. Sticking probability as a function of the aspect ratio. A sticking probability of 0.01 was found to best fit with published experiments.

deposition rate, the model considers the deposition using a stochastic simulation space where millions of particles are used to emulate the depositant flux. A single species is considered as a depositant and its deposition on the surface depends on physical and chemical factors. The physical factor is related to the visibility between the surface and the gas source, also known as shadowing. The chemical factor relates to the interaction of the species at the surface, represented as a sticking probability. A particle sticking on the surface means that deposition takes place.

As discussed previously, when depositing a material in trenches, there are several possible rate limiting interactions. These interactions are modeled using the sticking probability of the particles in the simulation space, as shown in Fig. 5. The sticking probability s at a location on the surface $(\vec{x})$ in the model can be modified depending on the rate limiting step, which in-turn depends on the trench depth, making it dependent on the local arriving particle flux at every location $F(\vec{x})$.

$$s(\vec{x}) \sim F(\vec{x})^{\eta-1}, \tag{6}$$

where η refers to the order of the reaction [31]. In the presented work a linear reaction kinetics is assumed with a sticking probability $s(\vec{x}) = 0.01$, which gives step coverages in agreement with published results [28], [30], [31].

B. TSV Structure Generation

Two sample TSV structures, generated using the described silicon DRIE and tungsten CVD models, are shown in Fig. 4. The differences between the flat and scalloped structures are evident. Additionally, the tungsten thickness distribution from the top to the bottom of the TSV trench is different between the flat and scalloped structures. The extreme reduction in the tungsten thickness at the bottom of the scalloped TSV from 89.3nm to 50.2nm can be attributed to the scalloped geometry, since the flat TSV experiences a very minor reduction – from 101.9nm at the top to 96.2nm at the bottom of the TSV. This result suggests that modifications

Table II
SUMMARY OF THE RESULTS AND VARIATIONS OBTAINED FOR THE TSV STRUCTURES WITH FLAT AND SCALLOPED SIDEWALLS. THE VARIATION SHOWN CORRESPONDS TO AN INDUCED 10% VARIATION IN THE TUNGSTEN DEPOSITION FLUX.

TSV Property	Flat sidewall		Scalloped sidewall	
	Median	Variation	Median	Variation
Resistance (mΩ)	534	10.32 %	965	10.80 %
Capacitance (pF)	4.76	0.00 %	4.79	0.00 %
Inductance (pH)	2.09	9.96 %	1.50	6.74 %
Ave. Stress (MPa)	288	0.14 %	253	1.48 %

to the CVD process are required when deposition along a scalloped structure. Lowering the pressure during fabrication may achieve the desired step coverage [27].

V. SIMULATION RESULTS

The structures generated using process simulations of DRIE and tungsten CVD, shown in Fig. 4 were meshed and imported into a finite element simulation environment. Several additional structures have been generated which represent a 10% variation in the tungsten depositant flux. A very fine mesh is required in order to properly simulate the structure due to the large differences in the thicknesses between the different materials and due to the size of the structure. For the scalloped TSVs meshes containing about 400,000 triangular elements are obtained, while for flat TSVs 100,000 suffices. The electrical performance and stress through the tungsten layer are examined by simulation, including the influence of the tungsten thickness variation and the presence of the DRIE scallops. The final summary of the variations in TSV performance are given in Table II.

The resistance through the generated structures is simulated and the results are shown in Fig. 6. As the tungsten flux is increased, the deposition rate increases, resulting in a bigger final tungsten thickness. This in-turn causes a decrease in the TSV resistance. The resistance through the scallop-sidewalled TSV is much higher than through the flat-sidewalled one due to the differences in the thickness, noted in Fig. 4. However, the variation for both flat and scalloped structures is approximately 10%, suggesting a linear relationship between the tungsten flux available during deposition and the final TSV resistance.

The capacitance and inductance of the TSV structures were simulated and the results are shown in Fig. 7 and Fig. 8, respectively. The capacitance does not vary due to the variation in the tungsten thickness, but the presence of scallops causes an increase in the capacitance. The lack of dependence on the tungsten thickness is expected, as it was previously found that the main factor in the capacitance is the deposition of the isolation oxide [32]. The capacitance increases in the presence of scallops due to the effective thinning of the oxide, which occurs between the scallop pinch-off points [19].

The inductance is shown to reduce with an increase in the tungsten flux and thickness. This is not unexpected since the induced magnetic energy increases with an increase in the cross-section of a conductor. Similarly, the inductance of a conductor is directly proportional to the magnetic energy. Therefore, an increased conductor diameter, or an increased tungsten thickness in the case of an open TSV, results in an increased inductance.

A stress can build up in the metal lining of the TSV due to the cooling of the structure after tungsten deposition. A simulation is performed, where the structure is cooled from the 400°C deposition temperature down to room temperature. The average stresses through the tungsten metal layer as a result of this cool-down are given in Fig. 9. Although some variation can be seen for the scalloped structure, overall, the variation is much smaller than the induced tungsten thickness variation. It is also worthy noting that the stress in the scalloped structure is smaller when compared to the flat TSV. This is due to the scallops allowing for local displacement around each scallop, relieving the structure of stress in the process [19].

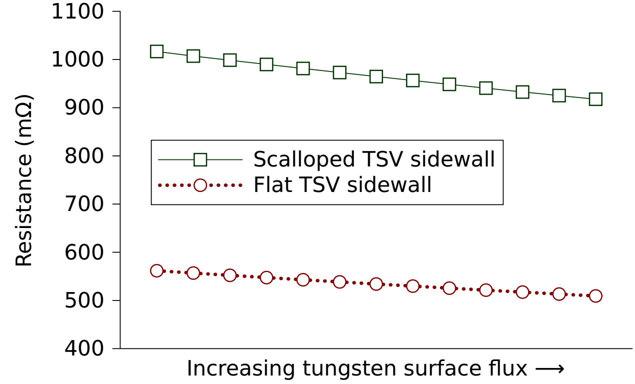


Figure 6. Variation in the TSV resistance (mΩ) due to increasing the tungsten flux along the wafer surface during CVD.

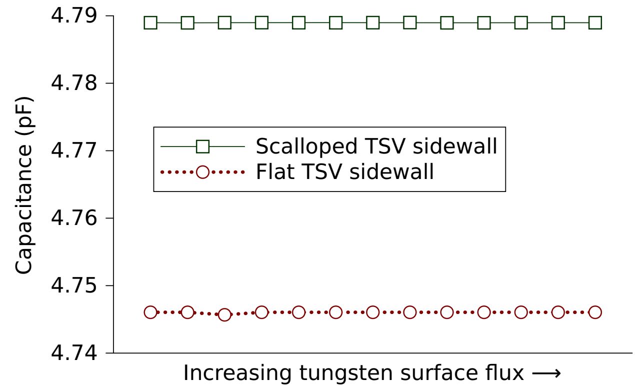


Figure 7. Variation in the TSV capacitance (pF) due to increasing the tungsten flux along the wafer surface during CVD.

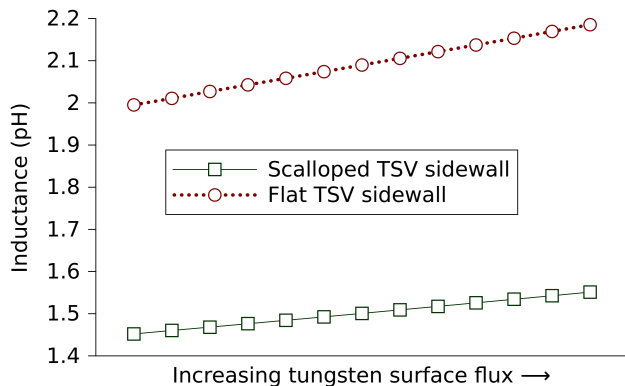


Figure 8. Variation in the TSV inductance (pH) due to increasing the tungsten flux along the wafer surface during CVD.

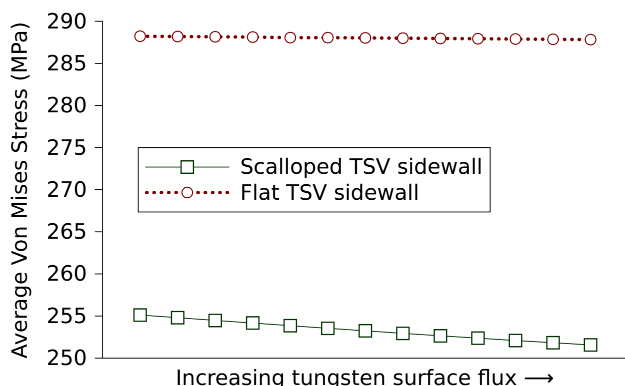


Figure 9. Variation in the average stress in the metal layer of the TSV due to increasing the tungsten flux along the wafer surface during CVD. The stress is caused by thermal expansion when cooling the structure from the 400°C deposition temperature down to room temperature.

VI. Conclusion

In this work several aspects of an open tungsten-lined TSV were studied using process and device simulation techniques. The main process techniques studied were silicon DRIE and tungsten CVD. Deep reactive ion etching of the silicon wafer is required to generate the TSV trench, while CVD is used to deposit the metal which connects the top and bottom metalizations of the wafer. A recipe for the metal deposition and silicon trench etching required to generate a TSV trench is given; however, the etching technique produces scalloped sidewalls, resulting in a different electrical performance and a different stress response when compared to a flat-sidewalled alternative. The scalloped TSV shows a higher resistance and capacitance, while the inductance decreases. The thermo-mechanical stress through the tungsten metal is also shown to decrease when scallops were present.

During the CVD process there are several factors which lead to variation in the amount of depositant available at the wafer surface. This, which can be in the range of 10% or more. In this work the effect of this variation on the electrical performance and stress build-up in the TSV metal layer is studied. It is found that a 10% variation in the tungsten thickness results in a 10% variation in the TSV resistance and a near-10% variation in its inductance. The capacitance and thermo-mechanical stress remain effectively unchanged. Therefore, when trying to understand the causes of variation in TSV structures, tungsten CVD may be omitted as a reason for any observed variation in the thermo-mechanical stress or capacitance.

References

[1] V. Pangracious, Z. Marrakchi, and H. Mehrez, "Three-dimensional integration: A more than moore technology," in *Three-Dimensional Design Methodologies for Tree-based FPGA Architecture*, V. Pangracious, Z. Marrakchi, and H. Mehrez, Eds. Springer, 2015, ch. 2, pp. 13–41.

[2] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp. 114-117," *Solid-State Circuits Society Newsletter*, vol. 11, no. 5, pp. 33–35, 2006.

[3] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "More-than-Moore white paper," IRC, Tech. Rep., 2010.

[4] R. Li, Y. Lamy, W. Besling, F. Roozeboom, and P. Sarro, "Continuous deep reactive ion etching of tapered via holes for three-dimensional integration," *Journal of Micromechanics and Microengineering*, vol. 18, no. 12, p. 125023, 2008.

[5] C. S. Selvanayagam, J. H. Lau, X. Zhang, S. Seah, K. Vaidyanathan, and T. Chai, "Nonlinear thermal stress/strain analyses of copper filled TSV (through silicon via) and their flip-chip microbumps," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 4, pp. 720–728, 2009.

[6] J. Kraft, F. Schrank, J. Teva, J. Siegert, G. Koppitsch, C. Cassidy, E. Wachmann, F. Altmann, S. Brand, C. Schmidt, and M. Petzold, "3D sensor application with open through silicon via technology," in *IEEE Electronic Components and Technology Conference (ECTC)*, 2011, pp. 560–566.

[7] V. Solberg, "TSV process variations for 2.5 and 3D semiconductor packaging," *Proc. International Wafer-Level Packaging Conference (IWLPC)*, 2012.

[8] "International Technology Roadmap for Semiconductors," IRC, Tech. Rep., 2013.

[9] J. V. Olmen, C. Huyghebaert, J. Coenen, J. V. Aelst, E. Sleeckx, A. V. Ammel, S. Armini, G. Katti, J. Vaes, W. Dehaene, E. Beyne, and Y. Travaly, "Integration challenges of copper through silicon via (TSV) metallization for 3D-stacked IC integration," *Microelectronic Engineering*, vol. 88, no. 5, pp. 745–748, 2011.

[10] F. Roger, J. Kraft, K. Molnar, and R. Minixhofer, "TCAD electrical parameters extraction on through silicon via (TSV) structures in a 0.35μm analog mixed-signal CMOS," in *Proc. International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2012, pp. 380–383.

[11] F. Roger, A. Singulani, S. Carniello, L. Filipovic, and S. Selberherr, "Global statistical methodology for the analysis of equipment parameter effects on TSV formation," in *Proc. 6th International Workshop on Variability (VARI)*, 2015, pp. 39–44.

[12] E. Baer, P. Evanschitzky, J. Lorenz, F. Roger, R. Minixhofer, L. Filipovic, R. de Orio, and S. Selberherr, "Coupled simulation to determine the impact of across wafer variations in oxide PECVD on electrical and reliability parameters of through-silicon vias," *Microelectronic Engineering*, vol. 137, pp. 141–145, 2015.

[13] R. Arora and R. Pollard, "A mathematical model for chemical vapor deposition processes influenced by surface reaction kinetics: Application to low-pressure deposition of tungsten," *Journal of the Electrochemical Society*, vol. 138, no. 5, pp. 1523–1537, 1991.

[14] C. Kleijn, "On the modelling of transport phenomena in chemical vapour deposition and its use in reactor design and process optimization," *Thin Solid Films*, vol. 206, no. 1, pp. 47–53, 1991.

[15] L. Filipovic, A. Singulani, F. Roger, S. Carniello, and S. Selberherr, "Impact of across-wafer variation on the electrical performance of TSVs. Submitted to: IEEE International Interconnect Technology Conference (IITC)," 2016.

[16] K. Kuijlaars, C. Kleijn, and H. van Den Akker, "A detailed model for low-pressure CVD of tungsten," *Thin Solid Films*, vol. 270, no. 1, pp. 456–461, 1995.

[17] F. Lärmer and A. Schilp, "Verfahren zum anisotropen Ätzen von Silicium," *Deutsches Patent DE4241045 C1*, 1994.

[18] J. Kraft, A. Hueber, S. Carniello, F. Schrank, and E. Wachmann, "Passivation integrity investigations for through wafer interconnects," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, 2008, pp. 506–509.

[19] L. Filipovic and S. Selberherr, "The effects of etching and deposition on the performance and stress evolution of open through silicon vias," *Microelectronics Reliability*, vol. 54, no. 9, pp. 1953–1958, 2014.

[20] N. Ranganathan, L. Youhe, G.-Q. Lo, K. Prasad, and K. L. Pey, "Influence of Bosch etch process on electrical isolation of TSV structures," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, no. 10, pp. 1497–1507, 2011.

[21] G. Craciun, M. Blauw, E. Van der Drift, P. Sarro, and P. French, "Temperature influence on etching deep holes with SF_6/O_2 cryogenic plasma," *Journal of Micromechanics and Microengineering*, vol. 12, no. 4, p. 390, 2002.

[22] M. Reiche, U. Gösele, and M. Wiegand, "Modification of Si(100)-surfaces by SF_6 plasma etching – application to wafer direct bonding," *Crystal Research and Technology*, vol. 35, no. 6-7, pp. 807–821, 2000.

[23] O. Ertl and S. Selberherr, "Three-dimensional level set based Bosch process simulations using ray tracing for flux calculation," *Microelectronic Engineering*, vol. 87, no. 1, pp. 20–29, 2010.

[24] G. Kokkoris, A. Tserepi, A. Boudouvis, and E. Gogolides, "Simulation of SiO_2 and Si feature etching for microelectronics and microelectromechanical systems fabrication: A combined simulator coupling modules of surface etching, local flux calculation, and profile evolution," *Journal of Vacuum Science & Technology A*, vol. 22, no. 4, pp. 1896–1902, 2004.

[25] R. J. Belen, S. Gomez, M. Kiehlbauch, D. Cooperberg, and E. S. Aydil, "Feature-scale model of Si etching in SF_6 plasma and comparison with experiments," *Journal of Vacuum Science & Technology A*, vol. 23, no. 1, 2005.

[26] R. J. Belen, S. Gomez, D. Cooperberg, M. Kiehlbauch, and E. S. Aydil, "Feature-scale model of Si etching in SF_6/O_2 plasma and comparison with experiments," *Journal of Vacuum Science & Technology A*, vol. 23, no. 5, pp. 1430–1439, 2005.

[27] J. Ammerlaan, P. Van der Put, and J. Schoonman, "Kinetics of tungsten low-pressure chemical-vapor deposition using WF_6 and SiH_4 studied by in situ growth-rate measurements," *Journal of Applied Physics*, vol. 73, no. 9, pp. 4631–4636, 1993.

[28] C. McConica and K. Krishnamani, "The kinetics of LPCVD tungsten deposition in a single wafer reactor," *Journal of the Electrochemical Society*, vol. 133, no. 12, pp. 2542–2548, 1986.

[29] S. Holzer, "Optimization for enhanced thermal technology CAD purposes," Dissertation, TU Wien, 2007. [Online]. Available: http://www.iue.tuwien.ac.at/phd/holzer/

[30] T. Cale and G. Raupp, "A unified line-of-sight model of deposition in rectangular trenches," *Journal of Vacuum Science & Technology B*, vol. 8, no. 6, pp. 1242–1248, 1990.

[31] O. Ertl, "Numerical methods for topography simulation," Dissertation, TU Wien, 2007. [Online]. Available: http://www.iue.tuwien.ac.at/phd/ertl/

[32] L. Filipovic, R. de Orio, S. Selberherr, A. Singulani, F. Roger, and R. Minixhofer, "Effects of sidewall scallops on open tungsten TSVs," in *Proc. IEEE International Reliability Physics Symposium (IRPS)*, 2014, pp. 3E3.1–3E3.6.