11:10   Gregory Di Pendina, CEA (Gregory.DiPendina@cea.fr)

with E. Zianbetov, J. Lopes, L. Torres and E. Beigné

MRAM-Based Non-Volatile FD-SOI Technology, from Ultra-Low Power to Space Applications using Asynchronous Design

Magnetic Random Access Memory (MRAM), using Magnetic Tunnel Junction (MTJ) as the basis element, is nowadays well known in the emerging non-volatile memory (NMV) community. Lots of research efforts are done in both academic and industrial worlds. Its specific features such as fast writing and reading capabilities compared to other NVM, its low power consumption and advanced CMOS process compatibility, its scalability down to 20-40 nm, its high endurance and its intrinsic immunity to radiations attracts lots of research groups worldwide. In the same way, Fully Depleted Silicon On Insulator (FD-SOI) fabrication process is well known for potentially being a breakthrough in terms of Application Specific Integrated Circuit (ASIC) power consumption on very advanced process nodes, ranging from 28nm to 10nm. Such a process is latch-up free, offers the possibility to boost the speed performance or drastically reduce the leakage power using body biasing, and is more robust against radiation effects than a standard bulk CMOS process. Finally, in opposition to standard synchronous ASICs, clock-less or asynchronous ASICs are well known for being much more efficient in terms of power consumption since there is no clock that consumes the majority of the dynamic power, even when the circuit is in a standby mode. They are also Quasi Delay Insensitive (QDI) meaning asynchronous ASICs are extremely robust against process variations. As a consequence, this paper presents our work that consists in combining these three microelectronics features to address: i) Ultra-Low power ASIC design for Internet of Things (IoT) applications; ii) Radiation hardened ASIC for space applications. In the case of i) we demonstrated that our circuit can compute at 160mV in CMOS mode and 650 mV in non-volatile mode giving a gain of 14% to 30% of energy using Forward Body Biasing (FBB) when saving/restoring NVM and 40% using Reverse Body Biasing (RBB). In the case of ii) we have been able to save about 30% of ASIC area on a circuit capable of detecting and correcting radiation induced errors with an extreme safe procedure thanks to MTJ integration into the CMOS logic. Both ASICs are presently under design finalization and will be fabricated on a hybrid CMOS/Magnetic silicon demonstrator on Q3 2016.

11:30   Thomas Windbacher, Technische Universität Wien (windbacher@iue.tuwien.ac.at)

with A. Makarov, V. Sverdlov and S. Selberherr

Novel Magnetic Devices for Memory and Non-Volatile Computing Applications

The introduction of non-volatile memory elements in the proximity of the CMOS devices helps to reduce the overall power dissipation and the interconnection delay significantly. In addition, logic gates can be built by combining two non-volatile memory cells or by specially designing non-volatile logic devices on which a part of the computation can be performed. Several examples of such logic-in-memory concepts at device, circuit, and logic design level will be presented. It will also be demonstrated how magnetic devices like magnetic tunnel junctions, magnetic non-volatile flip flops, and spin transfer torque majority gates can be exploited for building functionally complete non-volatile computing environments.