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Editorial

Special Issue of Solid-State Electronics, dedicated to EUROSOI-ULIS 2016

The current special issue of Solid-State Electronics includes 29 extended papers presented at the 2016 Second Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS 2016) held in Wien, Austria, on January 25–27, 2016. The papers entering to the special issue have been selected by the EUROSOI-ULIS 2016 Technical Program Committee based on the excellence of abstracts submitted and presentations delivered at the conference. In order to comply with the high standards of Solid-State Electronics the manuscripts went through the standard reviewing procedure.

The papers cover the vast variety of topics including fabrication, characterization and modeling of the cutting-edge fully depleted SOI, FinFET and nanowire-based devices, tunnel FETs, and novel emerging devices for memory and logic applications.

The invited paper by H. Stork and G. Hossey from ON Semiconductor introduces an exciting field of commercial SOI technology and provides an extensive review of its use for power management in automotive and industrial applications.

The problem of an accurate extraction of the effective oxide thickness and the work function in extremely scaled 14 nm fully depleted SOI devices is addressed in the paper by B. Mohamad et al.

Simulation study of silicon ultra-scaled gate all around nanowire FETs including the line-edge roughness by 3D Finite Element Monte Carlo Simulations is performed by M. Elmessary et al.

Another aspect of variability due to electron scattering on randomly positioned impurities and the problem of self-averaging of impurity-limited resistance in quasi-one dimensional nanowires is addressed in the paper by N. Sano.

Drain current variability in 28 nm n-MOSFETs in both linear and saturation regimes is studied in details by T. Karatsori et al.

Continuing the line of extremely scaled devices, the computational benchmarking of III–V semiconductors tunnel FETs against the 10 nm CMOS FinFET technology is performed by S. Strangio et al. at an example of basic arithmetic circuits.

An extensive comparison of the analog performance of fabricated line tunnel FETs with respect to other tunnel FET- and MOSFET-based architectures is reported in the paper by P. Agopian et al.

Confinement orientation effects on source to drain tunneling are addressed by C. Medina-Bailon et al.

Process modules for GeSn nanoelectronics with high Sn-concentration reported by C. Schulte-Braucks et al. provide a base for further optimization of GeSn FETs and novel tunnel FET devices.

An experimental evaluation of the analog performance of n- and p-type SOI nanowire FETs in a broad temperature range from room temperature down to 100 K is performed by B. Paz et al.

The influence of temperature on drain-induced barrier lowering in ultra-thin box and body fully depleted SOI MOSFETs is analyzed by A. Pereira et al. based on extensive experimental data, numerical simulations, and analytical modeling.

Continuing the line of exploiting materials with improved transport characteristics for the next generation transistors, the influence of layout effects including mechanical stress in 14 nm UTBB FDSOI SiGe channel p-MOSFETs is investigated and characterized both experimentally and by modeling in the paper by R. Berthelon et al.

Fabrication process and conduction mechanisms in back-gated InGaAs-on-insulator lateral $N^{+}NN^{+}$ junctionless MOSFETs are reported by H.J. Park et al.

DC and first RF characterization of InGaAs replacement metal gate n-FETs on SiGe-on-insulator FinFETs fabricated by 3D monolithic integration is presented by V. Deshpande et al.

A new MOSFET threshold voltage characterization method suggested by D. Tomaszewski et al. allows elimination of the channel current effects by using junction capacitance measurements.

D. Boudier et al. describe how low frequency noise measurements can provide an essential information on the quality of the gate oxide and the silicon film of tri-gate SOI FinFETs and thus can be used as a non-destructive characterization tool at sub-10 nm technology nodes.

A systematic method for electrical characterization of random telegraph noise in MOSFETs is presented by C. Marquez et al. aiming to facilitate massive on-wafer characterization of noise MOSFET characteristics.

In the work by B. Kazemi Esfeh et al. it is shown that a trap-rich layer in trap-rich high resistivity SOI wafers with thinner BOX does not alter RF characteristics of the MOSFET transistors while it allows for improved thermal properties thus making the technology viable for SoC applications.

The paper by C. Jungemann et al. continues along the line of frequency-dependent phenomena in MOSFETs and provides an efficient numerical simulation tool capturing plasma oscillation effects in silicon MOSFETs used for THz detection.

Efficient approaches for accurate high-performance TCAD simulations are reported by the CDL Laboratory for high-performance TCAD at TU Wien: V. Simonka et al. describe the anisotropic interpolation method of SiC oxidation growth rates for three-dimensional simulation, while P. Manstetten et al. present a computationally efficient framework to evaluate the neutral flux in high aspect ratio structures during three-dimensional plasma etching simulations.

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T. Baldauf et al. address by simulations the effect of mechanical stress on tunneling and the transfer characteristics in two independently gated Schottky junctions of Schottky barrier-based reconfigurable nanowire transistors.

Continuing the reconfigurable FETs topic, C. Navarro et al. highlight the main advantages, limitations, and ways to improve the performance by employing TCAD for careful optimization and benchmarking reconfigurable field effect transistors.

Concerning new applications and devices employing advanced FD-SOI technology, a novel scalable three-dimensional single-photon avalanche diode pixel with high fill factor is proposed and extensively studied by simulations in the work of M. Vignetti et al.

A novel electrostatic discharge protection based on reconfigurable ultra-thin film gated diode merged NMOS is proposed and fabricated with 28 nm UTBB FD-SOI high-k metal gate technology in the work by S. Athanasiou et al.

Another new sharp-switching band-modulation back-gated device fabricated in advanced FD-SOI technology is presented by H. El Dirani et al.

Finally, recent developments in promising devices and concepts beyond SOI MOSFETs for future non-volatile memory and logic applications are given in the paper by A. Grossi et al., where electrical characterization and modeling of one-transistor/one-resistor resistive random access memory arrays with amorphous and polycrystalline HfO_2 as an active medium is presented.

A substantial reduction of the switching current in spin-transfer torque due to inverse magnetostriction induced switching barrier lowering is predicted by Y. Takamura et al. A magnetic random access memory cell based on the magnetic tunnel junction surrounded by a piezoelectric gate operates at low voltages, which promises a large reduction of the write energy without degradation of the thermal stability.

We would like to express our gratitude and thank all the authors for accepting the invitation and preparing the excellent quality manuscripts within a tight time frame. We would also like to acknowledge all the reviewers for their time spent to provide highly professional comments to the authors, which indisputably helped boosting the overall paper quality to meet the highest publication standards adopted by Solid-State Electronics. Our special thank is dedicated to the Solid-State Electronics Editor Sorin Cristoloveanu for his constant encouragements, support, and help.

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