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# Threshold voltage instabilities of present SiC-power MOSFETs under positive bias temperature stress

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**Abstract.** We study the threshold voltage ($V_{th}$) instability of commercially available silicon carbide (SiC) power MOSFETs or prototypes from four different manufacturers under positive bias temperature stress (PBTS). A positive bias near $V_{th}$ causes a threshold voltage shift of 0.7 mV per decade in time per nanometer oxide thickness in the temperature range between -50°C and 150°C. Recovery at +5 V after a 100 s +25 V gate-pulse causes a recovery between -1.5 mV/dec/nm and -1.0 mV/dec/nm at room temperature and decreases with temperature. All devices show similar stress, recovery and temperature dependent behavior indicating that the observed $V_{th}$ instabilities are likely a fundamental physical property of the $SiC/SiO_2$ system caused by electron trapping in near interface traps. It is important to note that the trapping does not cause permanent damage to the interface like hydrogen bond breakage in silicon based devices and is nearly fully reversible via a negative gate bias.

## Introduction

Wide band gap semiconductor materials like silicon carbide (SiC) promise a better performance for power devices in comparison to silicon based devices. They allow higher operating temperature, higher power density, higher voltage and higher frequency than silicon based devices. Silicon carbide based power MOSFETs have been commercially available since 2011 but still suffer from more severe reliability issues than silicon based devices.

In this work, we study the threshold voltage instability of currently available SiC-MOSFETs or prototypes under positive bias temperature stress (PBTS) which is a key reliability issue. PBTS causes trapping of carriers near the $SiC/SiO_2$ interface which leads to a change in the output characteristics of the devices [1,2]. The shift in threshold voltage scales with applied bias voltage but does not cause permanent damage to the interface itself and is nearly fully recoverable by a small negative bias.

## Experimental Setup

The investigated SiC-MOSFETs are commercially available n-channel power MOSFETs or prototypes produced by four different manufactures. The devices are labeled A, B, C and D to preserve manufacturer anonymity. All measurements were performed with an Agilent B1500A parameter analyzer at various temperatures between -50°C and 150°C. All devices were measured at a drain voltage of $V_D = 0.01$ V. The low-field channel mobility was extracted from device characteristics using the method of Ghibaudo [3] for the devices A, B and D. The extracted mobility values are 8 cm²/Vs for device A, 19 cm²/Vs for device B and 58 cm²/Vs for device D. The mobility value of device C is missing due to unknown channel dimensions. Note that the mobility values of the other samples are below the maximum reported mobilities achieved in some recent studies (e.g. up to 100 cm²/Vs in Ref. [4]). These recent studies were, however, based on lateral MOSFETs not optimized for power electronics and reliability.

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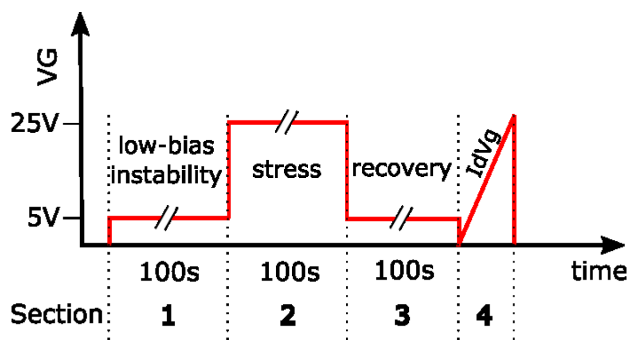


Fig. 1: Test pattern for bias temperature stress tests.

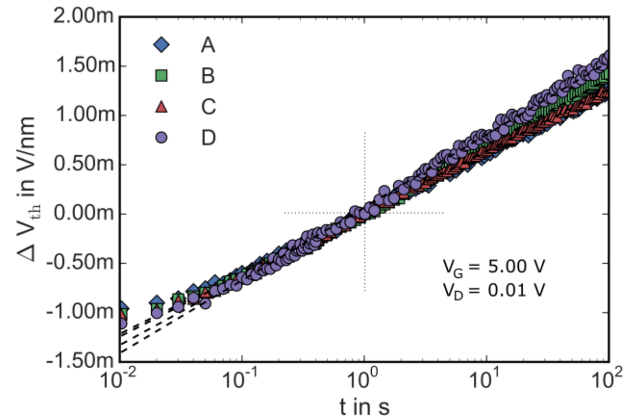


Fig. 2: Low-bias $\Delta V_{th}$ instability at a gate bias of +5 V divided by the oxide thickness.

The devices were subjected to positive bias stress (PBS) according to the test pattern sketched in Fig.1. The sequence consists of 4 different sections: 1) A 100 s long +5 V bias section to measure the low-bias drain current instability visible as a threshold voltage shift ($\Delta V_{th}$) of the devices. 2) A 100 s PBS section at a high bias voltage of +25 V. The applied positive bias stress of +25 V is within the allowed maximum gate bias range mentioned in all datasheets. 3) A 100 s section at +5 V to investigate the time-dependent recovery of the devices after the +25 V PBS. 4) An $I_D$-$V_G$ curve from -2 V to +26 V at $V_D$ = 0.01 V for the conversion of the change in drain current in the areas 1, 2 and 3 into a threshold voltage shift. The whole procedure was repeated at various temperatures between -50°C and 150°C to also investigate the temperature dependence of the low-bias instability and recovery traces.

## Discussion

As indicated in Fig.2, devices A, B, C and D show similar threshold voltage instabilities in the low gate bias regime during a positive bias of +5 V at 30°C within the measurement window from 10 ms to 100 s. The instability follows a logarithmic behavior indicated as dashed black lines with a slope of 0.7 mV per decade per nanometer oxide thickness. All traces are vertically shifted to a threshold voltage shift ($\Delta V_{th}$) of 0 V after 1 s for better comparability. The absolute value of the threshold voltage shift of the different devices originates from the amount of charges captured and emitted during the whole test procedure and already trapped charges before the whole stress procedure and is therefore unknown.

The temperature dependence of the low-bias threshold voltage instability of device A is shown in Fig. 3. We observe a non-temperature dependent behavior of the low-bias instability. Within the measurement range between -50°C and 150°C the low-bias instability has a constant value of 0.7 mV/dec/nm. The same trend is observed for the devices B, C and D (not shown). A temperature independent low-bias $\Delta V_{th}$ is most likely observed due to uniformly distributed trap activation energy in the experimental window.

The recovery traces of the $\Delta V_{th}$ at +5 V after the 100 s long +25 V stress at 30°C are shown in Fig. 4. Again, we observe a similar behavior for devices A (-1.5 mV/dec/nm), B (-1.1 mV/dec/nm), C (-1.4 mV/dec/nm) and D (-1.5 mV/dec/nm).

The temperature dependence of the recovery traces for device A is shown in Fig. 5. Devices B, C and D show a similar behavior (not shown). Unlike the low-bias instability, the recovery slope increases with decreasing temperature. Cold temperatures slow down the emission of trapped carriers. This behavior indicates that a considerable amount of recovery at 30°C takes place outside the experimental window and happens within the first 10 ms after the bias is applied and thus before the first measurement point. The increase in recovery slope is in contrast to silicon based devices, which show a constant recovery slope in a wide temperature range [5].

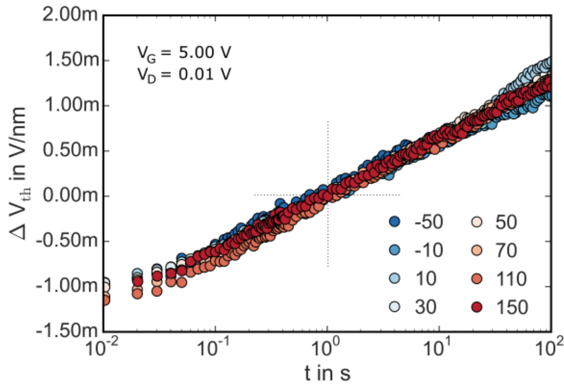


Fig. 3: The low-bias instability divided by the oxide thickness at +5 V does not show any temperature dependence within the measurement range above 10 ms. The picture shows the traces of device A. Devices B, C and D show the same trend.

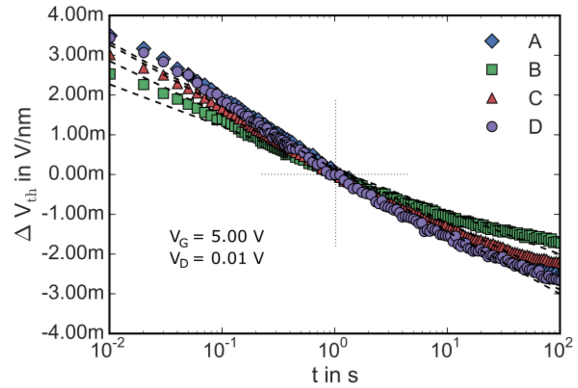


Fig. 4: Recovery of the threshold voltage shift divided by the oxide thickness at a positive bias of 5 V after a positive bias stress of +25 V for 100 s. Devices A, B and C show similar recovery rates while device B shows a slower recovery.

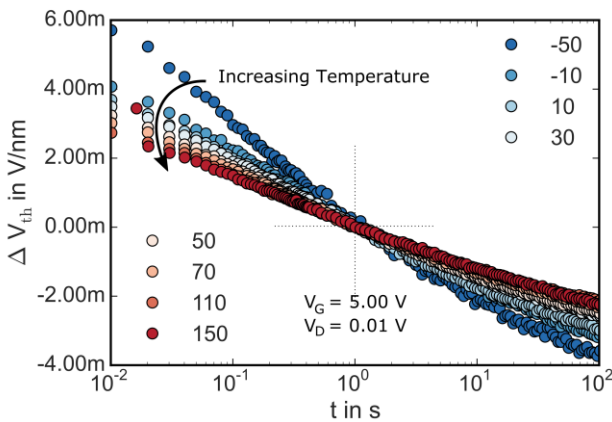


Fig. 5: Temperature dependence of the recovery at +5 V after a +25 V positive bias stress for 100 s (device A). The slope decreases with increasing temperature. The same trend is observed for all devices. This result indicates that most of the recovery already happens within the first 10 ms after the end of the stress pulse.

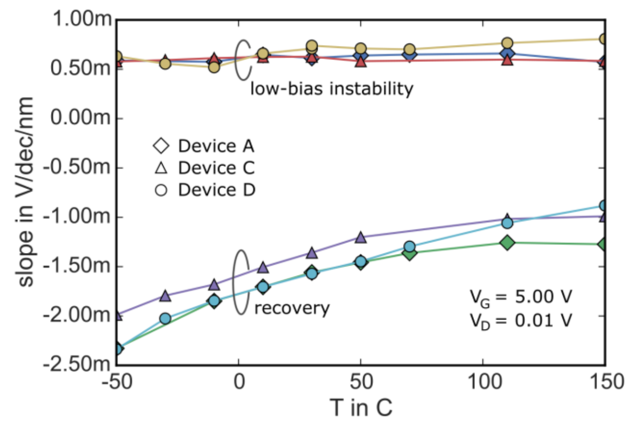


Fig. 6: Temperature dependence for devices A, C and D. The slopes of the low-bias instability at +5 V stay nearly constant in the measured temperature range between -50°C and 150°C at about 0.7 mV/dec/nm for all devices. The slope of the recovery traces increases with decreasing temperature indicating the majority of carrier detrapping occurs within 10 ms after the end of the stress pulse.

A comparison of the recovery and low-bias instability slopes of the devices A, C and D is shown in Fig. 6 indicating temperature independent low-bias instability and increasing recovery slope with decreasing temperature for all devices.

Although the devices from different manufactures differ in the absolute values of the threshold voltage shift, the similar tendencies of all traces indicate that all observed $V_{th}$ instabilities are likely a fundamental physical property of the $SiC/SiO_2$ system and not related to, e.g. mobile ion contamination, fundamental differences in device processing, chip-package interaction or other issues. Unlike in silicon devices, most of the $\Delta V_{th}$ does not originate from a permanent damage of the interface (e.g. H-bond breakage) and is nearly fully recoverable.

## Summary

The SiC-MOSFET devices of all manufacturers show similar $V_{th}$ instabilities caused by trapping and detrapping of charges in oxide or near interface traps. The trapping/detrapping effect appears to be a fundamental property of the $SiC/SiO_2$ system. As opposed to commercially available silicon-based MOSFETs, even an operation at low constant bias causes a $\Delta V_{th}$ in the range of tens of mV. However, the actual mechanism causing the $V_{th}$ instabilities in SiC devices differs from silicon and does not cause a permanent damage to the interface. The more pronounced trapping in the $SiC/SiO_2$ system is likely a consequence of the different energetic positions of the 4H-SiC conduction and valence band edges allowing for a wider range of carrier exchange with traps near the $SiC/SiO_2$ interface.

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