Topical Review

CMOS-compatible spintronic devices: a review

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Abstract

For many decades CMOS devices have been successfully scaled down to achieve higher speed and increased performance of integrated circuits at lower cost. Today's charge-based CMOS electronics encounters two major challenges: power dissipation and variability. Spintronics is a rapidly evolving research and development field, which offers a potential solution to these issues by introducing novel 'more than Moore' devices. Spin-based magnetoresistive random-access memory (MRAM) is already recognized as one of the most promising candidates for future universal memory. Magnetic tunnel junctions, the main elements of MRAM cells, can also be used to build logic-in-memory circuits with non-volatile storage elements on top of CMOS logic circuits, as well as versatile compact on-chip oscillators with low power consumption. We give an overview of CMOS-compatible spintronics applications. First, we present a brief introduction to the physical background considering such effects as magnetoresistance, spin-transfer torque (STT), spin Hall effect, and magnetoelectric effects. We continue with a comprehensive review of the state-of-the-art spintronic devices for memory applications (STT-MRAM, domain wall-motion MRAM, and spin–orbit torque MRAM), oscillators (spin torque oscillators and spin Hall nano-oscillators), logic (logic-in-memory, all-spin logic, and buffered magnetic logic gate grid), sensors, and random number generators. Devices with different types of resistivity switching are analyzed and compared, with their advantages highlighted and challenges revealed. CMOS-compatible spintronic devices are demonstrated beginning with predictive simulations, proceeding to their experimental confirmation and realization, and finalized by the current status of application in modern integrated systems and circuits. We conclude the review with an outlook, where we share our vision on the future applications of the prospective devices in the area.

Keywords: spintronics, magnetoresistance, spin torque, magnetic tunnel junction, spin oscillator, implication-based logic, logic-in-memory

(Some figures may appear in colour only in the online journal)

1. Introduction

The sustainable increase in performance of integrated circuits has been continuously supported by the miniaturization of electronic components and interconnects. The state-of-the art 14 nm technology recently adopted by the semiconductor industry allows manufacturing multi-gate three-dimensional transistors [1].

Even though single devices with a gate length of only a few nanometers are feasible [2], their fabrication and control

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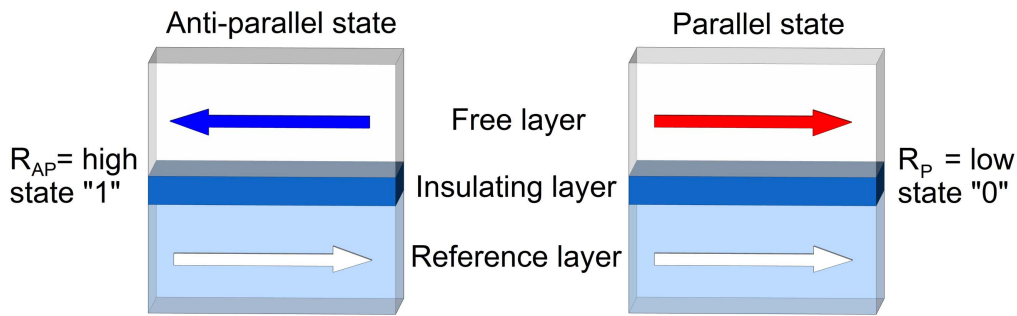
Figure 1. Schematic illustration of a magnetic pillar in a high resistance (left) and low resistance (right) state [17].

is rather difficult which causes reliability issues. Considering also their broad variability and thus high integration costs, the gradual end of scaling is foreseeable. The very heart of the MOSFET operation is the fundamental interaction of the electrons charge with the electrostatic field. However, there is another intrinsic electron attribute—the electron spin—which holds the potential to complement or even replace the currently ubiquitous charge degree of freedom in future electronic devices [3, 4].

The electron spin is commonly determined by its projection along a given axis, the resulting two projection orientations can be exploited for digital information processing. Furthermore, only an extremely small amount of energy is necessary to invert the spin orientation. All spin-based computing exhibits beneficial features such as low supply voltage, small device count, and zero static power [5].

Nevertheless, one must be able to inject, propagate, and detect spin signals for the realization of all spin-based computing, which has only been demonstrated recently. The underlying problem that prevented the successful demonstration of spin injection from a ferromagnetic metal into a semiconductor, is a spin impedance mismatch [6]. A way to resolve this impedance mismatch is to introduce a potential barrier between the metal and the semiconductor [7]. Also the formation of good contacts with low per area resistivity states a critical issue for spin injection. Single layer graphene contacts [8] have been shown to be close to optimal [9].

In contrast to charge, the excess spin injected into a semiconductor is not conserved. During the diffusion of the spin it successively relaxes to zero; the equilibrium value of non-magnetic semiconductors. It has been demonstrated that spin can propagate up to 350 μm through a silicon wafer at 77 K [10]. At room temperature the spin diffusion length is reduced to approximately 200 nm [9]. Confining the electrons reduces the spin lifetime further, because of the increased number of scattering events at the interfaces [11]. In order to compensate this diffusion length degradation, one needs a technology to boost the spin lifetime. In (001) silicon films the intervalley scattering between equivalent valleys is the dominant spin relaxation process. Introducing uniaxial stress along the [110] direction lifts the degeneracy and by this lessens the intervalley scattering [12], which leads to a large increase in the spin lifetime [13]. Since strain has been used to boost the electron mobility for many years, it is

straightforward to employ the same technique to achieve a spin lifetime enhancement.

Recently, InGaAs heterostructures with point contacts have been used to demonstrate purely electrical spin manipulation at low temperatures [14]. Unfortunately, it is very challenging to control the spin in silicon channels via voltage-dependent spin–orbit interaction. Thus, the only option to introduce spin into nanoscale CMOS technology, is to add ferromagnetic source and drain contacts [15]. For such structures the current depends on the relative orientation of the source and drain contacts, which enable the realization of reprogrammable non-volatile logic. Since the up to now achieved magnetoresistance ratios are far worse than the ratios for magnetic tunnel junctions (MTJ), the most reasonable path towards practical spin-driven applications in the near future is to concentrate on MTJ-based solutions.

The most viable option for practical spin-driven applications in the near future is to use an MTJ. An MTJ is a sandwich of two magnetic layers separated by a non-magnetic thin insulating layer. An MTJ exhibits a low resistance state (LRS) or a high resistance state (HRS), depending on the relative magnetization orientation of the magnetic layers (figure 1). The HRS and LRS are mapped to '0' and '1' (or vice versa) [16].

MTJ-based spin-transfer torque-magnetoresistive random-access memory (STT-MRAM) is one of the promising candidates for future universal memory. It combines CMOS compatibility, fast access, non-volatility, and potentially small size and high density [16, 18–20].

In addition, emerging spin-based technology opens an opportunity for manufacturing compact on-chip oscillators, which have great potential as versatile oscillators with low power consumption for consumer electronic products and telecommunication applications.

MRAM can also be used to build logic-in-memory architectures with non-volatile storage elements on top of CMOS logic circuits. Non-volatility and reduced interconnect losses guarantee low-power consumption. Some feasible spin-based solutions are already available and competitive with pure CMOS in respect to energy consumption and speed, nevertheless they are still not able to challenge pure CMOS with regard to integration density.

In this paper we present an overview of CMOS-compatible spintronics applications. In the beginning we will give a brief review regarding the spintronics background, then have
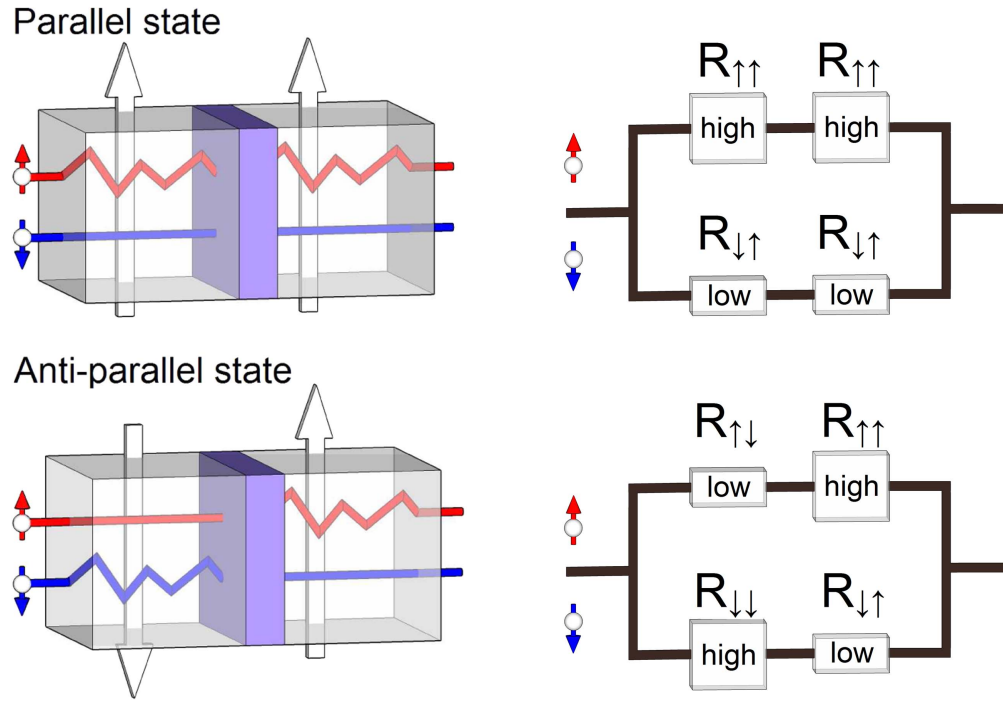
Figure 2. GMR effect in its simplest interpretation [24].

a closer look at the recent progress and discuss the current state-of-the-art of spintronics application for memory, logic, oscillators, as well as other applications (sensors, random number generators).

2. Fundamentals of spintronics

2.1. Magnetoresistance

The most impressive results of spin electronics are the giant magnetoresistance (GMR) and the tunnel magnetoresistance (TMR) effects.

2.1.1. Giant magnetoresistance. In the late 1980s, Baibich *et al* [21] and Binasch *et al* [22] have independently observed GMR in Fe/Cr superlattices. GMR is detected in a pillar consisting of at least two ferromagnetic layers separated by a non-magnetic conducting spacer layer. The resistance of the pillar depends on the layers' magnetization direction relative to each other.

To quantify the GMR effect the following ratio was introduced [23]:

$$\text{GMR} = \frac{R_{\text{AP}} - R_{\text{P}}}{R_{\text{P}}} = \frac{\rho_{\text{AP}} - \rho_{\text{P}}}{\rho_{\text{P}}} = \frac{\sigma_{\text{P}}}{\sigma_{\text{AP}}} - 1. \qquad (1)$$

Here, R_{AP} and R_{P} are the resistances, ρ_{AP} and ρ_{P} are the resistivities, σ_{AP} and σ_{P} are conductivities in the high (anti-parallel) and low (parallel) resistance state, respectively. According to (1) the GMR can be much larger than 1, if $\rho_{\text{AP}} > \rho_{\text{P}}$. For an alternative definition the quantity is less

than 1 ($\rho_{\text{AP}} > \rho_{\text{P}}$) and described as [23]:

$$\text{GMR}' = \frac{\rho_{\text{AP}} - \rho_{\text{P}}}{\rho_{\text{AP}}} = 1 - \frac{\sigma_{\text{AP}}}{\sigma_{\text{P}}}. \qquad (2)$$

In a first approximation one can assume that two independent channels of conductivity exist for electrons with 'spin-up' and 'spin-down' orientations [25]. The total current is the sum of the I↑ current carriers with 'spin-up' and the I↓ current carriers with 'spin-down'. If the currents I↑ and I↓ are flowing through the ferromagnetic layer with a fixed direction of magnetization ('up' or 'down'), the resistance of the first and second group of electrons differs.

The source of the GMR (figure 2) is the unequal scattering of the two groups of electrons with different spin orientations with respect to the magnetization direction of the ferromagnetic layer [25]. If the magnetization directions of the ferromagnetic layers are the same (parallel state), the 'spin-down' electrons (spin is anti-parallel to the magnetization) can propagate through the structure nearly unscattered, resulting thereby in high electron conductivity and hence a low resistance. In contrast, in the anti-parallel state both 'spin-up' and 'spin-down' electrons undergo collisions in ferromagnetic layers, leading to a high resistance [24].

This technology was adopted for hard disk drive read heads and stimulated the new phase of research in magnetic memory, as GMR-based MRAM [26].

2.1.2. Tunnel magnetoresistance. In 1975, Julliere *et al* discovered the phenomenon of the TMR in a Fe/Ge/Co junction at $T \leqslant 4.2$ K [27]. TMR is detected in a pillar consisting from two ferromagnetic layers separated by a thin
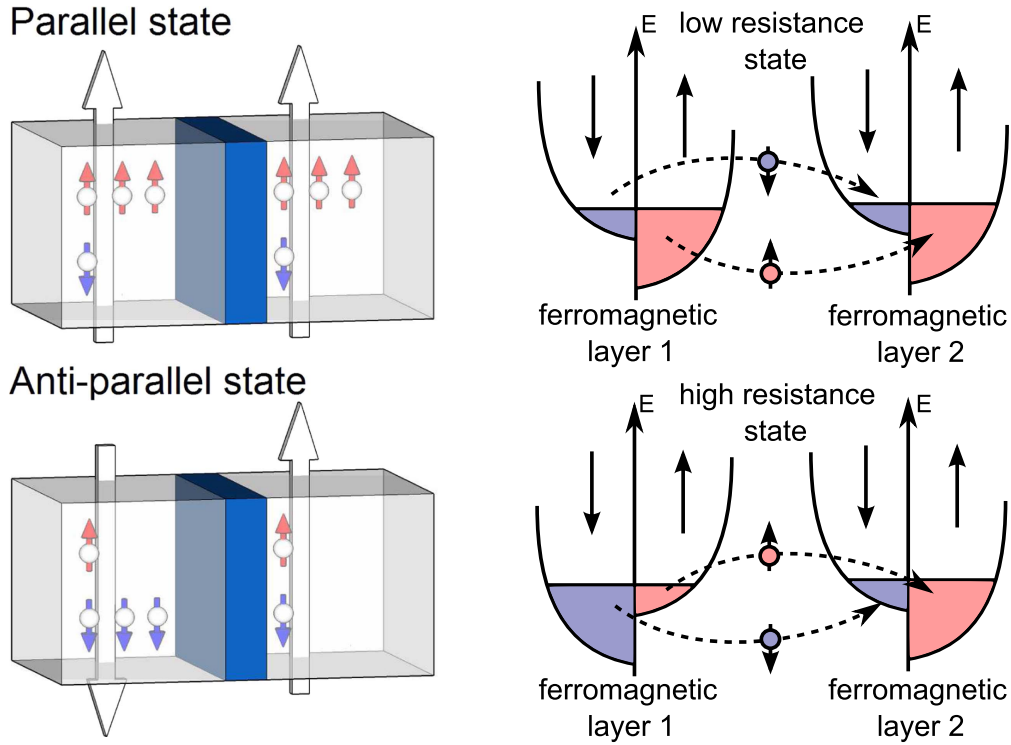
Figure 3. TMR effect in its simplest interpretation.

insulating layer (MTJ). The resistance of the pillar, as in the GMR case, depends on the magnetization direction layers with respect to each other.

To quantify the TMR effect the following ratio is commonly used [28, 29]:

$$\text{TMR} = \frac{R_{\text{AP}} - R_{\text{P}}}{R_{\text{P}}}. \tag{3}$$

Here, R_{AP} and R_{P} are resistances in the HRS and the LRS, respectively.

The simplest interpretation of the TMR effect can be performed as shown in figure 3. The electrons with a certain spin orientation ('spin-up' or 'spin-down') can tunnel from one ferromagnetic layer to another ferromagnetic layer through a non-conductive thin insulating layer, if there are available free states with the same spin orientation. In case of the parallel state, the majority spin ('spin-up') electrons and minority spin ('spin-down') electrons can easily tunnel to the second ferromagnetic layer and fill majority ('up') and minority ('down') states, respectively. This will result in a large conductance and corresponds to the low resistive state. In case of the anti-parallel state, the majority spin ('spin-down') electrons and minority spin ('spin-up') electrons from the first ferromagnetic layer fill the minority ('down') and majority ('up') states in the second ferromagnetic layer, respectively. This will result in a low conductance, which corresponds to the high resistive state.

Despite the fact that the TMR effect was demonstrated earlier than GMR, its use in memory became possible only after observing large TMR in structures with amorphous

Al_2O_3 tunnel barriers. The first developments of structures with amorphous Al_2O_3 tunnel barriers were performed independently by Moodera *et al* [30] and Miyazaki *et al* [31]. The largest TMR ratio of an MTJ with amorphous Al_2O_3 is equal to 70.4% at room temperature and was demonstrated by Wang *et al* [32] in 2004.

The next breakthrough in the development of magnetic memory was the discovery of a giant TMR in an epitaxially grown MTJ with MgO barrier. In 2001 a giant TMR in an MTJ with MgO barrier was independently predicted by Butler *et al* [33] and Mathon *et al* [34]. Mathon *et al* [34] predicted the TMR ratio for an MgO barrier in excess of 1000%. By nature, this effect occurs from the symmetry-based spin filter effect in the MgO barrier [29]. The first experimental observation of TMR in Fe/MgO/FeCo(001) single-crystal epitaxial junctions was made by Bowen *et al* [35]. The experiments showed a much smaller value of TMR (27% at 300 K, 60% at 30 K). In 2004 Parkin *et al* [36] and Yuasa *et al* [37] demonstrated TMR in single-crystal Fe/MgO/Fe MTJ up to 220% and 180% at room temperature, respectively. The TMR of the epitaxially grown MTJ increased rapidly, thanks to the rapid progress in fabrication techniques [28]. In 2006, Yuasa *et al* [38] have shown TMR up to 410%. In 2008, Ikeda *et al* observed giant TMR effects up to 604% at room temperature and 1144% at 4.2 K in junctions of Ta/$Co_{20}Fe_{60}B_{20}$/MgO/$Co_{20}Fe_{60}B_{20}$/Ta [39].

2.2. Spin-transfer torque

In conventional field-induced MRAM the free layer magnetization switching is performed by applying a magnetic field
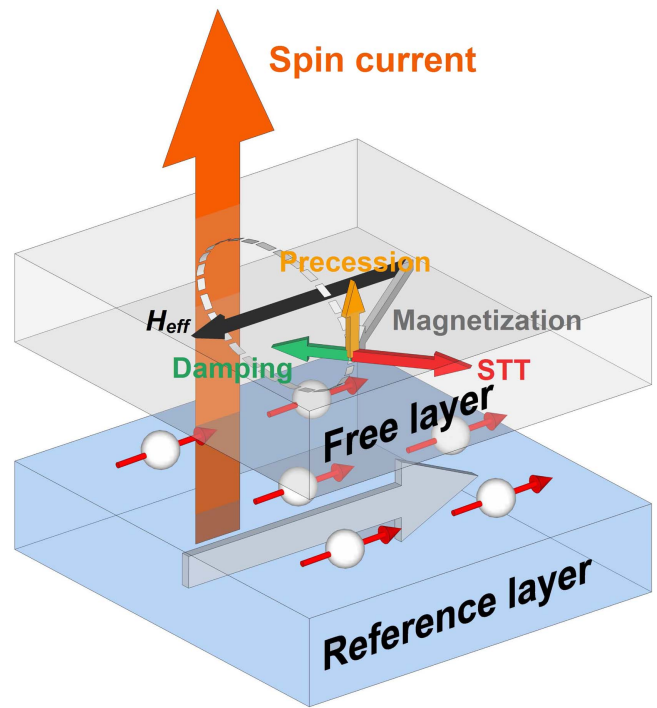
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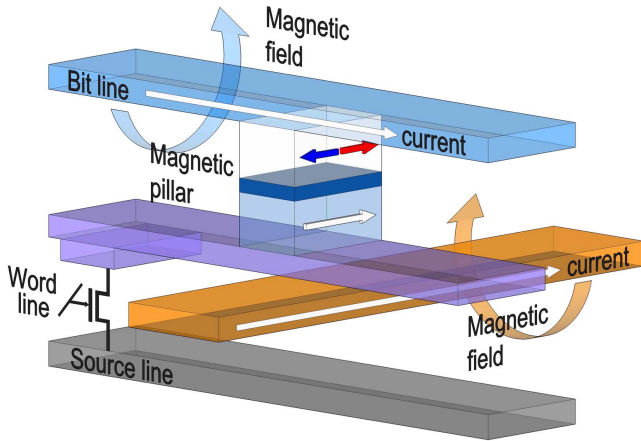
Figure 4. Schematic illustration of field-driven switching MRAM. Reproduced by permission from John Wiley [40].

Figure 5. Schematic illustration of the spin-transfer torque effect.

(figure 4). The write operation is carried out by the current flowing through the wires. Since the currents generate magnetic fields around the wires, switching occurs in the cell only, if the magnetic fields from both currents are present at the magnetic pillar. This protects cells disposed along one of the wires from spontaneous switching. The current required for generating the magnetic field for the switching increases, when the wire cross-section decreases, which leads to a problem for scaling MRAM cells. Therefore, MRAM cells based on a magnetic field switching exhibit a scalability limit of about 90 nm [40].

In 1996, the next breakthrough in the development of spin electronics devices was the theoretical prediction of the STT effect, which was performed independently by Slonczewski [41] and Berger [42]. STT opened a new way of manipulating magnetization dynamics by using spin polarized currents instead of magnetic fields.

In general, when electrons pass through the thick fixed magnetic layer, the spins of the electrons become aligned with the magnetization of this layer (figure 5). When these spin-polarized electrons enter the free layer, their spin orientations are getting aligned with the magnetization of the free layer within a transition layer of a few Ångströms. Because of their spin orientation change in the free layer, they exert a torque on the magnetization of the layer, which can cause magnetization switching, if the torque is large enough to overcome the damping. Smaller torque values result in magnetization precession around the effective magnetic field (H_{eff}). By changing the current polarity the magnetization of the free layer can be switched from the anti-parallel to the parallel state and back with respect to the reference layer.

The interest in MRAM has increased significantly after the observation of spin torque induced switching on all-metallic stacks [40], which happened long after the theoretical prediction of this phenomenon. GMR-based Co/Cu/Co was the first pillar, where spin torque induced switching [43–47] was shown. First AlO$_x$-based and MgO-based STT-MRAM cells were shown in 2004 [48] and 2005 [49], respectively. Figure 6 shows the switching principle of STT-MRAM.
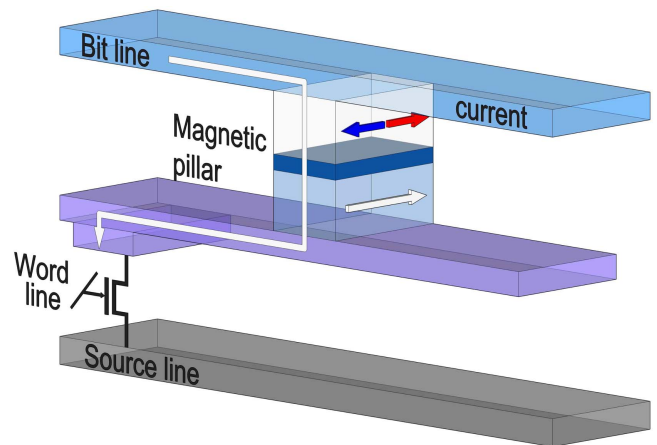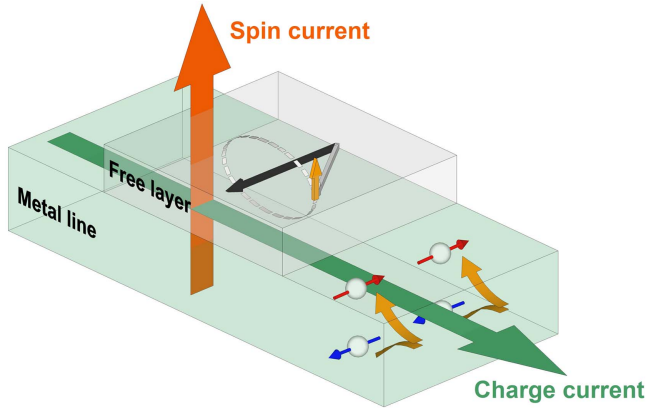

Figure 6. Schematic illustration of STT-MRAM switching. Reproduced by permission from John Wiley [40].

2.3. Spin Hall effect (SHE)

Another effect which can be used to manipulate the magnetization of the magnetic layer is the SHE. In 1971, SHE was predicted by Mikhail Dyakonov and Vladimir Perel [50]. For the SHE (figure 7), the application of a charge current through a non-magnetic material results in the generation of a transverse spin current due to the spin–orbit interaction [51]. The first experimental confirmation of the prediction has been made by Vorob'ev *et al* [52], who observed a change in the rotation rate of the plane of the polarization of light propagated in a Te crystal. The same effect was demonstrated by Yuichiro Kato in 2004 [53]. The first direct electronic measurement of SHE in metals was performed by Valenzuela and Tinkham [54]. Actually, this experiment was later identified

Figure 7. Schematic illustration of a spin Hall effect [56, 57].

as inverse SHE (ISHE). In the ISHE, the spin current generates a transverse current of charge and, when accumulated at the edges of the sample, the charge can be detected electrically [55]. In their experiment Valenzuela and Tinkham injected a spin current from a ferromagnetic electrode into a non-magnetic metal strip and then detected it by the ISHE as well as by the non-local spin-valve effect using a ferromagnetic probe electrode.

Kimura *et al* [58, 59] studied the ISHE and the SHE in a NiFe/Cu/Pt structure in which the spin current was detected by measuring the non-local spin-valve signal and inverse spin Hall measurements. The data provided experimental evidence of the utility of the SHE and the ISHE as a spin injection and detection tool.

2.4. Magnetoelectric effect

Magnetization switching by current involves Joule heating and thus leads to energy dissipation during switching. Replacing the magnetization dynamics manipulation based on the spin polarized current by a voltage-driven effect has the potential for a dramatic reduction in power dissipation [60].

In 2007, Weisheit *et al* [61] demonstrated that the magnetocrystalline anisotropy of FePt and FePd intermetallic compounds can be reversibly modified by an applied electric field. Maruyama *et al* [62] have shown that a relatively small electric field can cause a large change (~40%) in the magnetic anisotropy of a bcc Fe(001)/MgO(001) junction. Shiota *et al* [63] observed a magnetic anisotropy change in $Fe_{80}Co_{20}(001)/MgO(001)$ and demonstrated voltage-assisted magnetization switching. In 2014, high-frequency voltage-assisted magnetization reversal in MgO-MTJ was shown by Nozaki *et al* [64]. They observed a drastic reduction in the switching field by >80%.

The control of the magnetocrystalline anisotropy of ultra-thin ferromagnetic layers using an electric field can be explained by a change of the occupation of atomic orbitals at the interface, which, in conjunction with the spin–orbit interaction, results in a change of anisotropy [60, 65]. This effect can also be described based on the interfacial Rashba effect [60, 66].

3. Spintronic memory

Nowadays, spintronic memory technology is represented by STT-MRAM, domain wall (DW)-motion MRAM, and spin–orbit torque MRAM (SOT-MRAM). The introduction of STT-MRAM into the market has already started [67, 68].

3.1. STT memory

3.1.1. Free layer design. Depending on the orientation of the layer magnetizations the magnetic pillars can be divided into two categories (figure 8): 'perpendicular' with out-of-plane magnetization direction and 'in-plane' with magnetization lying in the plane of the magnetic layer.

Switching of the magnetization can occur not only under the influence of a spin-polarized current, but also spontaneously due to thermal fluctuations (figure 8). This is an unwanted event which leads to the loss of the stored information. Thus, an important parameter of MRAM (STT-MRAM) is the thermal stability factor which is defined as the ratio of the thermal stability barrier to the operating temperature [70]:

$$\Delta = \frac{E_b}{k_B T}. \tag{4}$$

Here, E_b is the energy barrier which separates the two magnetization states, k_B is the Boltzmann constant, and T is the temperature. The energy barrier is defined as $E_b = M_S H_K V / 2$ [70], where M_S is the saturation magnetization, H_K is effective anisotropy field, and V is the volume of the free layer.

The thermal stability factor for perpendicular MTJs (p-MTJs) is given by the interface-induced anisotropy field H_K^{perp} ($H_K = H_K^{perp} - 4\pi M_S$) as [71, 72]:

$$\Delta_{perp} = \frac{M_S \cdot (H_K^{perp} - 4\pi M_S) \cdot V}{2 k_B T}. \tag{5}$$

In [70] it was experimentally demonstrated that increasing the thickness of the free layer leads to the reduction of the effective interface-induced anisotropy field H_K^{perp}. Thus, to increase the thermal stability factor, it is sufficient to increase the cross-section of p-MTJs; however, due to domain formation, the cross-section is limited to approximately 70 nm in diameter, and, therefore, increasing the thermal stability factor of the single free layer p-MTJs above 40–50 is challenging [73, 74].

The thermal stability factor for in-plane MTJ is determined by the shape anisotropy field $H_K^{in-plane}$ ($H_K = H_K^{in-plane}$) [71, 72]:

$$\Delta_{in-plane} = \frac{M_S \cdot H_K^{in-plane} \cdot V}{2 k_B T}. \tag{6}$$

Therefore, to increase the thermal stability factor it is sufficient to increase the thickness of the free layer and/or the
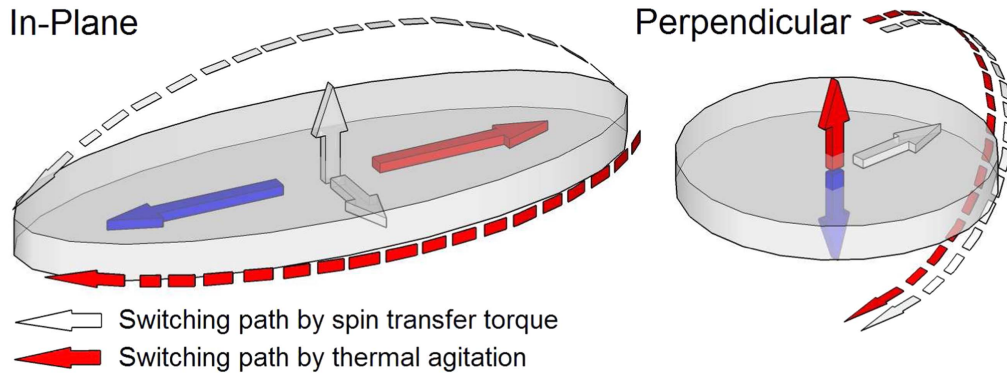
Figure 8. Schematic illustration of the free layer with a 'perpendicular' magnetization (right) and 'in-plane' magnetization direction (left) [69].

aspect ratio between the principal axes defining the elliptical cross-section.

In p-MTJs the switching paths by STT and thermal agitations (figure 8, right) are the same. Thus, the critical switching current I_c (the current which is needed for switching the free layer from its actual magnetization direction to the opposite direction) for p-MTJs is proportional to the thermal stability factor [71]:

$$
\begin{aligned}
I_c^{\text{perp}} &= \frac{1}{\eta} \frac{2\alpha e \mu_0}{\hbar} \cdot M_S \cdot V \cdot (H_K^{\text{perp}} - 4\pi M_S) \\
&= \frac{1}{\eta} \frac{2\alpha e \mu_0}{\hbar} \cdot 2k_B T \Delta_{\text{perp}}.
\end{aligned}
\tag{7}
$$

Here, η is the polarizing factor [41, 75], α is the Gilbert damping parameter, e is the electron charge, μ_0 is the vacuum permeability, and $\hbar$ is the reduced Planck constant.

In in-plane MTJs the switching under the influence of the spin current is following a different path than under thermal agitation (figure 8, left). Along this path the magnetization must get out of plane. This leads to an additional large term $2\pi M_S^2 V$ in the switching current [71]:

$$
\begin{aligned}
I_c^{\text{in-plane}} &= \frac{1}{\eta} \frac{2\alpha e \mu_0}{\hbar} \cdot M_S \cdot V \cdot (H_K^{\text{in-plane}} + 2\pi M_S) \\
&= \frac{1}{\eta} \frac{2\alpha e \mu_0}{\hbar} \cdot (2k_B T \Delta_{\text{in-plane}} + 2\pi M_S^2 V),
\end{aligned}
\tag{8}
$$

which results in a higher critical current compared to that in p-MTJs.

The spin-polarized current is only a fraction of the total charge current flowing through the device. Therefore, high current densities J_c from $\sim 10^7$ to $\sim 10^8$ A cm^{-2} ($J_c = I_c/A_{\text{cs}}$, where A_{cs} is the cross-section area of the free layer) are required to switch the magnetization direction of the free layer, and the reduction of this current density is the most important engineering challenge for the STT-MRAM devices.

Perpendicular cells with an interface-induced anisotropy show potential, but still require a reduction of damping and an increase of thermal stability [17]. The in-plane MTJs exhibit a high thermal stability, but still require a reduction of the critical current density [17].
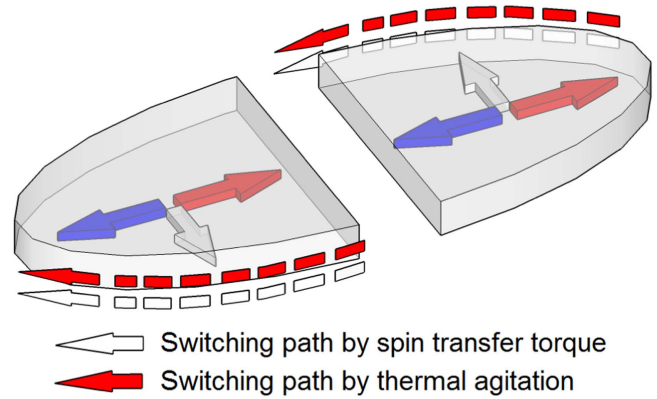
Figure 9. Switching path by STT and thermal agitation for an in-plane composite free layer.

For the solution of this difficulty a composite free layer with in-plane magnetization (figure 9) was proposed [76]. The free magnetic layer of such a structure consists of two equivalent parts of half-elliptic form separated by a narrow non-magnetic spacer (first generation).

As shown by simulating these structures, the switching barrier energy is practically equal to the thermal stability barrier (figure 10), which guarantees the reduction of the critical current similar to the structures with perpendicular magnetization [77]. Simultaneously, these structures are preserving the same dependence of the thermal stability factor as the conventional structure with in-plane magnetization, i.e. to boost the thermal stability factor in composite structures it is sufficient to increase the thickness of the free layer and/or the aspect ratio [78]. In addition, in such composite structures an almost threefold decrease of the switching time as compared to conventional in-plane structures has been found [76, 79]. Also an extremely narrow distribution of switching times is found for the composite structure [78]. In [80], the second generation of the composite free layer was studied. The composite free layer of the second generation is composed of two ellipses with the axes $a/2$ and b inscribed into a rectangle $a \times b$. The simulations show that, while preserving all the advantages of the first generation structure, such as fast switching, high thermal stability factor,
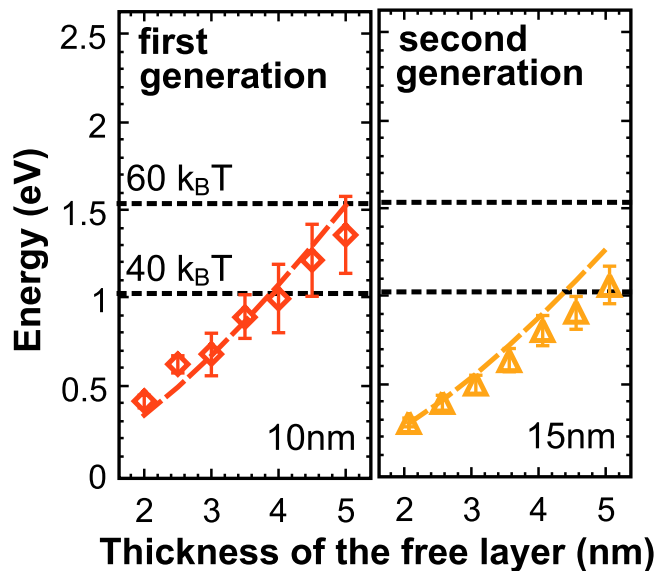
Figure 10. Thermal energy (lines) and switching energy barriers (symbols) as function of thickness of the free layer for two generations of the composite structure. The long axis is fixed at 52.5 nm and the thickness of the fixed layer is 5 nm. Dependences are shown for short axes of 10 nm (first generation) and 15 nm (second generation) length. Each point is a result of statistical averaging with respect to 30 different realizations of the switching process [17].

and very narrow distribution of switching times, the second generation of the free layer can be easier fabricated and offers a higher potential for STT-MRAM performance optimization. A very narrow distribution of switching times of composite structures is useful not only for application in an STT-MRAM memory cell, but also for magnetic sensors [17].

A similar approach to overcome the shortcomings of perpendicular structures is the use of a composite structure with a double-interface [81, 82]. The double-interface perpendicular structure possesses an increased thermal stability compared to the single-interface perpendicular structure [81]. In [82] it was shown that the effective damping constant is also reduced. However, annealing at 400 °C makes it difficult to preserve the low switching current, high TMR (up to 300%), and high thermal stability factor (up to 60) at reduced dimensions.

3.1.2. Magnetic cell architecture. Typical pillar designs for STT-MRAM cells are illustrated in figure 11. In all the structures (except the Pr-MTJ (figure 11(e))) instead of layers with in-plane magnetization layers with perpendicular magnetization or composite free layer can be used. The spacer layer is made from a non-magnetic conducting material (as in the case of the GMR-based devices) or an insulating oxide.

Single MTJ with one tunnel barrier: The SMTJ (figure 11(a)) is the simplest structure. It consists of one reference layer, a spacer layer, and a free layer. The reference layer must be more stable than the free layer in order to prevent the spontaneous switching of the reference layer during memory operation. The reference layer is made

as a synthetic antiferromagnet (SAF). A SAF comprises two magnetic sublayers with opposite magnetizations separated by a thin ruthenium layer to provide a strong antiferromagnetic exchange coupling between the sublayers. At the same time, the opposing magnetizations of the sublayers allow to minimize the impact of the magnetostatic influence of the reference layer onto the free layer. The reference layer is usually strengthened with direct exchange-bias coupling to an antiferromagnetic layer (AFM). The free layer can be formed as SAF, which leads to increased thermal stability.

Dual MTJ with two barriers and ultra-thin dual MTJ cell: the DMTJ (figure 11(b)) is the structure consisting of the reference layer/spacer layer/free layer/spacer layer/reference layer [83–85]. During the switching process the second reference layer provides an extra spin torque. In the anti-parallel configuration of the reference layers (the magnetizations of the two reference layers are anti-parallel), the spin currents from either of the reference layers exert torques in the same direction (full torque is the sum of the individual torques), while in the parallel configuration, the torques are in the opposite directions (full torque is the difference of the individual torques) [86–88]. Thus the switching current can be reduced by almost 2 times [83] in the anti-parallel configuration.

A disadvantage of this structure is the reduced magnetoresistance. Since the reference layers are in anti-parallel configuration, one part of the structure (a reference layer and the free layer) is always in a LRS while another part is in a HRS. This disadvantage can be easily solved by the use of different thicknesses of the spacer layers or different materials for each of the spacer layers.

In order to reduce the overall thickness of the cell in UT-DMTJ (figure 11(c)) each reference layer is not built as a SAF but as a single ferromagnetic layer. The magnetostatic interaction between them further strengthens the anti-parallel configuration of the reference layers.

Cell utilizing thermally assisted switching mechanism: the thermally assisted switching (TAS) mechanism is used in several designs of the magnetic cell [89]. In the first design of a TAS cell a free layer composed from a ferromagnetic material with low Curie point was used [90, 91]. The free layer is heated close to the Curie temperature and after that is switched to a desired direction by applying a small magnetic field. In the second design an interface coupling between the AFM and the ferromagnetic layer is used as the storage mechanism [91]. Both layers are heated above the Néel temperature and then cooled in the presence of a magnetic field in the write direction. The Néel temperature of the antiferromagnetic material is lower than the Curie temperature of the ferromagnetic material. Thus, a relatively modest current is required to heat both layers above the Néel temperature. In principle, both of these designs are covered by the structure shown in figure 11(d).

Cell utilizing precessional switching mechanism: the Pr-MTJ (figure 11(e)) is the structure with two reference layers, one with the in-plane magnetization and the other with the perpendicular magnetization [92]. The reference layer with
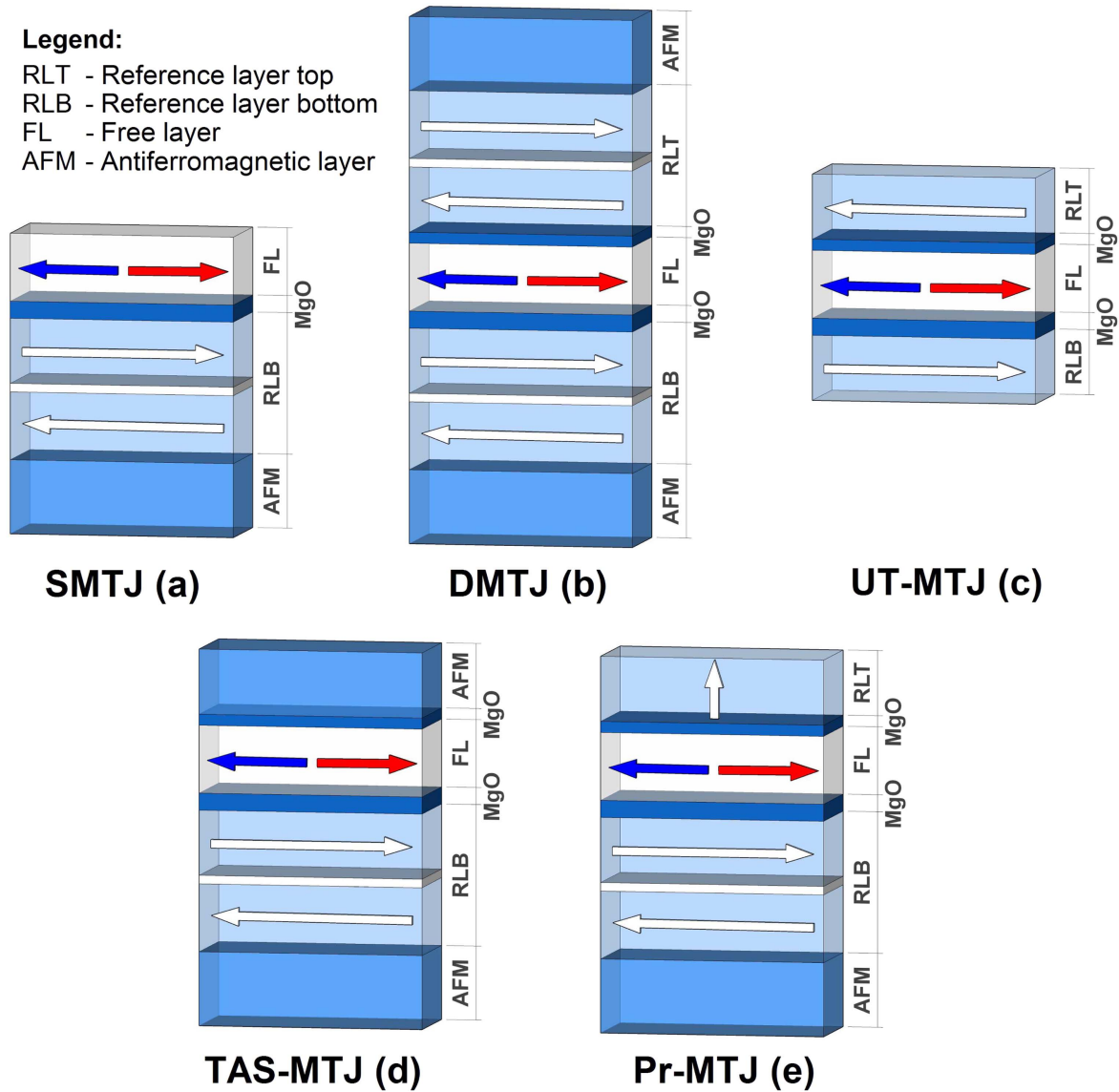
Figure 11. Magnetic memory cell designs: (a) single MTJ with one tunnel barrier (SMTJ), (b) dual MTJ with two barriers (DMTJ), (c) ultra-thin dual MTJ cell (UT-DMTJ), (d) cell utilizing thermally assisted switching mechanism (TAS-MTJ), (e) cell utilizing precessional switching mechanism (Pr-MTJ) [29].

the in-plane magnetization is used for readout of the magnetic state of the free layer. The reference layer with the perpendicular magnetization is used for the switching operation. During the switching operation, the spin torque from the reference layer with perpendicular magnetization affects the magnetization of the free layer causing the magnetization of the latter to tilt out of the plane. This leads to a large demagnetization field perpendicular to the plane of the free layer. This demagnetization field forces the magnetization of the free layer to precess about the direction normal to the free layer plane. Simulations of Pr-MTJ demonstrate that the switching time can be less than 50 ps [92]. A switching time of 500 ps [93] was demonstrated experimentally. Additional improvement of the design is still required to guarantee the necessary free layer final state [94].

3.2. DW-motion-based memory

All of the above designs are made on two-terminal devices with writing based on spin-polarized current and reading based on magnetoresistance (TMR or GMR). These two operations have different requirements for the device. For writing high spin-currents are needed. The memory cell must have a resistance around or below the CMOS FET impedance to guarantee a sufficient write current. However, for reading the resistance must be well above that of the FET impedance to improve the read signal [96]. Thereby, the two main shortcomings of the two-terminal devices are reliability and endurance: indeed, (i) the high write current density can occasionally damage the MTJ barrier and (ii) it remains a challenge to guarantee reliable reading without ever causing switching [97].
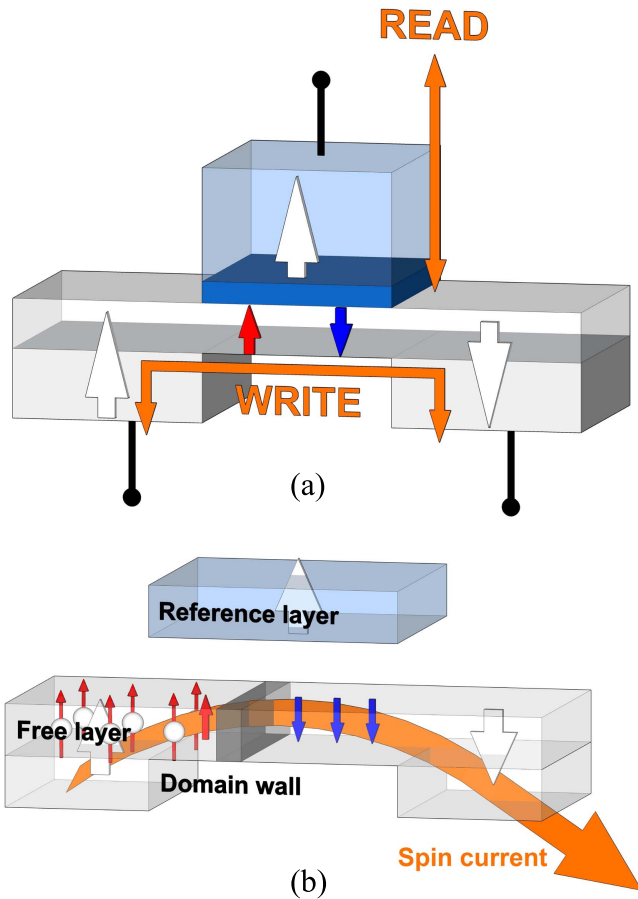
Figure 12. (a) Schematic illustration of a three-terminal memory device with switching based on domain wall-motion in a magnetic wire. © 2014 IEEE. reprinted, with permission, from [95]. (b) Switching principle of domain wall-motion-based memory.

For the solution of this difficulty a three-terminal memory cell was proposed in which different paths are used for read and write operations. Switching in more conventional three-terminal memory devices are based on STT-induced DW-motion in magnetic wires (figure 12). The development of this memory type has begun with the observation of a single DW-motion by an electrical current in a permalloy ($Ni_{81}Fe_{19}$) wire in 2004 [98, 99]. Recently also the DW-motion has been demonstrated in a ferromagnetic semiconductor structure [100]. All first experiments were performed on materials with an in-plane easy axis [98, 99, 101]. In 2008, it was theoretically predicted that the threshold current density necessary for DW-motion in the wire with perpendicular magnetization should be much smaller than that in the wire with in-plane magnetization [102]. Later, DW-motion was demonstrated in Co/Ni wires with perpendicular magnetic anisotropy [103, 104] and in memory cells based on it [105, 106]. In addition, the device with the Co/Ni multi-layer has a higher tolerance to a wide range of temperatures [107, 108] and external field [109]. Using Ta/CoFeB/MgO structures with perpendicular magnetization of the free layer DW-motion-based memory cells were demonstrated in [110].
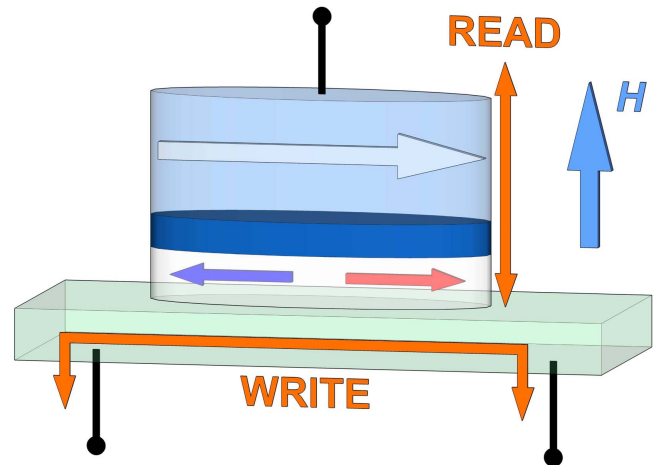
Figure 13. Schematic illustration of three-terminal memory device with a spin–orbit-based magnetization manipulation [113].

The critical switching current density for DW-motion-based memory is described by [111]:

$$j_c = \frac{e\mu_0 M_s \delta H_k}{\pi \hbar \eta},\qquad(9)$$

where δ is the DW width, H_k is the hard-axis anisotropy field, and η is the polarizing factor.

Note, that the critical current density and thermal stability are independent from each other for DW-motion-based memory [111]. Despite all the advantages of this memory type, typical DW three-terminal memory devices require more space and, thus, cause lower area density due to the second transistor required for writing [112].

3.3. SOT memory

Spin–orbit-based magnetization manipulation is also suitable for development of three terminal memory cells, because the switching current does not flow through the barrier layer [114, 115]. Typical spin–orbit-based memory is an MTJ fabricated on a heavy metal channel with large spin–orbit interaction, wherein the free layer is in direct contact with the heavy metal channel (figure 13). Spin torque is induced by the in-plane current through the spin–orbit coupling effect in terms of the Rashba effect and/or the SHE [116–120]. Also an external magnetic field is required for switching as it breaks the symmetry in response to the spin torque and provides the deterministic switching [121]. Recently, switching was shown in MTJs fabricated on Ta [113, 122], W [123] and Ir-doped Cu [124].

Another advantage of spin–orbit-based memory is that this memory demonstrates faster switching than the structure with STT switching [125]. On the other hand, a typical spin–orbit-based memory takes more space as it requires a second transistor for writing [97].

The second transistor issue can be resolved by a pre-selection of an individual cell by means of a voltage pulse applied to the cell simultaneously with powering the spin Hall metal line. The voltage pulse softens the magnetic anisotropy
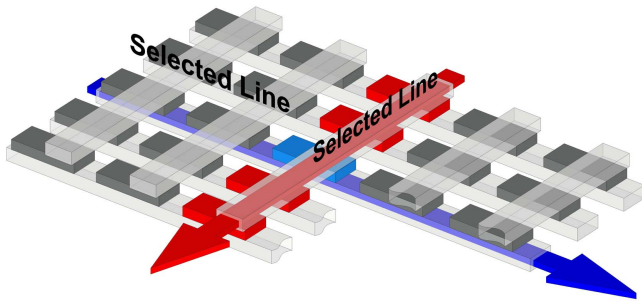
Figure 14. Schematic illustration of cross-point architecture for the switching of the soft magnetic layer by means of consecutive orthogonal subnanosecond current pulses [127].

Figure 15. Schematic illustration of a spin torque oscillator based on two MTJs with shared free layer. Colored arrows indicate the positive direction of the current for each of the MTJs [17].

of the cell's free layer, thus facilitating the magnetization switching of the preselected cell [125, 126]. However, this scheme still requires an external magnetic field.

An alternative method for solving this issue is presented in [127, 128]. The authors proposed a spin–orbit-based memory structure for which the write operation is based on two consecutive orthogonal sub-nanosecond in-plane current pulses. The switching is governed by the torques generated by the SHE. The first pulse is necessary for tilting the magnetization of the soft layer from its stable state and creating a small initial angle. The second pulse is used for switching the soft layer to a new state (figure 14). Switching occurs only in the cell under the influence of both pulses, which allows cells sharing the same heavy metal lines and use select-transistor (or diodes) only for read operation. In contrast to conventional spin–orbit-based memory, this scheme does not require an external magnetic field.

4. Spintronic oscillators

Depending on the physical phenomenon exploited to excite precessions of the magnetization in the magnetic layer the spin-based oscillators can be divided into two categories: spin torque oscillators (STOs) and spin Hall nano-oscillators (SHNOs).

4.1. Spin torque oscillators

In general an STO is formed by a GMR-pillar or an MTJ. The oscillation of the magnetization can be detected as a high frequency voltage by virtue of either the GMR or the TMR effect. The precession frequency of the STOs is tunable in a large range 5–46 GHz both via a DC current or an applied magnetic field [129–132]. Thus, STOs have an extremely wide tunability compared to that of the voltage controlled oscillator (VCO) as well as Yttrium iron garnet oscillators. Another major advantage of the STO is its extremely small size. Indeed, an STO is more than 50 times smaller than a standard LC-tank VCO designed in a CMOS process, mainly due to the large VCO inductor footprint [133]. The STO technology therefore offers a large operation frequency, small size, and low power consumption. Additionally, STOs have a considerable potential for several microwave-based
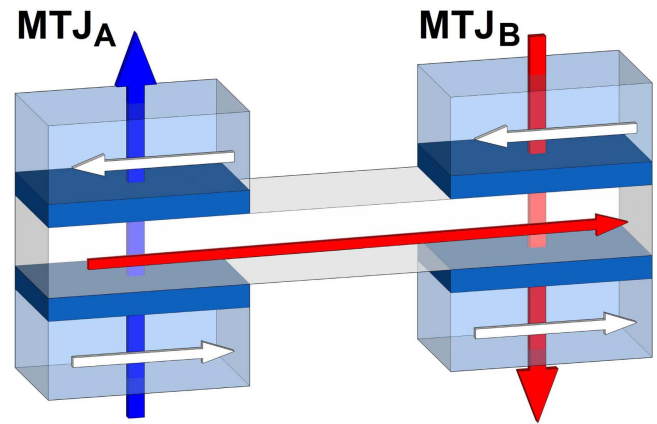
applications e.g., broadband oscillators [129–132], fast modulators [134–139], and sensitive field/current detectors [140].

STOs can be further distinguished by their structure and sub-divided into: (i) nano-contact STOs (NC-STO), in which the current enters into an extended magnetic structure through a constriction-NC and (ii) nano-pillar (GMR-pillar or MTJ) spin torque oscillators.

NC-STOs have been realized in a number of different geometries, and they can be classified according to the number of NCs [141–143].

Depending on the orientation of the free layer magnetization, the nano-pillar STOs can be divided into two categories: 'perpendicular' with out-of-plane magnetization and 'in-plane' with the magnetization lying in plane of the magnetic layer.

STOs based on nano-pillars with in-plane magnetization [144] show high frequency capabilities, but still need a large external magnetic field and are characterized by a low output power level [145]. Oscillators with perpendicular magnetization of the free layer [146] are shown to generate oscillations without an external magnetic field; however, they are also characterized by a relatively low output power. Their low operating frequency, usually below 2 GHz, limits their functionality and application as tunable oscillators [145].

In [147] a bias-field-free spin torque oscillator based on an in-plane MgO-MTJ with an elliptical cross-section but not perfect overlap between the free layer and the fixed magnetic layers was proposed. However, a disadvantage of such an architecture is a narrow range of frequencies and a weak dependence on the current density.

Besides that, an alternative structure based on two MTJs with a shared free layer (figure 15), which shows stable oscillations with high frequency without any external magnetic field has been proposed [148, 149]. In this structure the second MTJ is added in order to prevent the switching of the free layer and to promote an oscillatory behavior. The operating frequency of stable oscillations can be tuned in a wide range by varying the currents density flowing through the

MTJs and in [150] was shown, that the oscillation frequency of such a structure could reach ∼30 GHz.

As shown by simulations [151] the structure based on two MTJs with a shared free layer and with out-of-plane magnetization of the free layer also demonstrates stable oscillations.

Up to now, the power generated by STOs is not yet sufficient for applications. Typically, the conventional GMR-based STO has an output power in the sub-nW range. Higher output power has been achieved in nanopillars based on CoFeB/MgO/CoFeB structures [152–155], but it was still in the nW range.

The synchronization of several STOs has been proposed as a solution to overcome the power issue [136, 142, 156–163]. Similarly, STOs can also synchronize with an external microwave current or a field source, a phenomenon known as injection locking [164–168]. More recently, a parametric synchronization [168–171] was reported, where the frequency of an external microwave field, f_e, is close to twice the STO's free-running frequency, f_0, hence allowing measurements without interference from the external signal. In a related phenomenon called the parametric excitation, the device is biased in a subcritical regime, while maintaining the external signal at $f_e \sim 2f_0$. Urazhdin et al [172] have demonstrated a first experimental observation of the parametric excitation in a NC-STO at cryogenic temperatures, where a microwave field at $2f_0$ was provided via a separately fabricated strip line on top of the STO. A room-temperature approach was demonstrated by Bortolotti et al [173], in which a microwave current flowing through a vortex-based MTJ-STO provided a sufficiently strong Oersted field to parametrically excite the vortex gyration. In 2013, Sani et al [142] demonstrated mutual synchronization of three NC-STOs. However, even in the best case demonstrated the parametric synchronization is still lacking perfect locking and more research is required to further improve the output power and to reduce the phase noise [174].

4.2. Spin Hall nano-oscillator

The precession generated by the SHE can be used to create spin Hall nano-oscillators. An SHNO consists of a non-magnetic layer with high spin–orbit coupling grown on top of a magnetic layer. The device can generate a microwave signal usually in the range of 2–10 GHz useful for telecommunication applications. The devices use pure spin currents created by the SHE in the non-magnetic layer and offer very low power consumption, a broad frequency range (2–10 GHz), and smaller dimensions ($<5\,\mu$m) in comparison to existing technologies.

SHNOs have been fabricated and demonstrated in a number of geometries: (i) nano-gap (disk with triangular contacts) [175, 176]; (ii) nano-constriction [177]; (iii) nano-wire (figure 16) [178].

In 2013, Liu et al [175] showed that SHNOs based on the local injection of spin-current demonstrated relatively large power and small auto-oscillation linewidth at cryogenic temperatures. However, both of these characteristics significantly degrade at increased temperatures due to the excitation of additional modes, resulting in a thermal mode hopping at elevated temperatures [177]. These effects can be avoided, if only a single mode is selectively excited, for example, by controllably modifying the geometrical area of the auto-oscillation. In principle, one could expect that the auto-oscillation area should depend on the experimental conditions such as the spin injection geometry. However, in practice, this approach to control the auto-oscillation characteristics can be challenging [179], since the local injection of the spin current into a continuous magnetic film leads to the spontaneous formation of the so-called 'bullet' auto-oscillation mode [180], whose spatial dimensions are determined by the nonlinear self-localization effects rather than by the spin-current injection area [176, 181].

5. Spintronic logic

As reflected by the ITRS [182] spin-based devices are considered as a promising way to surpass the limits of state-of-the-art CMOS-based logic circuits. For instance, the introduction of non-volatile elements into logic circuits can be used to overcome the exponentially growing standby power dissipation issue [183]. Among the large variety of non-volatile storage technologies STT switched MTJs are very appealing for logic applications [20, 184–186].

5.1. Logic-in-memory

STT-MTJ-based logic circuits can in principle be distinguished into two categories. The first category are CMOS/MTJ circuits, where the MTJs act as mere buffer devices to store the computation results [187–192]. In general these hybrid CMOS/MTJ logic circuits employ MTJs only for storage. The actual logic operations are still carried out by CMOS components. Thus, sense amplifiers are required to read the stored data at each logic stage and to provide the next stage with a sufficient voltage or current signal as input [193]. This not only increases the device count, but also has a detrimental effect on delay and power consumption. There is also no generalization scheme for a transition towards large-scale logic systems, as well as it is difficult to directly compare the different implementations of hybrid CMOS/MTJ logic circuits. Therefore, thorough and extensive studies are required to benchmark the different hybrid CMOS/MTJ logic circuits against each other [194, 195].

The second category bypasses the above explained issues by employing the MTJs as the main computing elements. Indeed, it is possible to eliminate the need for sense amplifiers prior to each logic operation with a non-CMOS logic implementation which is based on MTJs acting as non-volatile storage elements as well as the logic gates [196]. This so called 'stateful' logic enables the realization of non-volatile logic-in-memory applications. In the next section the focus will be put on such spintronic stateful logic gates which allow zero-standby power and enable to shift away from the Von Neumann architecture.
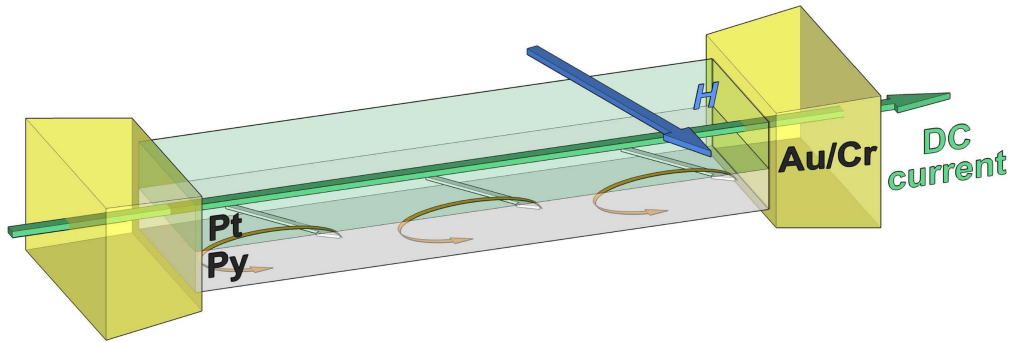
Figure 16. Schematic of a Pt/Py nanowire SHNO device: the external magnetic field is shown as blue arrow, the precessing Py magnetization is shown as white arrows, the green arrow indicates the flow of direct electric current applied to the nanowire. Reprinted by permission from Macmillan Publishers Ltd: *Nat. Commun.* [178], copyright 2014.

5.1.1. Stateful logic gates. In [197–199] it was demonstrated that the direct communication between STT-MTJ devices can be exploited to realize a conditional resistance switching on a target MTJ. The conditional switching depends on the initial resistance (logic) state and is equivalent to a specific Boolean operation. The initial resistance states of the MTJs act as the logic inputs and the resistance states after the operation hold the logic output. Since the for these operations required voltages or currents are fixed and independent of the state of the logic gates, circuits to readout the MTJs' resistance states prior to a subsequent logic operation are superfluous. Thus, stateful logic circuits like the presented MTJ-based one exhibit an extremely simplified architecture in comparison to the hybrid CMOS/MTJ logic circuits with a CMOS-based logic implementation. In the following we will present two types of stateful logic gates which are capable of performing the conventional Boolean logic operations AND, OR, NAND, NOR, and MAJORITY by employing a reprogrammable [197, 198] and an implication-based [199] logic architecture. These stateful logic architectures are of special interest due to their potential for generalization to large-scale logic systems by using STT-MRAM arrays without the addition of extra hardware [196].

5.1.2. Reprogrammable gates. A two- and a three-input reprogrammable logic gate are shown in figures 17(a) and (b), respectively [197, 198]. By selecting the proper preset (TRUE or FALSE) on the output MTJ and subsequently applying the proper voltage (V_A) to the gate, one can realize the well known Boolean (N)AND and (N)OR operations. When the voltage V_A is applied, the resistance states of the input MTJs modulate the current passing through the output MTJ and determine if the critical current for the STT-switching is reached. Depending on the applied voltage V_A and the preset of output MTJ, a conditional switching behavior with respect to the resistance states of the input MTJs is provided for the output MTJ, which corresponds to a particular logic operation [197, 198]. Since the performed Boolean operation can be easily swapped by changing the applied voltage level V_A and/
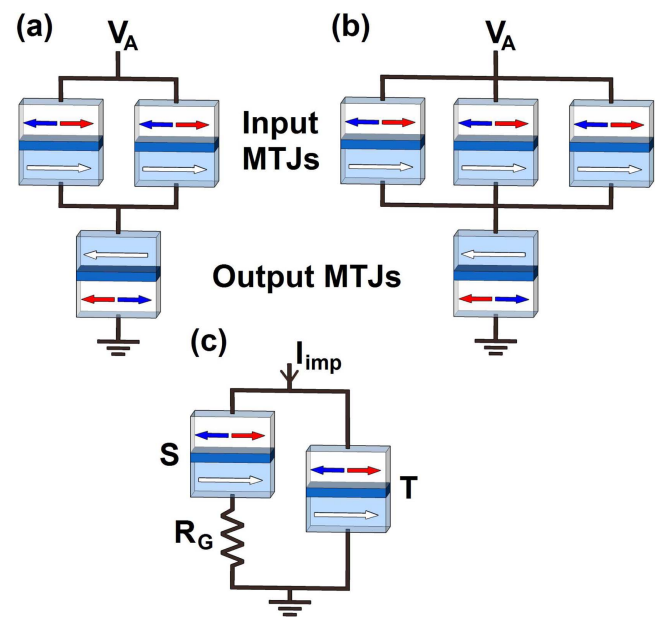
Figure 17. STT-MTJ-based (a) two-input and (b) three-input reprogrammable logic gates [197, 198]. (c) Current-controlled implication logic gate [199].

or changing the preset of the output MTJ, these gates are reprogrammable.

Furthermore, it has been shown that for the two- and the three-input gates there is an optimum V_A with respect to the error probability. It also has been shown that in general the AND and NAND operations feature a higher reliability than OR and NOR [200] (see figure 18(a)). This stems from the fact that for the AND and NAND operation the gate shows a higher current modulation on the output MTJ in comparison to the OR and NOR operation. Comparing the three- and the two-input gate shows that the three-input gate always performs worse than the two-input gate. This can be explained by the smaller current modulation due to the smaller resistance change at the input, when the number of MTJs is increased. This effect also causes major reliability issues for the three-input MAJORITY, OR, and NOR operations [200].
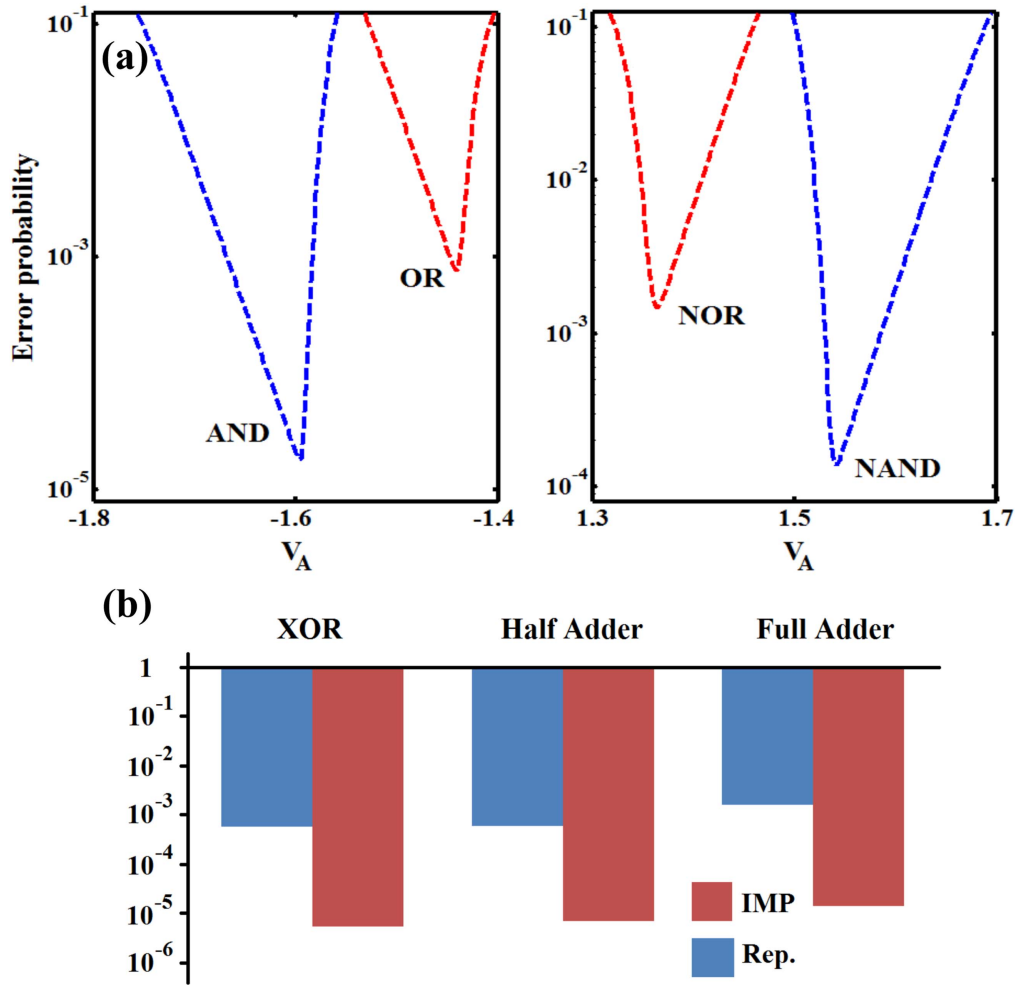
Figure 18. (a) Optimized values of V_A for minimum reprogrammable gate error probability with MTJs characterized in [204]. (b) Minimum error probability of the implication-(IMP) and the reprogrammable-(Rep.) based implementations of XOR, half-adder, and full-adder logic functions.

5.1.3. Implication gates. The fundamental Boolean logic operation called material implication (IMP) can be realized by MTJ-based implication logic gates. The material implication is one of the four fundamental Boolean logic operations, AND, OR, NOT, and IMP [201], but it has been only rarely employed in modern digital electronics. Indeed, the switching algebra introduced by Shannon is based on the other three logic operations [202], since these are readily performed in switching devices and form a computationally complete basis. Nevertheless, the IMP and NIMP (negated IMP) operations form as well a computationally complete logic basis with any of the operations from {NOT, FALSE, XOR, NIMP} and {NOT, TRUE, XNOR, IMP}, respectively. Thus, they can be used to compute arbitrary Boolean functions.

A current-controlled implication logic gate is proposed in [199]. It realizes a conditional switching behavior on the target MTJ depending on the initial logic (resistance) states of both the source and the target MTJ (see figure 17(c)). Depending on the chosen definitions for the high and LRSs, LRS ≡ Logical 1 and HRS ≡ Logical 0 or vice-versa, the realized conditional switching corresponds to the IMP or NIMP operation.

The gate is operated by applying the current I_{imp} to the implication logic gate. When the source and the target MTJ are in the HRS, a high-to-low resistance switching event is enforced on the target MTJ only. The applied current value for I_{imp} is independent of the initial MTJ states and tends to enforce a high-to-low resistance switching on both MTJs. Thus, for the reliability analysis and optimization of the gate, the resistance switching probability for all four initial input combinations has to be taken into account.

A thorough reliability study and comparison between the reprogrammable and the implication logic gates has been carried out in [200]. It has been shown that the error probabilities can be decreased exponentially by increasing the TMR ratio. It also has been shown that for a given TMR ratio the implication gate intrinsically exhibits a more reliable behavior in comparison to the reprogrammable logic gate devices. Due to its superior reliability performance the IMP implementation outperforms the reprogrammable gate for complex logic functions like XOR and full-adder operations and, thus, makes it the implementation of choice for large scale circuits. Figure 18(b) illustrates that the implication-based implementation of more complex logic functions is due
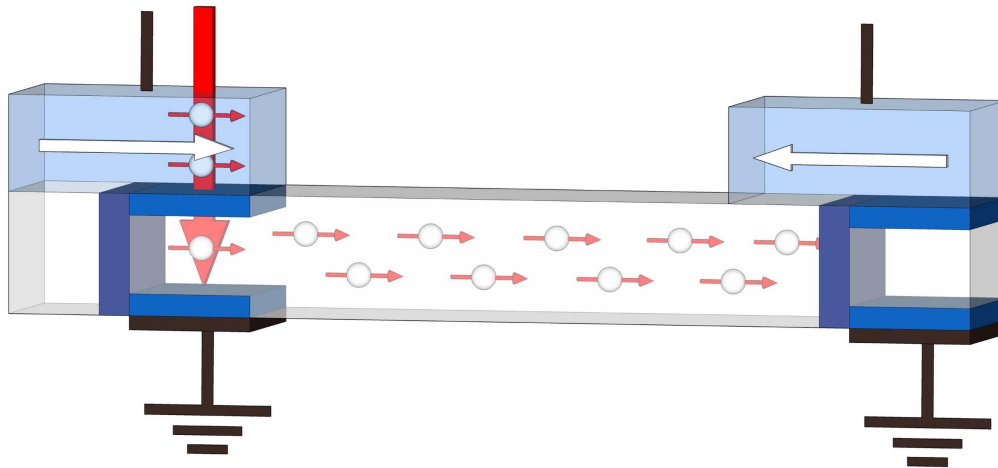
Figure 19. The all spin switch is operated by using the input magnet (left blue layer) to polarize traversing electrons. After they have passed an oxide layer, they enter the interconnect and a spin accumulation forms below the input magnet. From there a spin diffusive current flows towards the output magnet's interface (right blue layer) and exerts a spin-transfer torque. This way the by the input magnetization orientation encoded spin signal can be used to copy information from the input magnet into the output magnet. Reprinted by permission from Macmillan Publishers Ltd: *Nat. Nanotechnol.* [206], copyright 2010.

to its two orders of magnitude higher reliability by far superior in comparison to their reprogrammable logic gate counterpart based on the more reliable AND and NAND operations (figure 18(a)). However, one can further optimize the overall performance like the required number of logic steps, delay, power consumption, and error probability by combining implication-based IMP/NIMP operations and reprogrammable operations in STT-MTJ-based MRAM arrays. The implementation and performance analysis for different MRAM-based complex logic function designs employing a series of sequential operations is shown in [203]. The extension of MRAM arrays to stateful logic allows the execution of logic operations without extra hardware added, which will be elaborated on in the following.

5.1.4. STT-MRAM stateful logic arrays. On the way to a generalized MTJ-based large-scale logic circuit realization of more complex logic functions, some issues have to be addressed before. For instance, is it mandatory to realize a non-volatile logic fan out. This means one must be able to reuse the logic result stored in an implication or reprogrammable gate in a subsequent logic stage. Since the input and output MTJs are physically connected to each other, any additional connection to other MTJs will introduce an extra disturbance to the conditional switching behavior of the output (target) MTJ (as shown in figures 17(a) and (b)).

This limits the possibility of performing logic operations between different arbitrary localized inputs of the logic circuits and highly localizes the logic computation. Even worse, this would also require intermediate circuitry to perform extra read/write operations to readout the information stored in the output (target) and to write it to an input (source) MTJ, which degrades the delay, the energy consumption, and increases the complexity. The implication gate illustrated in figure 17(c) cannot swap the positions for the source and target MTJs for the next logical stage, due to

the structural asymmetry introduced by the resistor R_G. Also in the reprogrammable gate circuit topology the output MTJs cannot change their role from output to input and vice-versa, since their parallel connection restricts the possibility to perform the necessary conditional switching for the MTJ-based logic. Additionally, independent access to all input MTJs is necessary to cover all logic input patterns. Therefore, magnetic field-based switching was used for the input MTJs in [198]. This solution bears the disadvantage of an extra writing wire for the creation of the required Oersted field for switching, which in contrast to the STT-based switching is prohibitive from the energy consumption and scalability point of view [24].

On the other hand, it is very easy to integrate MTJs on top of a CMOS circuit, which can be used to create a one-transistor/one-MTJ (1T/1MTJ) cell. These hybrid CMOS/MTJ technology is a promising remedy to the above mentioned problems for the extension of stateful logic gates to large-scale non-volatile circuits [204]. Due to the fact that the 1T/1MTJ cell is also the basic memory cell for the STT-MRAM structure [19, 205], STT-MRAM arrays can be exploited for logic magnetic circuits and the development of novel non-volatile large-scale logic architectures [196]. Stateful STT-MRAM logic is of special interest as it allows the exploitation of non-volatile MRAM for computing applications without the need for cumbersome intermediate circuitry. It features high flexibility due to its delocalized computation ability and it provides logic fan-out as well. STT-MRAM-based logic is capable of parallel computation execution and thus is suited for high performance parallel non-volatile computation applications as it was demonstrated in [203]. The advantages of the MRAM-based stateful logic are highlighted in [204] by demonstrating the STT-MRAM-based implementation of the fundamental arithmetic functions. By elaborating on design examples like a stateful full-adder, the trade offs for such a technology with respect to the

execution time, the energy consumption, and the reliability of the MRAM-based stateful logic architectures are investigated.

5.2. All-spin logic

The insight that a spin signal is in principle independent from charge transport can be exploited for spintronic logic [206–208]. For this so called 'All-spin logic' physically separated magnets are connected by non-magnetic interconnects (see figure 19). By traversing a charge current through a magnet and its adjacent interconnect, polarized electrons accumulate below the respective magnet in the corresponding portion of the interconnect [209]. This spin accumulation starts to diffuse along the interconnect to the next magnet, where it relaxes and exerts a STT on the magnetization. Since the electrons are immediately absorbed by the grounded bottom contact, the generated spin signal is a pure spin current and can be used for sequential as well as combinational logic [206, 210, 211].

This very intriguing concept has gained a lot of attention and ignited a wide variety of activities which investigate the different aspects of this idea. For instance in [210] schemes for the operation of sequential logic via the examples of a shift register and a ring oscillator are investigated. Reference [208] studies the energy delay for such 'All-spin logic' devices and examines its scaling properties. Also the choice of interconnect materials, their respective advantages and disadvantages, as well as ways for the optimization of the device structure have been investigated [195, 212–218]. Another important step was the development of a generalized framework for modeling of spintronic devices on the circuit level [219].

Even though the decoupling from the charge transport should reduce the power dissipation drastically, the energy estimates for their operation are currently—like for most spintronic technologies—worse than for state-of-the-art CMOS [5, 194, 195]. However, this is easily comprehensible, since semiconductor technology and especially CMOS technology has a head start of many decades with respect to research and hands-on experience. Therefore, it is—in our opinion—a realistic assumption that with growing knowledge and experience the field of spintronics will catch up and might even supersede CMOS for certain applications.

One of the current issues in the field of 'All-spin logic' is that most people employ compact models based on a macrospin assumption for the description of the circuits [216, 218–221]. Since the analysis of circuits with meaningful sizes would be impossible without compact models, they are obviously essential for the investigation and analysis of circuits. But the quality of the by such models gained results severely depends on their physical accuracy. In [222] it is shown, that the assumption of a uniform precession and switching behavior for all magnetic moments in the 'All-spin logic' magnets is not valid. It is further shown that the current flow through the magnet and the associated torque is strongly non-uniform. This has a substantial effect on the overall switching of the magnet and must not be disregarded. Another effect which to the best of our knowledge is ignored in these

models is the pair wise occurrence of torques. By polarizing the electrons before they enter the interconnect and diffuse to the next interface, where the create a STT, there is always a second torque with opposite sign, which acts on the polarizing magnet and destabilizes it [223]. Thus, it is necessary to incorporate those effects into the model descriptions and reinvestigate the 'All-spin logic' on the circuit level.

5.3. Buffered magnetic logic gate grid

5.3.1. STT logic. As already mentioned before, the static power consumption and the interconnection delay have become major concerns in the current CMOS technology [182, 224]. Commonly the dissipated static power is reduced by simply shutting down unused circuit parts. But this comes at the price of losing the information previously stored in the circuit. Thus, it must be recovered, when the circuit is reactivated, which again adds delay and power consumption. In order to avoid this, one must add non-volatile elements to the circuits. Spintronics got a lot of attention due to its potential for such non-volatile elements and circuits. However, the field is very heterogeneous with a wide variety in maturity and readiness for commercial applications [20, 194]. Despite the abundance of ideas for possible CMOS successors, the most probable scenario for a widespread introduction into commercial products within a few years is the combination of CMOS and MTJs to non-volatile hybrids [20, 192, 225–227]. Even though the before presented logic-in-memory applications bear great potential for novel computation concepts and feature high integration density capabilities, they are still limited by the same boundaries as the STT-MRAM. Therefore, researchers are also investigating possibilities to push the limits of the achievable integration density even further [20].

Eventually, this led us to the idea to push more of the CMOS functionality into the spintronic domain to get rid of as many CMOS components as possible. The result is the proposal of a non-volatile magnetic flip flop (NVMFF) and a non-volatile magnetic shift register [228]. The device performs the actual computation in the magnetic domain via the STT effect and the magnetic exchange coupling. Thus, it is possible to reduce the required structural complexity and benefit from the resulting extremely dense layout foot prints. A series of simulation studies were carried out to investigate the capabilities and limits of the NVMFF [229–233]. It also led to the proposal of a novel buffered magnetic logic gate grid which will be explained in detail in the following.

5.3.2. Non-volatile magnetic flip flop. Before going into the details of the buffered magnetic logic gate grid, it is necessary to first explain the NVMFF, the STT majority gate, and their interaction. Thus, their basic principles and their operation will be clear and one can focus on the actual computation environment and its operation. We start with the NVMFF's structure and its operation principle and successively progress to the buffered magnetic logic gate grid and its operation.

As shown in figure 20 the NVMFF consists of three anti-ferromagnetically coupled polarizer stacks featuring out-of-
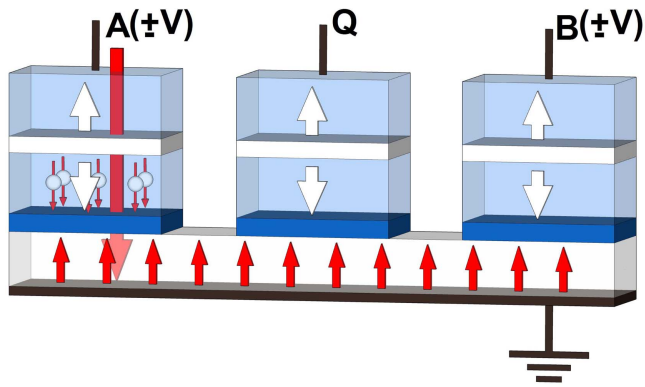
Figure 20. The non-volatile magnetic flip flop is operated by two synchronous current pulses, which are applied to its two inputs *A* and *B*. The binary information of '0' and '1' is encoded in the pulse polarity. The logic state is stored in the common free layer and can be readout at *Q* by either facilitating the GMR or the TMR effect (high or low resistance).

Figure 21. The spin-transfer torque majority gate exhibits a cross shaped common free layer. There is a polarizer stack at each leg of the common free layer. Three stacks are used for input *A*, *B* and *C* and one stack is used for readout *Q*.

plane magnetization. The polarizer stacks are connected to a common free layer (with a perpendicular uniaxial anisotropy) by non-magnetic interconnection layers (e.g. Cu, MgO or Al_2O_3). Two of the stacks are used for input *A* and *B* and one stack is used for readout *Q*. It is further assumed that the stray fields created by the anti-ferromagnetically coupled polarizer stacks are small and can be ignored safely. The actual information is stored in the magnetization orientation of the common free layer and can be accessed by exploiting the GMR effect or the TMR effect. Depending on the relative orientation between the magnetization orientation of the common free layer and the polarizer stack *Q*, either a HRS or a LRS can be read and mapped to logic '0' and '1', respectively. The non-volatile flip flop is operated by polarity encoded current pulses. The positive polarity is assigned to logic '1' and the negative polarity is assigned to logic '0'.

Assuming a grounded metal layer at the bottom of the free layer and applying a positive voltage to one of the inputs (e.g. *A*) will cause the flow of electrons from the bottom contact through the free layer towards the top contact. During their passage through the free layer the electrons' magnetic moment will align parallel to the free layers' magnetization orientation. If the now (partially) polarized electrons try to cross over into the polarizer stack, only a minority of the electrons with magnetization orientations parallel to the polarizer stack is able to enter, while the majority gets scattered and piles up at the interface. There, they relax to the free layer's magnetization again, which exerts a STT on the local magnetization in the corresponding portion of the free layer. The created STT either tries to push the local magnetization into its other stable position or strives to hold the magnetization in its current position. If the torque acts preserving or destabilizing depends on the input currents' polarity as well as on the relative orientation between the electrons' polarization vector and the free layer's local magnetization orientation.

For two synchronously applied input pulses at the stacks *A* and *B*, two STTs are generated. Since the input stacks are
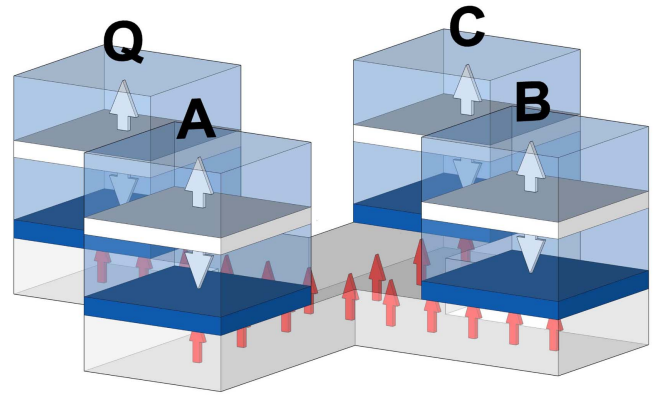
chosen in a way that their magnetization orientations are parallel to each other and much harder to switch than the free layer, the device is restricted to two possible directions for the STT. Depending on the polarity of the input pulses the acting torques either oppose each other and damp the switching (opposing current polarities) or they add up and accelerate the switching (identical current polarities). The resulting device can, if two sufficiently high and long enough current pulses are applied, either HOLD its current state (opposing polarities) or can be SET/RESET (identical polarities). This behavior exactly fits to sequential logic and especially to flip flops and latches [234].

5.3.3. STT majority gate. The non-volatile flip flop and the STT majority gate are not only built out of the same material stack for the common free layer and the polarizers, but also share the information encoding principle by input polarity [229, 235]. Therefore, they are compatible and can be combined into circuits. However, there are a few important differences. The STT majority gate belongs to the group of combinational logic class, while the NVMFF is part of the sequential logic class. Both are essential for building a computing environment and their functionalities perfectly interlock with each other. Another important structural difference is that the STT majority gate possesses a cross shaped common free layer with a uniaxial magnetic out-of-plane anisotropy and four anti-ferromagnetically coupled polarizer stacks (see figure 21). The polarizer stacks are connected to the common free layer by non-magnetic layers and evenly distributed among the legs of the common free layer. The stacks *A*, *B*, and *C* are designated as input stacks and stack *Q* is dedicated for readout. It is an important requirement of the STT majority gate that the number of inputs is odd. For an even number of inputs and the assumption of equal torque strength (identical amplitude) for all inputs, there are always input combinations with an equal amount of logic '0' and logic '1'. The outcome of such an input combination is not well defined, since the torques balance each other perfectly. Therefore, an odd number of
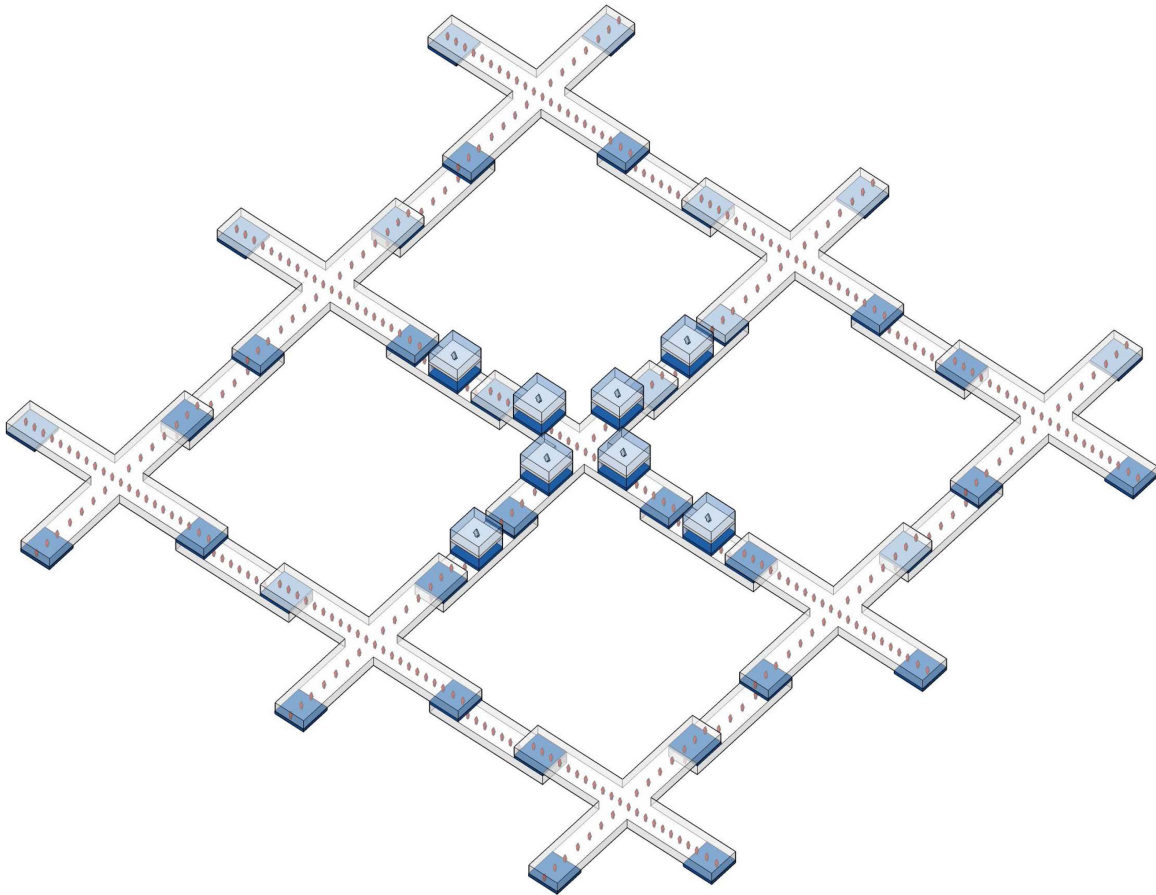
Figure 22. The buffered magnetic logic gate grid combines spin-transfer torque majority gates and non-volatile flip flops. The majority gates act as combinational logic and perform the logic operations (crosses), while the non-volatile flip flops (rectangles) play the role of the sequential logic and act as a shared buffer.

inputs is required, to guarantee that there is always at least one uncompensated torque left, which decides the majority for the operation as outcome. Nevertheless, a logic gate must also be functional complete to perform arbitrary logic operations. NAND and NOR meet this requirement and are commonly used in CMOS logic. The majority function can be split into a two input AND and OR, if one of the inputs is fixed to logic '0' or '1'. Therefore, one must supplement the majority gate with the NOT operation to gain functional completeness. The simplest way to implement the NOT operation, which requires the inversion of the acting torque, is to flip the polarity of the input pulse.

5.3.4. Buffered magnetic logic gate grid. The NVMFF and the STT majority gate are CMOS-compatible and thus able to complement CMOS logic. However, in order to address the leakage power and the interconnection delay issues [5, 183, 194], we proposed to combine both devices to a synergetic buffered magnetic logic gate grid [233]. This way it is possible to reduce the communication between the (external) memory and the logic, while at the same time supplemental CMOS circuits for the signal conversion between the magnetic and CMOS domain become superfluous. The buffered magnetic logic gate grid features

a periodic structure with evenly distributed devices over the wafer plane (shown in figure 22). The STT majority gates and the non-volatile flip flops are placed in two distinct levels and are arranged in a grid like structure. They overlap at their ends with their respective neighbors from the other level and are electrically connected by non-magnetic electrically conducting layers. By adding a top and a bottom contact to each of these overlapping regions it is possible to exploit the overlapping regions for information transport between the different free layers by STT. For instance, if one wants to copy the in the central STT majority gate stored data into a neighboring flip flop e.g. FF1 (see figure 23), then one needs to push a current pulse through the stack of the overlapping region (i.e. C_{out}). Thereby the electrons passing through the STT majority gates' free layer align to the local magnetization and get polarized. Then these electrons traverse through the non-magnetic connection layer and finally enter the flip flops' free layer, where they relax to the local magnetization. Due to the electrons passage of the STT majority gates' free layer the electrons are encoded with the layers magnetization orientation and create an orientation encoded torque in the overlapping region of FF1. As described before a second synchronous pulse (clock signal Clk_1) is applied to copy the information stored in the free layer of the STT majority gate into the free layer of flip flop FF1. The second pulse creates a
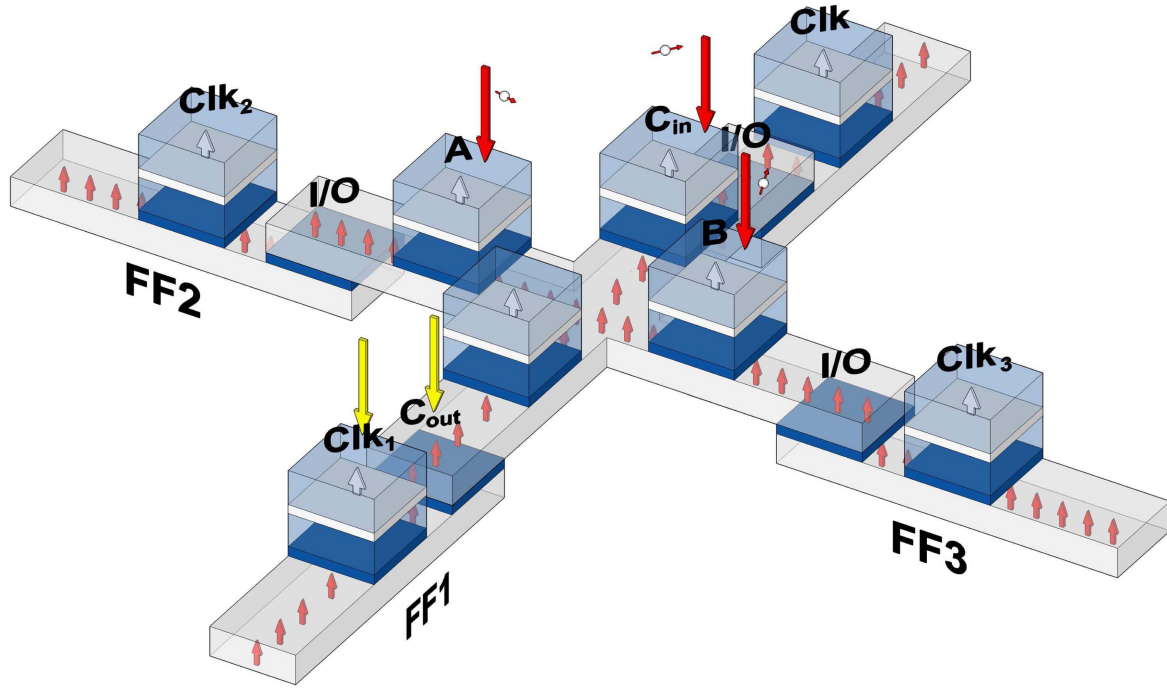
Figure 23. Employing a single majority gate and three flip flops as buffers is already sufficient for the creation of a concatenable one-bit full adder. The key of the interaction is the exploitation of the devices' free layers as polarizers. This way an electron entering a free layer is polarized according to the free layer's magnetization orientation and generates an orientation encoded spin-transfer torque in a subsequent device's free layer.

second torque which aids to prevent the undesired switching of the majority gate during the copy operation before the switching of the flip flop is finished. Due to the faster switching for two active torques (the free layer of FF1 is written) in comparison to one active torque (the free layer of the majority gate is read) at fixed and equal currents, there is a safe time window for the copy operation. The same reasoning can be applied for synchronously copying the information from the surrounding flip flops back to the STT majority gate for a majority operation.

The described structure is not only highly regular, but it is also capable of executing operations in parallel as well as offers the benefit of shared buffers between neighboring logic gates. Thus, it allows to reduce the energy and time spent for the information transport, while at the same time maintaining a very dense layout. Furthermore, it allows to investigate alternatives to the currently performance limiting physical separation of memory and computation units and their required continuous information exchange also known as the Von Neumann architecture. Even more the synergetic combination of the flip flops and the majority gates into a grid enables the flexible allocation of employed resources and allows a generous freedom in reconfiguring its logic. The number of utilized buffers and gates can be easily adjusted depending on the task at hand.

5.3.5. Full adder procedure. In order to demonstrate the potential of the proposed buffered magnetic logic gate grid and help to better understand how this computation environment can be exploited, the example of an easily to

arbitrary bit length extendable one-bit full adder is shown (see figure 23). For this example we assume a one-bit full adder with three inputs A, B, C_{in} and two outputs Sum and C_{out}. Sum describes the sum of the three inputs A, B, C_{in} and is defined as [234]:

$$
\begin{aligned}
\text{Sum} &= A \text{ XOR } B \text{ XOR } C_{\text{in}} \\
&= A \cdot B \cdot C_{\text{in}} + A \cdot \overline{B} \cdot \overline{C}_{\text{in}} + \overline{A} \cdot B \cdot \overline{C}_{\text{in}} \\
&\quad + \overline{A} \cdot \overline{B} \cdot C_{\text{in}}
\end{aligned} \tag{10}
$$

and the carry out bit C_{out} handles the overflow into the next digit for multi-digit additions:

$$
\begin{aligned}
C_{\text{out}} &= \text{MAJORITY}(A, B, C_{\text{in}}) \\
&= A \cdot B + A \cdot C_{\text{in}} + B \cdot C_{\text{in}}.
\end{aligned} \tag{11}
$$

As explained previously the combination of the MAJORITY and the NOT function are sufficient to compute arbitrary complex logic functions. Thus, the Sum function can be converted into a well defined set of successively executed MAJORITY, NOT and copy operations:

- execute MAJORITY(A, B, C_{in})
- copy the result into FF1
- execute MAJORITY(A, B, $\overline{C}_{\text{in}}$)
- copy the result into FF2
- execute MAJORITY($\overline{\text{FF1}}$, FF2, C_{in})
- copy the result into FF3
- C_{out} = FF1 and Sum = FF3

In a first step MAJORITY(A, B, C_{in}) is executed and the result is copied into the first flip flop FF1 (see figure 23). Then the MAJORITY(A, B, NOT(C_{in})) is calculated and subsequently copied into the second flip flop FF2. Finally, we have all the information necessary to calculate the Sum by using the information stored in FF1 and FF2 via the execution of MAJORITY(NOT(FF1), FF2, C_{in}). In a last step the gained Sum is copied into FF3 for future calculations.

C_{out} and Sum are safely stored in FF1 and FF3 and, since these flip flops are accessible to the neighboring STT majority gates, can be exploited for calculations in adjoining gates. For instance, the carry-out bit C_{out} stored in FF1 can be used as carry-in bit C_{in} for the next one-bit adder stage provided by its neighbor STT majority gate. The proposition to calculate C_{out} in the first step was made deliberately to allow to pass C_{out} to a subsequent one-bit adder stage, before the required steps for the calculation of Sum is finished. This illustrates the parallelization potential of the proposed buffered magnetic logic gate grid and highlights its capability to reduce the information transport over the common bus.

For the sake of completeness one has to mention that the realization of a full adder with STT majority gates naturally is also feasible without flip flops [236]. However, this realization is not easily extendable towards large scale integration and also suffers from other issues, which led to the proposal of an alternative solution with in-plane magnetization [237], where a hybrid shift register structure inspired by 'All-spin logic' and the stacking of the magnetic free layers similar to our previously suggested shift register [228, 230] is proposed. Additionally, the exchange of the out-of-plane majority gate cross structure with a ring structure is required to account for the overall switch to in-plane magnetization.

6. Other spin-based applications

As shown above, the major efforts in development of CMOS-compatible spintronic devices are in the fields of spin-based memory, logic, and oscillators. In addition, MTJ-based devices are useful for other applications. The following section gives two examples, namely magnetic field sensors and random number generators.

6.1. Magnetic field sensors

MTJ-based sensors have been widely used in applications, such as field sensors, position, and rotation sensors, due to their large signal, low power consumption, and long endurance [238]. If the magnetic moments of ferromagnetic electrodes in an MTJ are aligned along the same axis, then the MTJ exhibits a hysteresis-like resistance (R) versus applied magnetic field (H). However, for magnetic field sensor applications an MTJ-based device should rather exhibit a linear dependence of the resistance on the applied field. Ideally, $R(H)$ should be non-hysteretic with zero coercivity and show a steep slope (dR/dH) in the sensing regime [239]. In order to achieve this property, several approaches were suggested. In [240, 241] it was demonstrated that by varying the

junction shape, the $R(H)$ curve can be transformed from a hysteretic response curve to a non-hysteretic linear curve. Another way to switch the MTJ to sensing mode is applying a DC field along the hard axes of the ferromagnet, which moves the magnetization of the free layer perpendicular to the reference layer [239]. Later, a structure with MgO/CoFeB as free layer with out-of-plane magnetization, due to a perpendicular magnetic interface anisotropy, was used [242–245]. As an extension of this method, the use of a voltage controlled magnetic anisotropy in a p-MTJ was proposed [246, 247]. MTJ sensors with a superparamagnetic free layer were also proposed [248, 249]. Recently, continued pushing of the detection limits is one of the most significant challenges in MTJ-based magnetic field sensors [250].

6.2. Random number generators

The switching probability of an MTJ can be controlled by the amplitude of the injected current. Therefore, STT switching events can be used as a physical realization of a random number generator [251]. The first spin-based random numbers generating device (spin dice) was build on a conventional in-plane MTJ [252] with the current set to guarantee the switching probability 0.5. However, in-plane MTJs have only a narrow magnetic field range for bistable states and require a high switching current density, which causes practical difficulty in their development as spin dice [253]. Next, a spin dice utilizing top-free-type p-MTJs with a SAF bottom reference layer was proposed [251, 253].

7. Conclusion

The most viable option for practical spin-driven applications in the near future is to use MTJs. We reviewed the recent advances regarding three different CMOS-compatible spintronics applications: memory, oscillators, and logic.

Although the introduction of STT-MRAM into the market has already started, STT-MRAM still has challenges. Perpendicular cells with an interface-induced anisotropy still require a reduction of damping and an increase of thermal stability. The in-plane MTJs exhibit higher thermal stability, but still require a reduction of the critical current density. A structure with an in-plane composite free layer (which combines the advantages of in-plane MTJs and p-MTJs) or double-interface p-MTJs demonstrates potential, but at the same time, fabrication, reliability, and endurance are still challenges for such devices. DW-motion-based memory and SOT-MRAM are free from these limitations; however, compared to conventional STT-MRAM devices, DW-motion-based memory and SOT-MRAM demand more space, which results in a lower integration density. A potential solution is to use the cross-point SOT-MRAM architecture with the switching performed by two subnanosecond current pulses applied to orthogonal buses.

The STOs have a great potential, as they offer large operation frequencies, small size, and low power consumption. STOs based on nano-pillars with in-plane magnetization

show high frequency capabilities, but still need a large external magnetic field and are characterized by a low output power level. Oscillators with perpendicular magnetization of the free layer are shown to generate oscillations without an external magnetic field; however, they are also characterized by a relatively low output power. Their low operating frequencies, usually below 2 GHz, limit their functionality and application as tunable oscillators. STOs based on MTJs with a shared free layer are bias-field-free and provide high-frequency stable oscillations (up to ∼ 30 GHz). However, the power generated by STOs is not sufficient for practical applications yet. Investigations of new structures and materials are required for SHNOs. Parametric synchronization is still lacking perfect locking and more research is required to further improve the output power and to reduce the phase noise.

Concerning spintronic logic, three concepts with the potential for large scale integration have been discussed. The IMP-based logic-in-memory realization in STT-MRAM has the advantage that the technology is already available. Thus, it has the highest potential for the introduction into the market in the next few years. However, from the point of view of scalability, 'All-spin logic' and the buffered magnetic logic gate grid are favorable. Nevertheless, the 'All-spin logic' models have to be extended to cover all important effects and the buffered magnetic logic gate grid needs the realization of first prototypes to advance on the way towards market applications.

In addition, we also have given a brief overview of other spintronics applications: magnetic field sensors and random number generators. MTJ-based sensors have already been widely used as field sensors, position, and rotation sensors, due to their large signal, low power consumption, and long endurance. However, improving the detection limits is one of the most significant challenges. MTJ-based random number generators are relatively new devices with the potential to come into the market in the near future.

Acknowledgments

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