Simulation Analysis of the Electro-Thermal Performance of SOI FinFETs

L. Wang[a*], T. Sadi[a], A. R. Brown[b], M. Nedjalkov[c], C. Alexander[b], B. Cheng[b], C. Millar[b], A. Asenov[a,b]
[a] School of Engineering, University of Glasgow, Glasgow, U.K.,
[b] Gold Standard Simulations Ltd, Glasgow, U.K.,
[c] Institute for Microelectronics, TU Wien, Gußhausstraße 27-29/E360, 1040 Wien, Austria
[*]Liping.Wang @glasgow.ac.uk

***Abstract*— The GSS 'atomistic' simulator GARAND has been enhanced with a thermal simulation module to investigate the impact of self-heating on FinFET DC operation. This thermal simulation module is based on the solution of the coupled Heat Flow, Poisson, and Current Continuity Equations, which is developed for the benefit of computational efficiency. A new formula for the calculation of the thermal conductivity in the fin region is employed considering both fin shape and temperature dependencies. The heat dissipation through the gate is treated by nonhomogeneous Neumann boundary conditions. The electro-thermal simulation results for an SOI FinFET example, designed to meet the specifications for the 14/16nm CMOS technology generation, are presented. The lattice temperature profiles under different external thermal resistances connected to the gate and the corresponding Id-Vg characteristics are investigated and analysed.**

Keywords—FinFET; thermal effects; self-heating effects

I. INTRODUCTION

Self-heating is one of the major concerns for nanoscale semiconductor transistors in terms of performance and reliability. As a result, there is a growing demand for the development of reliable electrothermal models and tools treating more accurately the self-heating effects in nano CMOS devices [1-3]. Simultaneously FinFETs, with their superior electrostatic integrity, performance and variability are replacing the traditional planar MOSFET [4]. However, because of its 3D architecture, the FinFETs' thermal properties are significantly degraded. Self-heating effects will be exacerbated in SOI FinFETs (a schematic of an SOI FinFET is shown in Fig. 1), due to the low thermal conductivity of the buried oxide layer beneath the fin. To maximize the benefits of FinFET technology, an enhancement of TCAD tools is required to allow accurate analysis and modelling of self-heating in FinFETs and its influence on device performance [1-2]. A progressive electro-thermal FinFET simulation study has been presented [5].

Recently, the thermal simulation module in the GSS 'atomistic' simulator GARAND [6] has been enhanced to capture accurately the fin geometry dependence of the thermal conductivity [7-8]. In this paper, GARAND is used to investigate the electro-thermal performance of SOI FinFETs under different external thermal resistances connected to the gate. The paper is organised as follows. In section II we provide a brief description of the simulation methodology, including the new approximate formula for the calculation of the thermal conductivity in the fin region, and the treatment of heat dissipation through the gate. In Section III, the electro-thermal simulation results, for an SOI FinFET example, designed to meet the specifications for the 14/16nm CMOS technology generation, are presented and analysed. The lattice temperature profiles under different external thermal resistances connected to the gate and the corresponding Id-Vg characteristics are investigated. Finally the conclusions are drawn in Section V.

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

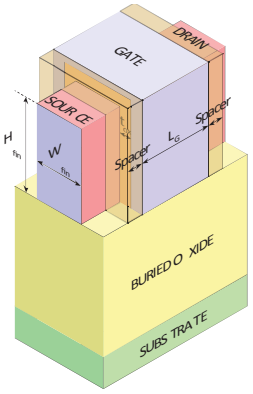


Fig. 1. Schematics of SOI FinFET.

II. SIMULATION METHODOLOGY

A. Coupled electro-thermal simulations

Our electro-thermal simulation module, which is implemented in the atomistic simulator GARAND, is based on the solution of the coupled Heat Flow, Poisson and Current Continuity Equations. The heat flow equation may be derived using phenomenological considerations, beginning with the Fourier law, which relates the heat current and the temperature gradient via the thermal conductivity into a linear response model, equivalent to Ohm's law. The heat flow equation can be written as:

$$\rho c \frac{\partial T_L}{\partial t} = H + \nabla(\kappa \nabla T_L), \qquad (1)$$

where T_L is the lattice temperature, ρ is the mass density, c is the specific heat of the material, κ is the thermal conductivity, and H is the heat generation term. This assumes that the electrons and holes are in thermal equilibrium with the silicon lattice. If Joule heat is considered, the heat generation term can be written as:

$$H = J_n \cdot E_n + H_U \quad (2)$$

where J_n is the electron current densitiy, E_n is the electric field, H_U is the lattice heating due to carrier recombination/generation. Here we focus on the self-consistent solution of the steady-state heat-flow equation. The current density has three components corresponding to a drift term, electron density gradient and temperature gradient terms:

$$J_n = qn\mu_n E_n + k\mu_n T_L \nabla n + +k\mu_n n \nabla T_L \quad (3)$$

where n is the electron density, μ_n is the electron mobility, k is Boltzmann constant.

B. Thermal conduction in the fin

A special thermal conductivity model is developed considering the effects of thermal confinement in FinFETs, where the thickness and width of the fin are less than 100 nm. The thermal conductivity in the fin can be significantly reduced compared to bulk Si, due to phonon-boundary scattering. A new approximate formula is employed in our thermal module for the calculation of the thermal conductivity in the fin region, which generalises a previous 1D paradigm [9] to 2D confined structures by assuming a similar integral dependency in the second direction [7]. For a fin of height h and width w, the thermal conductivity in the fin is given by

$$\kappa(y,z) = \kappa_0(T) \int_0^{\pi/2} \sin^3\theta \left\{1 - \exp\left(-\frac{h}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{h-2z}{2\lambda(T)\cos\theta}\right)\right\} d\theta \int_0^{\pi/2} \sin^3\theta \left\{1 - \exp\left(-\frac{w}{2\lambda(T)\cos\theta}\right)\cosh\left(\frac{-2y}{2\lambda(T)\cos\theta}\right)\right\} d\theta \quad (4)$$

where the offset of the y and z origins is accounted as follows: the z-axis is along the direction of fin height with the top and bottom surfaces of the fin being at z=0 and z=h, and the y-axis is along the direction of fin width with the surfaces of the fin being at y=-w/2 and y=w/2. Using this new calculation method the fin thermal conductivity is estimated to be 1~2 orders of magnitude lower than conventional values for bulk Si.

C. Heat dissipation through the gate

The thermal environment, where heat is dissipated, is a large domain, including transistors, the substrate, the interconnect layers, the die, the heat sink and packaging. The bulk of the thermal resistance lies outside of the usual electrical simulation domain, which is typically restricted to the active region of the device in order to maximize computational efficiency. The inclusion of external thermal resistances to account for heat dissipation into interconnects, the wafer, the case etc. is crucial for thermal simulations.

In FinFETs, the gate almost "wraps" around the channel, which gives excellent control of the conducting channel and very little current is allowed to leak through the body when the device is in the off state. This is beneficial for optimal switching speeds and power. However, the heat dissipation through the gate is more complicated than the source and drain region, because the shape and materials of the gate stack and the surrounding region are much more complex. At thermally conducting interfaces, nonhomogeneous Neumann boundary conditions can be imposed:

$$\kappa \frac{\partial T}{\partial N} = \frac{T_a - T}{R_{th}} \quad (5)$$

where R_{th} is the external thermal resistance, T_a is the ambient temperature, N is the unit vector in the direction of the outer normal at the interface.

III. SOI FINFET EXAMPLE

The material and structure of the SOI FinFET used in this study are shown in Fig. 2. Its channel length is 25 nm with spacers of 6nm on both sides of the gate, while the fin width and the fin height are 12nm and 30nm respectively. A high-k metal gate stack is used. The device parameters are listed in Table I. This SOI FinFET example is designed to meet the specifications for the 14/16nm CMOS technology generation.

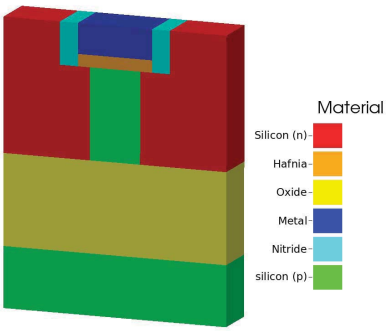


Fig. 2. Materials and structures of the bulk FinFET's electrical simulation domain, showing a cross section.

TABLE I. DEVICE PARAMETERS FOR THE SOI FINFET EXAMPLE

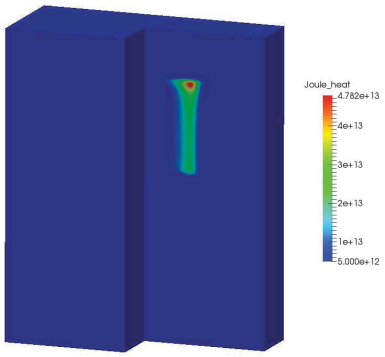
Parameter	Value
L_G	25 nm
Fin Width, W_F	12 nm
Fin Height, H_F	30 nm
Spacer	6 nm
highly doped drain (HDD) profile	2nm/dec (σ=2.1nm)
highly doped drain (HDD) doping	1×10^{20} cm^{-3}
Equivalent Oxide Thickness (EOT)	0.8 nm
Channel doping	1×10^{15} cm^{-3}
BOX depth	30 nm
Supply Voltage	0.9 V

Following the progressive study of a coupled electro-thermal simulation for FinFETs [6], as a further step, in this paper we investigate the impact of external thermal resistances connected to the gate on the electro-thermal performance of the SOI FinFET. Three external resistances are used accounting for heat dissipation through the top of the gate, the front and the back of the gate. By using GARAND with the coupled thermal simulation module, five different cases with various external thermal resistances connected to the gate of the SOI FinFET example are simulated, as summarised in Table II. The external thermal resistances are user-specified parameters for the electro-thermal simulation module. The values used here demonstrate the effect and importance of the choice of relevant thermal resistances. In the simulation, a special thermal conductivity model that considers the effects of confinement in the fin is employed according to Eq. (4). Temperature dependence has been taken into account in the mobility models and saturation velocity. The Masetti model is used for doping-dependent low-field mobility, the enhanced Lombardi model is used for perpendicular field-dependent mobility and the Caughey-Thomas model is used for lateral field-dependent mobility.

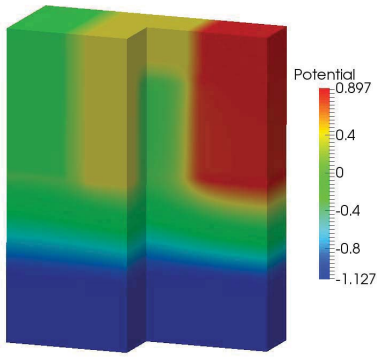
TABLE II. FIVE DIFFERENT CASES WITH VARIOUS EXTERNAL THERMAL RESISTANCES FOR 3D COUPLED ELECTRO-THERMAL SIMULATION

	External thermal resistance connected to		
	Top gate	***Front gate***	***Back gate***
Case 1	4800	32	32
Case 2	4800	320	320
Case 3	4800	3200	3200
Case 4	480	32	32
Case 5	480	320	320

Joule heat and potential distributions at high drain and high gate biases resulting from the 3D coupled electro-thermal simulations for "Case 1" are illustrated in Fig. 3. Lattice temperature distributions at high drain and high gate biases for five cases are illustrated in Fig.4, as well as the temperature variation according to gate voltage at high drain bias. The Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations are illustrated in Fig.5. Because of the much lower thermal conductivity of the fin, a significant hot spot is produced near the drain, where the peak lattice temperature exceeds 420K in all five cases in this study, and strong temperature gradients are also generated in this region. As would be expected, the increase of external thermal resistances raises the lattice temperature. However, the external thermal resistance at different places connected to the gate has a different impact. When external thermal resistances connected to the front and the back of the gate increase by 10 times, the lattice temperature increase by approximately 30 K, and consequently the on-current decreases by 3~7%. Conversely, when external thermal resistances connected to the front and the back of the gate are fixed and external thermal resistance connected to the top of the gate is increased 10 times, there is no obvious impact on the lattice temperature and the corresponding electrical performance. Peak temperature and the average temperature in the fin at the high drain and high gate biases, and the on-current are compared in Table III.

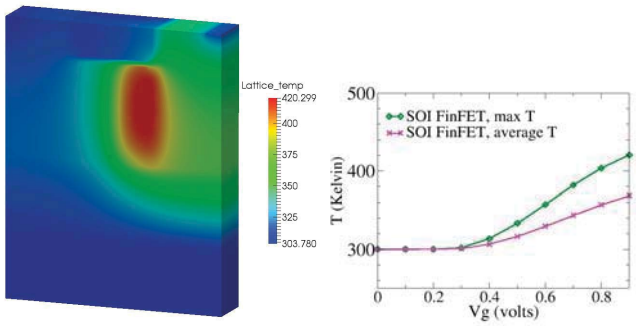


(a)

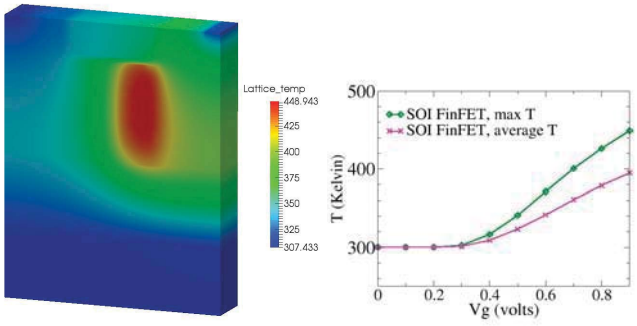


(b)

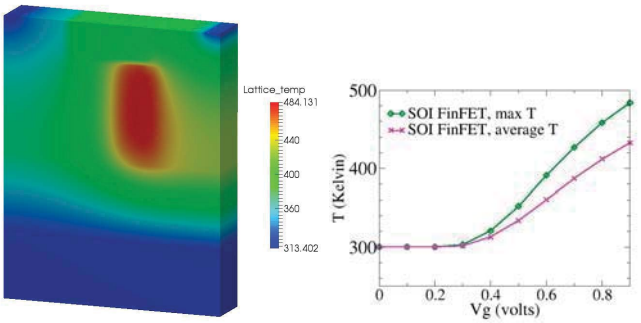
Fig. 3. (a) Joule heat and (b) potential distributions at high drain and high gate biases resulting from the 3D coupled electro-thermal simulations for "Case 1".



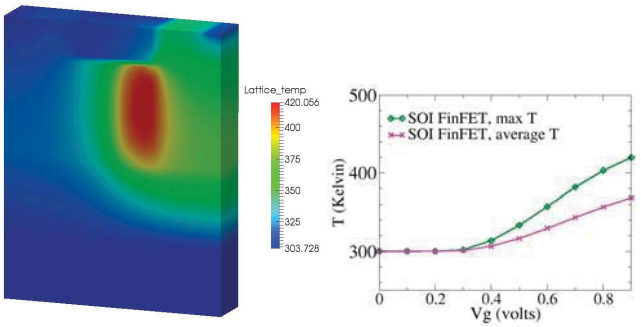
(a) Case 1



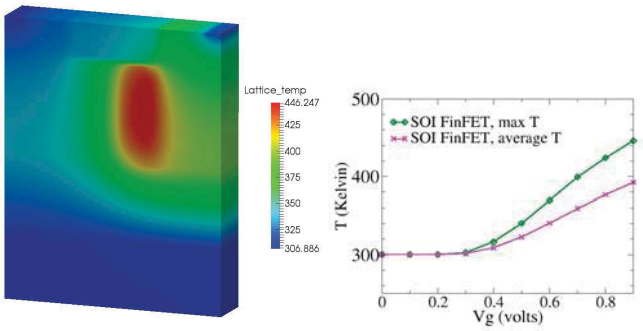
(b) Case 2



(c) Case 3



(d) Case 4



(e) Case 5

Fig. 4. Lattice temperature distributions at high drain and high gate biases (left) and the temperature variation with gate voltage at high drain (right), resulting from the 3D couped electro-thermal simulations for five cases.

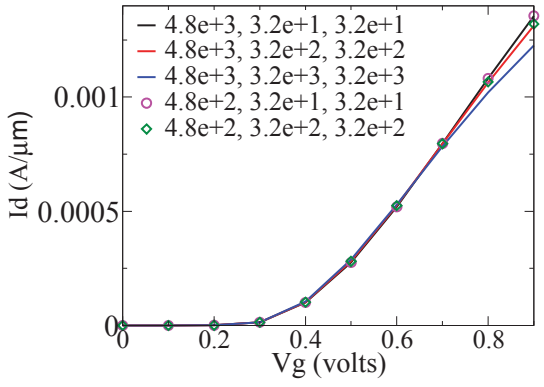


Fig. 5. Id-Vg characteristics at high drain bias from the 3D electro-thermal simulations, comparing five cases.

TABLE III. COMPARISON OF RESULTS FROM THE 3D COUPLED ELECTRO-THERMAL SIMULATION FOR THE SOI FINFET EXAMPLE AT HIGH DRAIN BIAS

	Peak temperature (K)	*Average Temperature (K)*	*On-current (μA)*
Case 1	420.30	368.74	97.54
Case 2	448.94	395.11	94.56
Case 3	484.13	432.71	88.21
Case 4	420.06	368.51	97.57
Case 5	446.25	392.43	95.02

IV. CONCLUSOINS

The electro-thermal simulation capabilities of the drift-diffusion simulator GARAND were enhanced by the development of a thermal conductivity model taking into account the effects of thermal confinement in FinFETs. The 3D coupled electro-thermal simulation results for an SOI FinFET, targeting the 14/16nm CMOS technology generation, has been presented. The lattice temperature profiles under different external thermal resistances connected to the gate and the corresponding Id-Vg characteristics are investigated and analysed. The results show a significant hot spot generated near the drain because of the much lower thermal conductivity of the fin, as the peak lattice temperature exceeds 420 K for all five cases in this study, and strong temperature gradients are also generated in this region. The impact of external thermal resistances at different places connected to the gate is different, consequently affecting the electrical performance of the SOI FinFET.

REFERENCES

[1] I. N. Adisusilo, K. Kukita, and Y. Kamakura. “Analysis of Heat Conduction Property in FinFETs Using Phonon Monte Carlo Simulation, ” Proc. SISPAD 2014, pp.17-20, Sep. 2014.

[2] S. Kolluri, K. Endo, E. Suzuki, K. Banerjee. “Modelling and analysis of self-heating in FinFET devices for improved circuit and EOS/ESD performance,” IEDM 2007, Dec 2007.

[3] T. Sadi, R.W. Kelsall and N. J. Pilgrim, “Electrothermal Monte Carlo Simulation of Submicrometer Si/SiGe MODFETs”, IEEE Trans. Electron. Dev., Vol. 54, No. 2, pp. 332-339, 2007

[4] C. Auth, C. Allen, A. Blattner, et al. “A 22 nm high per- formance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors,” in Proc. VLSI Technol. Symp., pp. 131–132, June 2012.

[5] L. Wang, A. R. Brown, et al. “3D Coupled Electro-Thermal FinFET Simulations Including the Fin Shape Dependence of the Thermal Conductivity,” Proc. SISPAD 2014, pp.269-272, Sep. 2014.

[6] GARAND Statistical 3D TCAD Simulator [Online]. Available: http://www.GoldStandardSimulations.com/products/garand/

[7] L. Wang, A. R. Brown, et al. “Impact of Self-Heating on the Statistical Variability in Bulk and SOI FinFETs,” *IEEE Trans Electron Dev*., Vol.62, No.7, pp.2106-2112, July 2015.

[8] L. Wang, A. R. Brown, et al. “3D Electro-Thermal Simulations of Bulk FinFETs with Statistical Variations,” Proc. *SISPAD 2015,* pp.112-115, Sep. 2015.

[9] D. Vasileska, K. Raleva, S. M. Goodnick. “Electrothermal studies of FD SOI devices that utilize a new theoretical model for the temperature and thickness dependence of the thermal conductivity,” IEEE Trans. Electron. Dev., Vol. 57, No. 3, pp.726-728, March 2010.