# Accurate Mapping of Oxide Traps in Highly-Stable Black Phosphorus FETs

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**Abstract** – We examine *highly-stable black phosphorus field-effect transistors* and demonstrate that they can exhibit *reproducible characteristics for over ten months*. Nevertheless, we show that the performance of these devices is affected by thermally activated charge trapping in oxide traps. In order to characterize these important traps, we introduce a universal experimental technique which allows for *an accurate mapping of the defects with different time constants*. At room temperature the extracted oxide trap densities are close to those reported for more mature $Si/SiO_2$ devices.

## Introduction

Black phosphorus (BP) is a crystalline 2D semiconductor which is now considered for applications in next-generation electronic devices [1]. In particular, a few successful attempts at fabricating black phosphorus FETs (BPFETs) have been reported recently [1–3]. However, so far the poor air-stability of these devices has not allowed any analysis of their reliability, which has only become possible due to the recent introduction of conformal capping [3].

The reliability of all 2D transistors investigated so far is reduced by charge trapping in oxide traps [4, 5], which typically results in a hysteresis of the gate transfer characteristics [6, 7] and threshold voltage shifts [8, 9]. As such, the information about density and energetic alignment of these defects is of utmost importance, especially for such unexplored system as $BP/SiO_2$.

## Devices and Experimental Technique

Our devices are few-layer BPFETs with an 80 nm thick $SiO_2$ insulator and conformal $Al_2O_3$ encapsulation (Fig. 1a). During ten months after fabrication, we have either performed intensive measurements or stored the devices in ambient conditions (Fig. 1b). The $I_d$-$V_g$ characteristics measured at different time intervals remain similar (Fig. 1c). Remarkably, some drifts are observed only after several months of intensive measurements, while long storage in ambient conditions does not have any significant impact on the device performance. Furthermore, the consequtively measured $I_d$-$V_g$ characteristics in a vacuum and in ambient conditions are similar. All this confirms the high stability of our devices.

Aiming to map the oxide traps with widely distributed time constants and different energy levels, we suggest the following experimental technique: An elementary loop consists of measurements of the $I_d$-$V_g$ characteristics in a vacuum in both forward ($V^+$) and reversed ($V^-$) sweep directions using a fixed sweep range $V_{gmin}$ to $V_{gmax}$ and different step voltages $V_{step}$ and sampling times $t_{step}$ [8]. As shown in Fig. 2, the full measurement procedure consists of repeating these loops using either, 1) a fixed $V_{gmin} = -20\,V$ and $V_{gmax}$ varied from 0 to 20 V in 1 V steps or 2) a fixed $V_{gmax} = 20\,V$ and $V_{gmin}$ varied from 0 to $-20\,V$ in $-1\,V$ steps. We express the results in terms of the hysteresis width in the electron/hole branches $\Delta V_{Hn|p}$ versus the measurement frequency $f = 1/(N t_{step})$ [8] curves, which contain the information about the spatial and energy distribution of the density of charged oxide traps.

## Results and Discussion

In Fig. 3a we show the $I_d$-$V_g$ characteristics measured at $T = 165\,°C$ using different sweep rates $S = V_{step}/t_{step}$. As $S$ is decreased, the charge neutrality point $V_{NP}^+$ becomes more negative, which means that some defects become charged while passing through the hole conduction region. At the same time, hole emission which takes place while approaching $V_{gmax}$ leads to a more positive $V_{NP}^-$. As a result, the observed hysteresis is due to both capture and emission. Since both processes are thermally activated, the hysteresis width $\Delta V_{Hn}$ increases versus temperature (Fig. 3b). Furthermore, the total hysteresis width $\Delta V_{Hn}$ is a superposition of the threshold voltage shifts $\Delta V_{Tn}^+$ and $\Delta V_{Tn}^-$ with respect to the fast sweep reference curve (Fig. 3c).

Fig. 4a shows the $\Delta V_{Tn}^+(f)$ and $\Delta V_{Tn}^-(f)$ curves measured using $V_{gmin} = -20\,V$ and $V_{gmax}$ between 1 and 20 V. Clearly, the $\Delta V_{Tn}^-(f)$ curves follow the increase of $V_{gmax}$ along which the number of traps which can emit a hole becomes larger. As such, the concentration of oxide traps which contribute between $V_{gmax}^i$ and $V_{gmax}^{i+1}$ is

$$N_{ot}^i(f) = \left(\Delta V_{Tn}^-(f, V_{gmax}^i) - \Delta V_{Tn}^-(f, V_{gmax}^{i+1})\right)\frac{C_{ox}}{q} \quad (1)$$

To contribute to the charge trapping processes, these traps should be situated within $d \approx 3\,nm$ from the $BP/SiO_2$ interface. Thus, the oxide trap density within the electron conduction region is

$$D_{ot}\left(\frac{V_{gmax}^i + V_{gmax}^{i+1}}{2}, f\right) = \frac{N_{ot}^i(f)}{d \mid V_{gmax}^{i+1} - V_{gmax}^i \mid} \quad (2)$$

The results for $V_{gmax} = 20\,V$ and $V_{gmin}$ between 0 and $-20\,V$ are shown in Fig. 4b. Since $V_{gmin}$ impacts the number of traps which can capture a hole, we use the $\Delta V_{Tp|n}^+(f)$ dependences for an analogous extraction of $D_{ot}$ within the hole conduction region.

Taking into account the previously extracted position of the trap level $E_T$ [9], we next evaluate the energy distributions $D_{ot}(E)$, see Fig. 5. At higher temperatures these distributions are more sensitive to the measurement frequency, while the trap density is larger. As such, our results are fully consistent with thermally activated charge trapping. At the same time, the shape of the $D_{ot}(E)$ curves is well reproducible at different temperatures. This confirms both the accuracy of our technique and the high stability of the BPFETs.

Finally, in Fig. 6 we compare the typical $D_{ot}$ extracted for our BPFETs with literature values for different technologies [10–17]. At room temperature the density of active oxide traps in our devices is $\sim 10^{17}\,cm^{-3}/eV$, which is close to $Si/SiO_2$ FETs. At the same time, this is considerably lower than for $MoS_2/SiO_2$ and Si/high-k devices ($10^{19}$–$10^{20}\,cm^{-3}/eV$). Although at $T = 165\,°C$ $D_{ot}$ increases, the obtained values ($\sim 10^{19}\,cm^{-3}/eV$) remain reasonable.

## Conclusions

We have performed an accurate mapping of oxide traps with widely distributed time constants for our highly-stable BPFETs. Although the thermal activation of charge trapping is very important, we found that at room temperature the obtained values of the oxide trap density can be *comparable to Si technologies*. As such, we conclude that *a considerable advancement in the manufacturing and technology of next-generation 2D FETs has been obtained*.

*Acknowledgements:* MoRV project n° 619234 and FWF grant n° I2606-N30. D.A. acknowledges the support of the NSF and the ONR.

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978-1-5090-4660-7/17/$31.00 ©2017 IEEE 2017 IEEE Electron Devices Technology and Manufacturing Conference Proceedings of Technical Papers

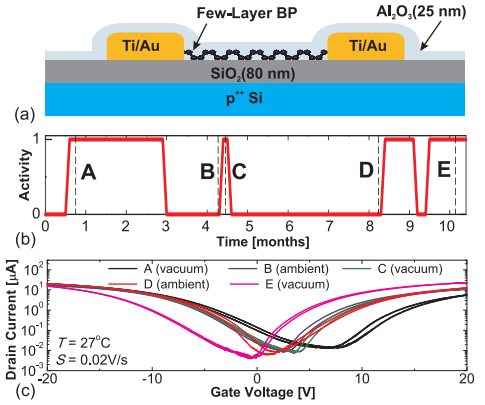


**Fig. 1:** (a) Schematic layout of our BPFETs ($L = 500\,\text{nm}$) with $Al_2O_3$ encapsulation. (b) Measurement activity versus time since fabrication. "0" means that the devices have been stored in ambient conditions, while "1" expresses intensive measurements in vacuum (mostly stressing) up to $T = 165\,^\circ\text{C}$. (c) The $I_\text{d}$-$V_\text{g}$ characteristics measured for the same device at different stages of our long-term study (as marked in (b)).

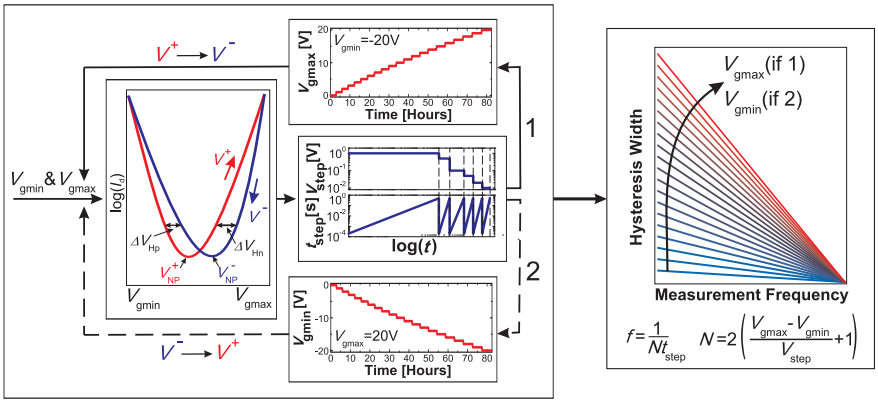


**Fig. 2:** Schematic illustration of our experimental technique. We measure the $I_\text{d}$-$V_\text{g}$ characteristics at $V_\text{d} = 0.1\,\text{V}$ in both sweep directions using the step voltage $V_\text{step}$ range [1 V…0.01 V] and sampling time $t_\text{step}$ varied between 0.2 ms and 0.5 s for each $V_\text{step}$, i.e. the sweep rate $S = V_\text{step}/t_\text{step}$ between 0.02 and 5000 V/s. The measurements are repeated with either $V_\text{gmin} = -20\,\text{V}$ and $V_\text{gmax}$ varied between 0 and 20 V (1) or with $V_\text{gmax} = 20\,\text{V}$ and $V_\text{gmin}$ varied between 0 and −20 V in −1 V steps (2). As a result we obtain two sets of the hysteresis width versus measurement frequency ($\Delta V_\text{Hn|p}(f)$) characteristics which contain the information about the distribution of the charged oxide traps with different time constants. Interestingly, although each measurement loop takes over 80 hours, our BPFETs remain highly stable.

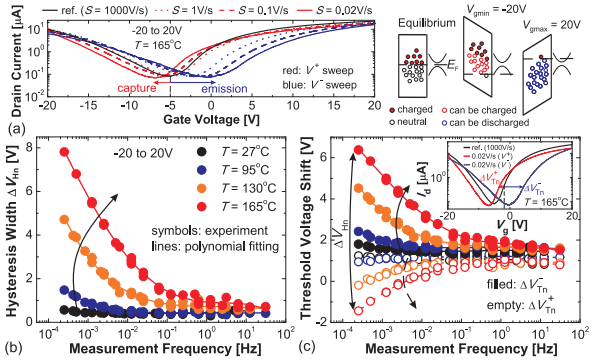


**Fig. 3:** (a) The $I_\text{d}$-$V_\text{g}$ characteristics measured using different sweep rates. For slow sweeps, many defects can become charged within the hole conduction region. This makes $V^+_\text{NP}$ more negative than it was for the reference curve ($S = 1000\,\text{V/s}$). At the same time, large $V_\text{gmax}$ leads to a more positive $V^-_\text{NP}$ due to a hole emission. (b) The $\Delta V_\text{Hn}(f)$ curves are consistent with thermally activated charge trapping. (c) The total hysteresis width can be split into the threshold voltage shifts $\Delta V^+_\text{Tn}$ and $\Delta V^-_\text{Tn}$ (inset) with respect to the reference $I_\text{d}$-$V_\text{g}$ curve.

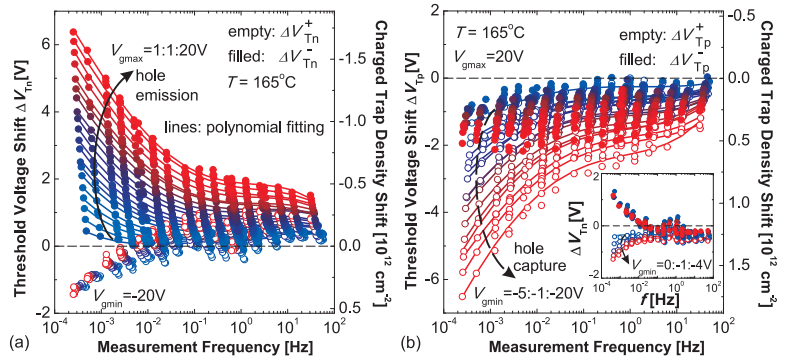


**Fig. 4:** (a) The $\Delta V^+_\text{Tn}(f)$ and $\Delta V^-_\text{Tn}(f)$ characteristics obtained at $T = 165\,^\circ\text{C}$ for $V_\text{gmin} = -20\,\text{V}$ and $V_\text{gmax}$ from 1 to 20 V. While for larger $V_\text{gmax}$ the number of defects which can emit a hole becomes larger, the distances between the $\Delta V^-_\text{Tn}(f)$ curves are proportional to the concentrations of oxide traps which discharge within the corresponding $V_\text{g}$ interval. (b) The $\Delta V^+_\text{Tp}(f)$ and $\Delta V^-_\text{Tp}(f)$ characteristics obtained for $V_\text{gmax} = 20\,\text{V}$ and $V_\text{gmin}$ from −5 to −20 V. Since $V_\text{gmin}$ determines the number of traps which can become charged, we analyze the distances between the $\Delta V^+_\text{Tp}(f)$ curves. However, since for $V_\text{gmin}$ from 0 to −4 V $\Delta V^+_\text{Tp}$ is not accessible, we have to use the $\Delta V^+_\text{Tn}(f)$ curves (inset).

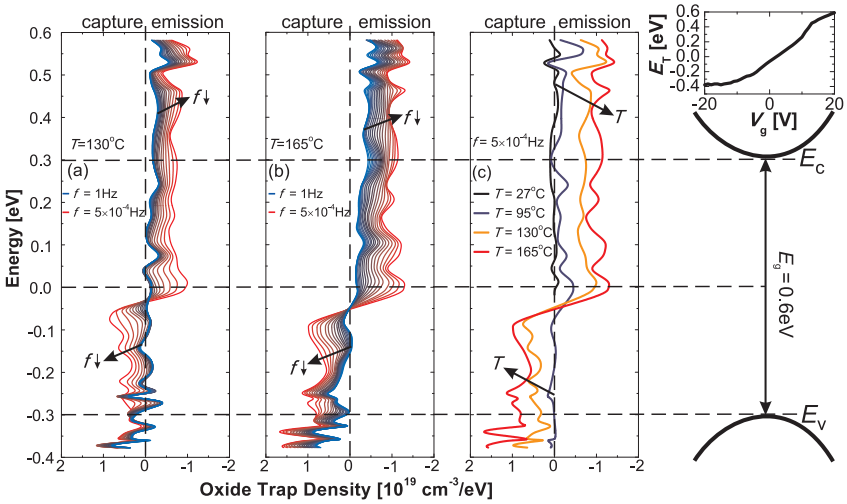


**Fig. 5:** The differential energy distributions $D_\text{ot}(E)$ for (a) $T = 130\,^\circ\text{C}$ and (b) $T = 165\,^\circ\text{C}$; $f$ is spaced logarithmically between $5\times10^{-4}$ and 1 Hz. Since the originally extracted $D_\text{ot}$ is given in $\text{cm}^{-3}/\text{V}$, we recalculated the gate voltage into the trap level $E_\text{T}$ (top right plot) by considering the band-bending within 3 nm from the interface [9]. We can clearly discern the regions with dominating hole capture and emission. Both processes become more effecient for smaller $f$, while emission is more sensitive to $f$ than capture, i.e. the emission times are more widely distributed. Also, at higher temperature the impact of $f$ becomes more pronounced, which is consistent with thermal activation. (c) The energy distributions of slow oxide traps ($f = 5\times10^{-4}\,\text{Hz}$) obtained for different temperatures. Due to thermal activation, the trap density becomes larger for higher temperatures, while the positions of the spikes on the $D_\text{ot}(E)$ curves remain fixed.

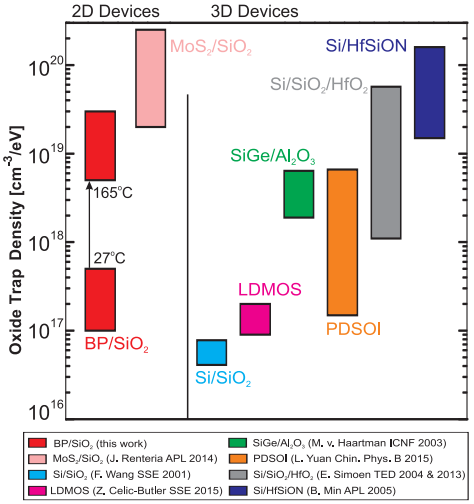


**Fig. 6:** Comparison of typical $D_\text{ot}$ values for our BPFETs with literature reports for different technologies [10–17]. At room temperature the obtained densities of active oxide traps can be $\sim10^{17}\,\text{cm}^{-3}/\text{eV}$. This is lower than in $MoS_2/SiO_2$ and Si/high-k FETs, while being close to $Si/SiO_2$ devices. Taking into account the novelty of BP and recent issues with its stability, we found these values to be unexpectedly low. Nevertheless, thermal activation of oxide traps presents a crucial issue for BPFETs.