Reliability of Black Phosphorus Field-Effect Transistors with Respect to Bias-Temperature and Hot-Carrier Stress

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***Abstract*—We perform a detailed study of bias-temperature instabilities and hot-carrier degradation in highly-stable black phosphorus field-effect transistors and attempt to capture the correlation between these phenomena. We demonstrate that a hot-carrier stress applied in conjunction with a bias stress leads neither to a considerably stronger degradation nor to dramatically different recovery dynamics, which is in contrast to graphene devices and Si technologies. This allows us to conclude that the BP/SiO_2 system is a significant step forward in terms of the reliability improvement of next-generation 2D devices.**

I. Introduction

Black phosphorus (BP) is a crystalline 2D semiconductor which is now considered for applications in next-generation electronic devices [1–3]. Contrary to graphene [4, 5], BP has a sizable direct bandgap ranging from 0.3 eV in bulk to over 1 eV in the monolayer limit [1, 6], which makes this material interesting for digital electronics. Also, unlike MoS_2, BP exhibits a comparatively high mobility (up to 1000 cm^2/Vs) for both electrons [7] and holes [3]. As such, BP can be considered a promising channel material for both n- and p-FETs, as required for integrated CMOS circuits. Furthermore, p-FETs with BP channel can be potentially interesting for CMOS circuits with MoS_2 n-FETs [8–10]. All these possibilities are essential in the context of the recently demonstrated epitaxial synthesis of monolayer phosphorene, which represents a breakthrough for very large scale integration [11].

By now, several groups have succeded at fabricating black phosphorus field-effect transistors (BPFETs) [1, 3, 12–14]. However, so far the poor air-stability of these devices did not allow any long-term analysis of their reliability. These studies have only become possible now due to the recent introduction of conformal capping schemes [14, 15]. In particular, in our previous work [16] we have demonstrated that the time interval of stability of BPFETs encapsulated with Al_2O_3 can be at least eight months. This allowed us to perform the first long-term study of the hysteresis and bias-temperature instabilities (BTI) in these devices [16]. However, the question of hot-carrier degradation (HCD) in BPFETs has not been discussed in the literature so far. Since HCD typically occurs in conjunction with BTI, we perform here a detailed study of both phenomena and attempt to capture the correlation between them, while paying attention to the reproducibility of the measured results. An important point is that this study is performed nearly a year after the fabrication of our devices, which is considerably larger than previously reported time intervals of BPFETs stability [14, 17–19].

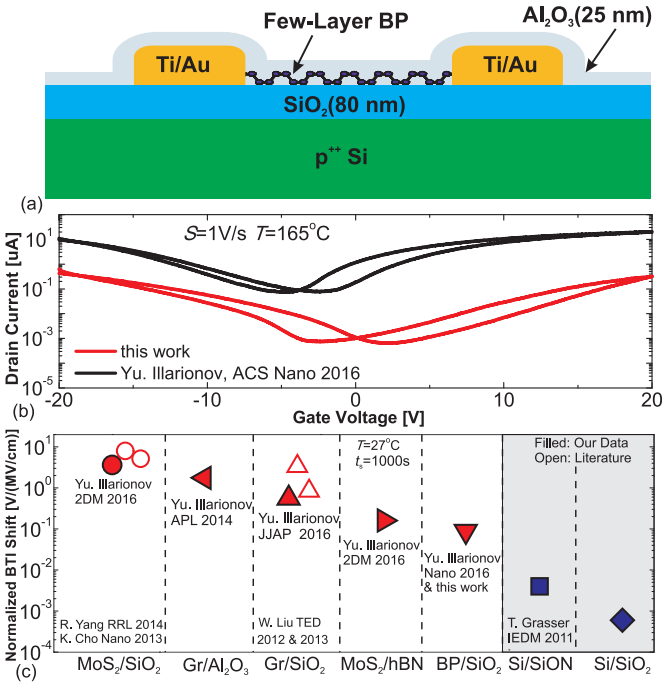

Fig. 1: (a) Schematic layout of our encapsulated BPFETs with $L = 500$ nm. (b) A device with thinner BP layer and better I_{off} performance is examined. (c) At room temperature the BP/SiO_2 system exhibits the best BTI reliability among all 2D systems investigated so far.

II. Devices

We examine few-layer BPFETs with 80 nm thick SiO_2 as a gate insulator, source/drain contacts made of Ti/Au and a channel length $L = 500$ nm (Fig. 1a). In order to prevent severe degradation of BP films in ambient air [14, 15, 20], our devices have been conformally encapsulated with a 25 nm thick Al_2O_3 layer. In contrast to our previous work [16], for this study we select devices with thinner BP channel (likely below 10 nm) which exhibit a better I_{off} performance (Fig. 1b). By comparing the measured BTI shifts normalized by the oxide field for different 2D systems [21–26], we found that the BP/SiO_2

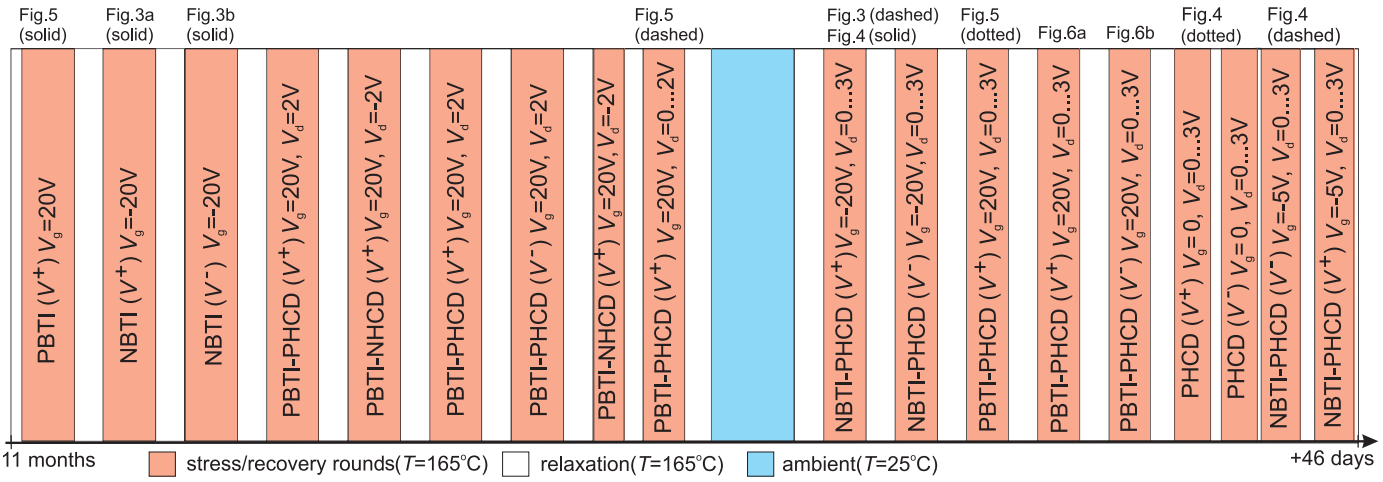

Fig. 2: Schematic timing of our long-term study which was started 11 months after device fabrication. Subsequent BTI and HCD stress/recovery rounds are followed by up to one day long intervals of complete relaxation (no measurements). PHCD and NHCD express positive ($V_d > 0$) and negative ($V_d < 0$) HCD, respectively. The obtained results are shown in the figures below as marked on top.

system is the most stable with respect to room-temperature BTI among other 2D systems, although the observed shifts are still considerably larger than for Si technologies [27] (Fig. 1c). While the previously reported time intervals of BPFET stability rarely exceed few weeks [14, 17–19], the total time since fabrication of our devices till the end of this study is over one year.

III. Experiment

In order to verify the stability of our BPFETs under severe stress conditions, we performed the measurements at $T = 165$°C in a vacuum ($\sim 5\times10^{-6}$ torr). In the spirit of our works for graphene FETs (GFETs) [25, 28], the BTI and HCD dynamics have been studied using measurement loops with subsequent stress/recovery rounds with either constant drain voltage V_d and increasing stress time t_s or constant t_s and increasing V_d; the gate voltage V_g during the stress was constant for each measurement loop. The gate transfer (I_d-V_g) charateristics have been measured at each recovery stage corresponding to a certain relaxation time t_r using either a forward (V^+) or reversed (V^-) sweep direction. While the device operation range corresponds to V_g from -20 to 20 V, the typical measurement delay due to an I_d-V_g sweep rate $S = 20$ V/s was about two seconds. Since at $T = 165$°C the charge neutrality point V_{NP} can be identified reliably, we express the degradation magnitude in terms of the charge neutrality point shift ΔV_{NP}. Schematic timing of our long-term reliability study is shown in Fig. 2. In addition to positive and negative BTI (PBTI and NBTI, respectively), we introduce positive HCD (PHCD, $V_d > 0$) and negative HCD (NHCD, $V_d < 0$) and analyze the degradation/recovery dynamics for various reliability issues which correspond to either pure BTI ($V_d = 0$), pure HCD ($V_g = 0$) or BTI and HCD acting in conjunction (both V_d and V_g are non-zero). Each of the measurement loops corresponding to a particular reliability issue has been followed by up to one day of relaxation, which, contrary to Si technologies, was sufficient to achieve complete recovery and make the results reproducible. Also, in order to analyze the impact of the ambient on the reliability characteristics, the device was once removed from vacuum and stored at room temperature under ambient conditions for three days. Afterwards, the experiments were continued, see Fig. 2.

IV. Results and Discussions

In Fig. 3 we show the results for pure NBTI obtained using the V^+ and V^- sweep modes. In agreement with our previous results for GFETs [25] and thicker BPFETs [16], the V_{NP} shifts measured using the V^- sweep mode are considerably smaller. This is because in the case of the V^- sweep mode the faster component of NBTI is strongly compensated by PBTI degradation which occurs while sweeping from 20 V towards V_{NP}. Conversely, the use of the V^+ sweep mode allows us to conserve the NBTI shift accumulated during the stress, since no PBTI degradation takes place between -20 V and V_{NP}. At the same time, three weeks of intensive stressing followed by an exposure of the device to the ambient leads to an only insignificant increase of the degradation level, while almost not affecting the transfer characteristic measured at the beginning of the measurement loop, i.e. for the relatively fresh device. This strongly confirms the high stability of our BPFETs with respect to both the electrical stress and the detrimental impact of the environment. In Fig. 4 we compare the results obtained after NBTI ($V_d = 0$), PHCD ($V_g = 0$, $V_d > 0$) and NBTI-PHCD ($V_g = -20$ V and -5 V, $V_d > 0$) stresses with different V_d and $t_s = 10$ ks for both sweep modes. Similarly to GFETs [28, 29], pure PHCD stress leads to an NBTI-like shift of V_{NP} and supplements NBTI degradation. However, we observe that in BPFETs the impact of PHCD on the NBTI shift is small, while in GFETs PHCD considerably accelerates NBTI degradation [28, 29]. We argue that in both BPFETs and GFETs NBTI and PHCD are of a similar nature due to a reduced number of dangling bonds from the channel side. Namely, both issues lead to hole capture by preexisting oxide defects. The only difference is that in the case of NBTI the distribution of the defects which have changed their charge state after the stress is homogeneous, while for PHCD it has a maximum

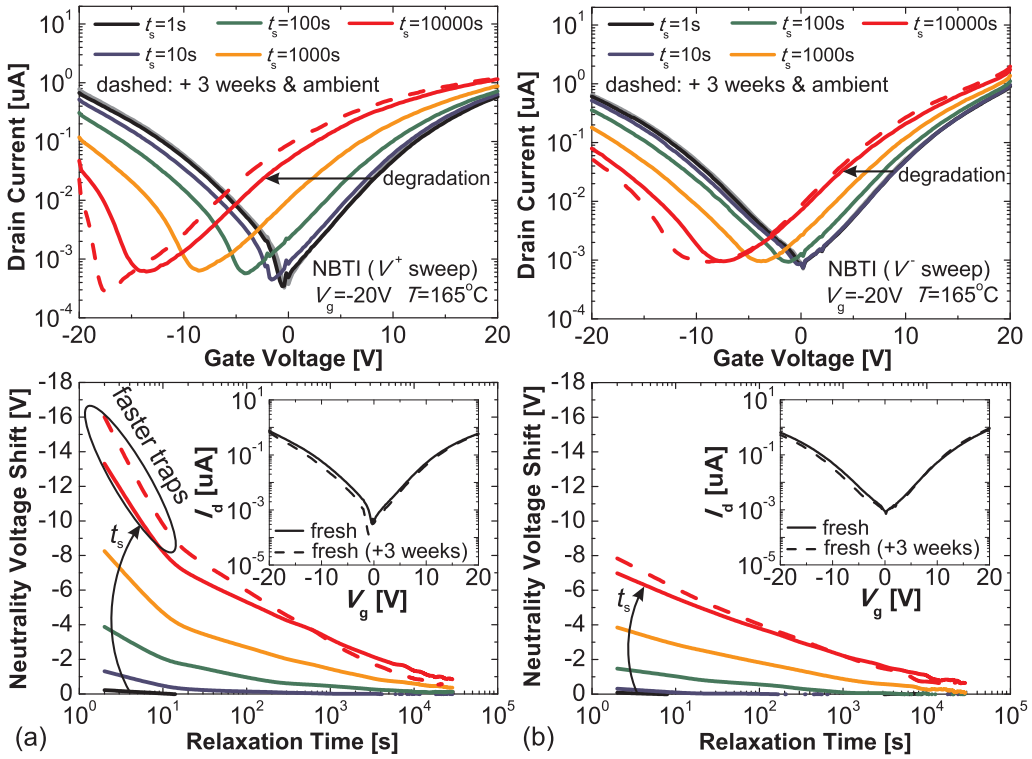

Fig. 3: Evolution of the I_d-V_g characteristics of our BPFETs after subsequent NBTI stresses with increasing stress times (top) and the corresponding recovery traces for the charge neutrality voltage shift (bottom). (a) V^+ sweep. (b) V^- sweep. While the observed shifts are larger when the V^+ sweep is used, intensive stressing of the device during three weeks followed by several days of exposure to the ambient leads to an only insignificant increase of NBTI. At the same time, the transfer characteristics of a relatively fresh device which have been used as a reference are nicely reproducible for both sweep directions (insets), which confirms the absence of any significant residual degradation from previous stress rounds and further underlines the stability of our devices.

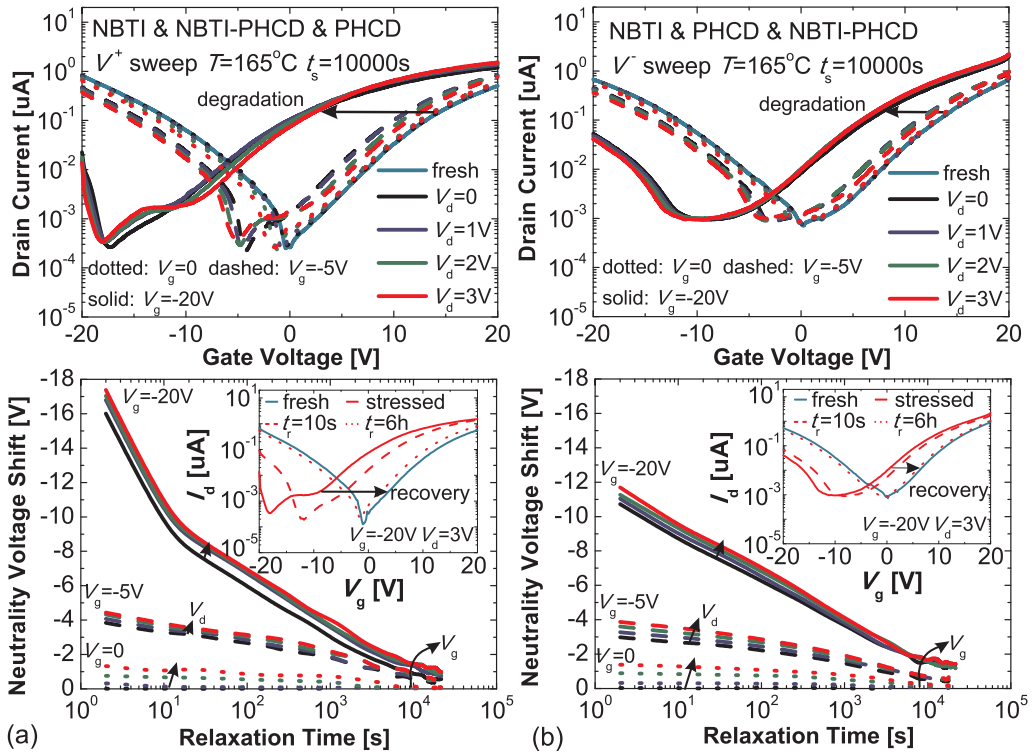

Fig. 4: Evolution of the I_d-V_g characteristics of our BPFETs after subsequent NBTI (V_d = 0), PHCD (V_g = 0) and NBTI-PHCD (V_g = −5 V and −20 V) stresses with increasing V_d (top) and the corresponding recovery traces for the V_{NP} shift (bottom). (a) V^+ sweep. (b) V^- sweep. PHCD leads to an insignificant NBTI-like degradation and thus slightly supplements NBTI. Similarly to NBTI, NBTI-PHCD contains some faster component which is suppressed if the V^- sweep mode is used. In addition to a strongly recoverable V_{NP} shift, an essential feature of this faster component is the transformation of the shape of the transfer characteristics. While being strongly recoverable (inset), this issue is more pronounced at larger V_g and V_d.

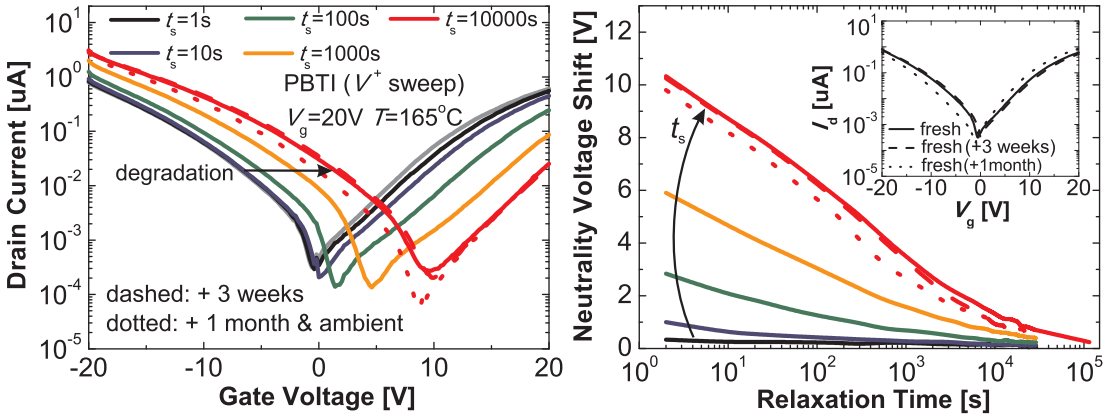

Fig. 5: Evolution of the I_d-V_g characteristics of our BPFETs after subsequent PBTI stresses with increasing stress times (left) and the corresponding recovery traces for the V_{NP} shift (right). While intensive stress/recovery measurements during three weeks do not affect the degradation magnitude and recovery dynamics, exposure to the ambient for several days slightly reduces the observed PBTI shift.

near the drain. As such, a reduction of PHCD in BPFETs fully agrees with a considerably better BTI reliability of BP/SiO_2 system compared to its Gr/Al_2O_3 counterpart (Fig. 1c) studied in Refs. [28, 29]. At the same time, NBTI-PHCD contains a strongly recoverable component associated with faster oxide traps, which is similar to NBTI and becomes more pronounced at larger V_g. While being suppressed when using the V^- sweep mode, this faster component impacts both the observed V_{NP} shifts and the shape of the transfer characteristics in the electron conduction region. The latter is definitely associated with the defects which are not accessible under the pure NBTI stress condition and can be activated only at the presence of the PHCD contribution. At larger V_g and V_d the number of accessible defects increases, which leads to a more severe transformation of the shape of the I_d-V_g characteristic. Since these additionally activated defects are extremely fast, we suggest that they could be interface traps located either at the BP/SiO_2 interface or at the interface between the BP channel and Al_2O_3 encapsulation layer. In addition, we notice that even pure HCD is nearly completely recoverable, while the degree of recovery is almost independent of the magnitude of PHCD contribution. This is in contrast to Si technologies, where the major contribution to HCD is typically associated with dangling bonds at the channel/oxide interface [30, 31], thus making the degradation weakly recoverable.

In Fig. 5 we show the results obtained for pure PBTI using the V^+ sweep mode and different stress times. Similarly to GFETs [28, 29], PBTI in BPFETs is due to electron capture, which leads to an opposite direction of V_{NP} drift compared to NBTI. At the same time, just like for NBTI, the recovery traces are well reproducible after three weeks of intensive measurements, while subsequent exposure of the device in the ambient slightly reduces the measured ΔV_{NP}. Nevertheless, in all cases PBTI is almost completely recoverable, while the device exhibits a high stability with respect to the bias stress, temperature and environment. In Fig. 6 we proceed with the analysis of PBTI-PHCD for both sweep directions. Contrary to the case of NBTI-PHCD, here the faster component is conserved when using the V^- sweep mode, since no NBTI degradation can take place while sweeping from 20 V to V_{NP}. While this faster component is considerably smaller than for NBTI-PHCD, PHCD with larger V_d leads to its partial compensation. This agrees with the results of Fig. 4 showing that PHCD in BPFETs, just like for GFETs [28, 29], is of NBTI-like nature. Furthermore, we observe some transformation of the shape of the I_d-V_g characteristics, which presents another fingerprint of a PHCD contribution. Nevertheless, there is no significant impact of PHCD on the slower component of PBTI, i.e. the issue is compensated by strong PBTI degradation. This is in contrast to GFETs, where the NBTI-like PHCD contribution can be strong enough to considerably compensate the PBTI degradation, while the recovery dynamics of PBTI-PHCD is non-trivial [28, 29].

In Fig. 7a we summarize the V_d dependences of V_{NP} shifts measured at $t_r = 2$ s for different V_g and using both sweep directions. The most essential findings are the following. First, the NBTI and NBTI-PHCD shifts contain the faster component if the measurements are performed using the V^+ sweep mode, while for their PBTI and PBTI-PHCD counterparts this is the case for the V^- sweep mode. This observation confirms that the time constants of the involved defects are widely distributed. Namely, if the bias condition is favourable, a considerable number of faster traps are able to recover during the first post-stress I_d-V_g sweep, while the slower ones remain perturbed for several hours/days. Second, for larger V_g the faster component is considerably larger, while being negligible for pure PHCD. Thus, the faster defects follow the variations of Fermi level determined by V_g, as well as their slower counterparts. Finally, we notice that pure PHCD in BPFETs shifts V_{NP} in the same manner as NBTI, although the observed shifts are considerably smaller. As such, in most cases non-zero V_d during stress leads to some increase of NBTI and decrease of PBTI shifts. In Fig. 7b we show the dependences of the relative degradation level remaining after $t_r = 5$ h versus V_d. The permanent component does not exceed 15% of the initially measured ΔV_{NP} even for the most severe stresses with $V_g = \pm 20$ V. At the same time, an increase versus V_d is observed only for those sweep modes which allow to measure the full ΔV_{NP}, including the faster component. In contrast, for the cases where the faster component is suppressed, the

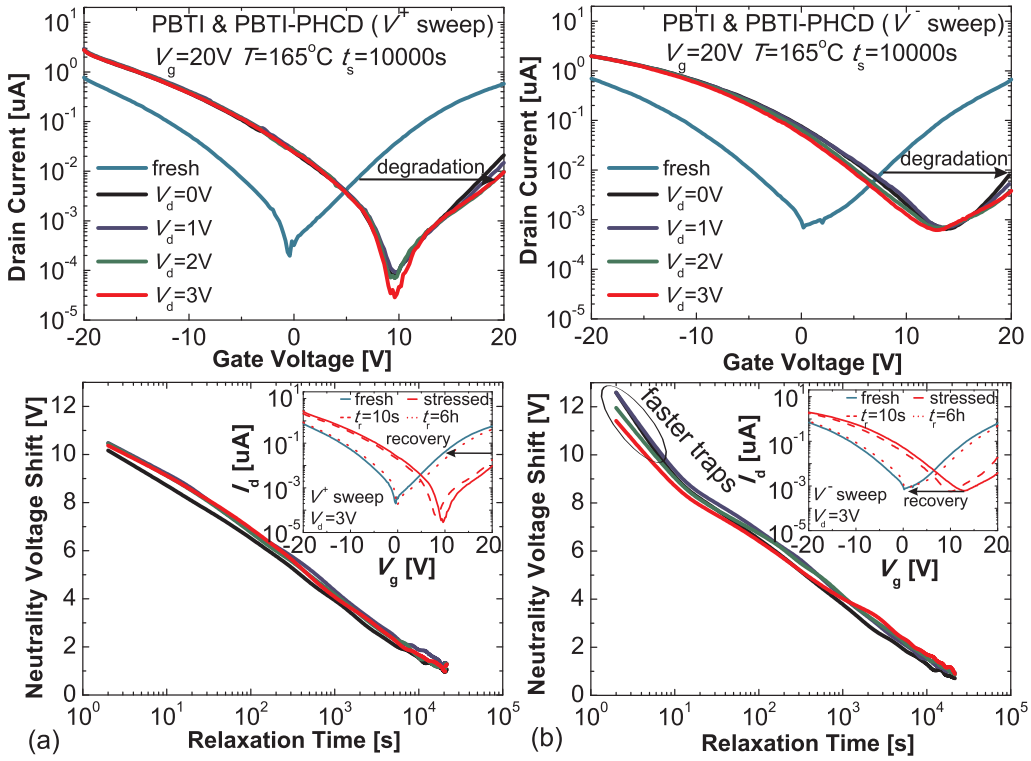

Fig. 6: Evolution of the I_d-V_g characteristics of our BPFETs after subsequent PBTI ($V_d = 0$) and PBTI-PHCD stresses with increasing V_d (top) and the corresponding recovery traces (bottom). (a) V^+ sweep. (b) V^- sweep. In contrast to NBTI-PHCD, the faster component of the degradation is observed when using the V^- sweep mode. While being reduced by PHCD, this faster component is small compared to the case of NBTI-PHCD. As for the slower component, it is weakly dependent on the magnitude of PHCD, which means that in general a small NBTI-like impact of PHCD is compensated by PBTI degradation. At the same time, after PBTI-PHCD stresses with larger V_d the shape of the electron conduction region of the I_d-V_g characteristic is modified. However, this issue is strongly recoverable (insets).

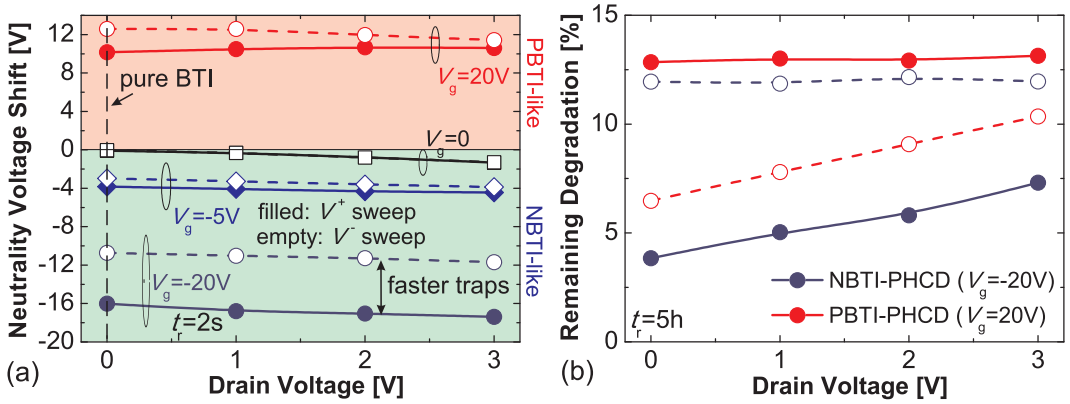

Fig. 7: (a) The V_{NP} shifts measured for different degradation issues at $t_r = 2$s. NBTI-PHCD and PBTI-PHCD contain faster components in V^+ and V^- sweep modes, respectively. At larger V_g, PHCD reduces the faster component of PBTI and supplements those of NBTI. (b) The relative degradation remaining after $t_r = 5$h increases versus V_d only for those sweep modes which conserve the faster component.

relative slower component is almost independent of V_d, while being considerably larger. This further confirms that in contrast to GFETs, in our BPFETs the PHCD contribution mostly affects the faster component of BTI rather than the more permanent one.

V. Conclusions

We have demonstrated that our BPFETs remain stable for at least one year, while conserving their main properties even under intensive bias and hot-carrier stressing at high temperature, as well as under ambient conditions. This allowed us to perform a first combined study of BTI and HCD on BPFETs and capture the correlation between these phenomena. Our results show that the hot-carrier stress applied in conjunction with BTI leads neither to a considerably stronger degradation nor to dramatically different recovery dynamics, which is in contrast to GFETs and Si technologies. Together with a better BTI stability, this allows us to conclude that the BP/SiO_2 system presents a significant step forward in terms of reliability improvement of next-generation 2D devices.

VI. Acknowledgements

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References

[1] H. Liu, A. Neal, Z. Zhu, Z. Luo, X. Xu, D. Tomanek, and P. Ye, "Phosphorene: An Unexplored 2D Semiconductor with a High Hole Mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, 2014.

[2] Q. Wei and X. Peng, "Superior Mechanical Flexibility of Phosphorene and Few-Layer Black Phosphorus," *Applied Physics Letters*, vol. 104, no. 25, p. 251915, 2014.

[3] L. Li, Y. Yu, G. Ye, Q. Ge, X. Ou, H. Wu, D. Feng, X. Chen, and Y. Zhang, "Black Phosphorus Field-Effect Transistors," *Nature Nanotechnology*, vol. 9, pp. 372–377, 2014.

[4] K. Novoselov, A. Geim, S. Morozov, D. Jiang, Y. Zhang, S. Dubonos, I. Grigorieva, and A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.

[5] A. Geim and K. Novoselov, "The Rise of Graphene," *Nature Materials*, vol. 6, no. 3, pp. 183–191, 2007.

[6] H. Liu, Y. Du, Y. Deng, and D. Peide, "Semiconducting Black Phosphorus: Synthesis, Transport Properties and Electronic Applications," *Chemical Society Reviews*, vol. 44, no. 9, pp. 2732–2743, 2014.

[7] D. J. Perello, S. H. Chae, S. Song, and Y. H. Lee, "High-Performance n-Type Black Phosphorus Transistors with Type Control via Thickness and Contact-Metal Engineering," *Nature Communications*, vol. 6, 2015.

[8] B. Radisavljevic, A. Radenovic, J. Berivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nature Nanotechnology*, vol. 6, pp. 147–150, 2011.

[9] Y. Yoon, K. Ganapathi, and S. Salahuddin, "How Good Can Monolayer MoS_2 Transistors Be?" *Nano Letters*, vol. 11, pp. 3768–3773, 2011.

[10] J. Kang, W. Liu, and K. Banerjee, "High-performance MoS_2 Transistors with Low Resistance Molybdenum Contacts," *Applied Physics Letters*, vol. 104, p. 093106, 2014.

[11] J. Zhang, S. Zhao, C. Han, Z. Wang, S. Zhong, S. Sun, R. Guo, X. Zhou, C. Gu, K. Yuan, Z. Li, and W. Chen, "Epitaxial Growth of Single Layer Blue Phosphorus: A New Phase of Two-Dimensional Phosphorus," *Nano Letters*, vol. 16, no. 8, pp. 4903–4908, 2016.

[12] S. Das, M. Demarteau, and A. Roelofs, "Ambipolar Phosphorene Field Effect Transistor," *ACS Nano*, vol. 8, no. 11, pp. 11 730–11 738, 2014.

[13] H. Liu, A. Neal, Z. Zhu, D. Tomanek, and P. Ye, "Phosphorene: a New 2D Material With High Carrier Mobility," *arXiv*, p. 1401.4133, 2014.

[14] J.-S. Kim, Y. Liu, W. Zhu, S. Kim, D. Wu, L. Tao, A. Dodabalapur, K. Lai, and D. Akinwande, "Toward Air-Stable Multilayer Phosphorene Thin-Films and Transistors," *Scientific Reports*, vol. 5, pp. 1–7, 2015.

[15] J. Wood, S. Wells, D. Jariwala, K.-S. Chen, E. Cho, V. Sangwan, X. Liu, L. Lauhon, T. Marks, and M. Hersam, "Effective Passivation of Exfoliated Black Phosphorus Transistors against Ambient Degradation," *Nano Letters*, vol. 14, no. 12, pp. 6964–6970, 2014.

[16] Y. Illarionov, M. Waltl, G. Rzepa, J.-S. Kim, S. Kim, A. Dodabalapur, D. Akinwande, and T. Grasser, "Long-term Stability and Reliability of Black Phosphorus Field-Effect Transistors," *ACS Nano*, vol. 10, no. 10, pp. 9543–9549, 2016.

[17] N. Gillgren, D. Wickramaratne, Y. Shi, T. Espiritu, J. Yang, J. Hu, J. Wei, X. Liu, Z. Mao, K. Watanabe, T. Taniguchi, M. Bockrath, Y. Barlas, R. Lake, and C. Lau, "Gate Tunable Quantum Oscillations in Air-Stable and High Mobility Few-Layer Phosphorene Heterostructures," *2D Materials*, vol. 2, no. 1, p. 011001, 2014.

[18] J. Na, Y. Lee, J. Lim, D. Hwang, G.-T. Kim, W. Choi, and Y.-W. Song, "Few-layer Black Phosphorus Field-Effect Transistors with Reduced Current Fluctuation," *ACS Nano*, vol. 8, no. 11, pp. 11 753–11 762, 2014.

[19] X. Chen, Y. Wu, Z. Wu, Y. Han, S. Xu, L. Wang, W. Ye, T. Han, Y. He, Y. Cai, and N. Wang, "High-Quality Sandwiched Black Phosphorus Heterostructure and its Quantum Oscillations," *Nature Communications*, vol. 6, 2015.

[20] A. Favron, E. Gaufres, F. Fossard, A. Phaneuf-L'Heureux, N. Tang, P. Levesque, A. Loiseau, R. Leonelli, S. Francoeur, and R. Martel, "Photooxidation and Quantum Confinement Effects in Exfoliated Black Phosphorus," *Nature Materials*, vol. 14, no. 8, pp. 826–832, 2015.

[21] W. Liu, X. Sun, Z. Fang, Z. Wang, X. Tran, F. Wang, L. Wu, G. Ng, J. Zhang, J. Wei, H. Zhu, and H. Yu, "Positive Bias-Induced V_{th} Instability in Graphene Field Effect Transistors," *IEEE Electron Device Letters*, vol. 33, no. 3, pp. 339–341, 2012.

[22] W. Liu, X. Sun, X. Tran, Z. Fang, Z. Wang, F. Wang, L. Wu, J. Zhang, J. Wei, H. Zhu, and H. Yu, "Observation of the Ambient Effect in BTI Characteristics of Back-Gated Single Layer Graphene Field Effect Transistors," *IEEE Transactions on Electron Devices*, vol. 60, no. 8, pp. 2682–2686, 2013.

[23] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, and T. Lee, "Electric Stress-Induced Threshold Voltage Instability of Multilayer MoS_2 Field Effect Transistors," *ACS Nano*, vol. 7, pp. 7751–7758, 2013.

[24] S. Yang, S. Park, S. Jang, H. Kim, and J.-Y. Kwon, "Electrical Stability of Multilayer MoS_2 Field-Effect Transistor under Negative Bias Stress at Various Temperatures," *Physica Status Solidi*, vol. 8, pp. 714–718, 2014.

[25] Y. Illarionov, A. Smith, S. Vaziri, M. Ostling, T. Mueller, M. Lemme, and T. Grasser, "Bias-Temperature Instability in Single-Layer Graphene Field-Effect Transistors," *Applied Physics Letters*, vol. 105, no. 14, p. 143507, 2014.

[26] Y. Illarionov, M. Waltl, A. Smith, S. Vaziri, M. Ostling, M. Lemme, and T. Grasser, "Bias-Temperature Instability on the Back Gate of Single-Layer Double-Gated Graphene Field-Effect Transistors," *Japanese Journal of Applied Physics*, vol. 55, no. 4S, p. 04EP03, 2016.

[27] T. Grasser, P.-J. Wagner, H. Reisinger, T. Aichinger, G. Pobegen, M. Nelhiebel, and B. Kaczer, "Analytic Modeling of the Bias Temperature Instability Using Capture/Emission Time Maps," in *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2011, pp. 27.4.1–27.4.4.

[28] Y. Illarionov, M. Waltl, A. Smith, S. Vaziri, M. Ostling, M. Lemme, and T. Grasser, "Interplay between Hot Carrier and Bias Stress Components in Single-Layer Double-Gated Graphene Field-Effect Transistors," in *European Solid State Device Research Conference (ESSDERC)*, 2015, pp. 172–175.

[29] Y. Illarionov, A. Smith, S. Vaziri, M. Ostling, T. Mueller, M. Lemme, and T. Grasser, "Hot-Carrier Degradation and Bias-Temperature Instability in Single-Layer Graphene Field-Effect Transistors: Similarities and Differences," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3876–3881, 2015.

[30] O. Penzin, A. Haggag, W. McMahon, E. Lyumkis, and K. Hess, "MOSFET Degradation Kinetics and its Simulation," *IEEE Transactions on Electron Devices*, vol. 50, no. 6, pp. 1445–1450, 2003.

[31] S. Tyaginov, I. Starkov, O. Triebl, J. Cervenka, C. Jungemann, S. Carniello, J. Park, H. Enichlmair, M. Karner, C. Kernstock, E. Seebacher, R. Minixhofer, H. Ceric, and T. Grasser, "Interface Traps Density-of-States as a Vital Component for Hot-Carrier Degradation Modeling," *Microelectronics Reliability*, vol. 50, no. 9, pp. 1267–1272, 2010.