## Encapsulated MoS<sub>2</sub> FETs with Improved Performance and Reliability

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Considerable progress in the fabrication of  $MoS_2$  FETs has been demonstrated recently [1]. However, available device prototypes still suffer from a sizable hysteresis of the  $I_D$ - $V_G$  characteristics [2,3] and long-term drifts of threshold voltage  $V_{th}$  [3,4], known as bias-temperature instabilities (BTI). As such, these issues must be addressed prior to commercialization of  $MoS_2$  technologies.

Here we report on the improvement of the properties of  $MoS_2/SiO_2(25 \text{ nm})$  FETs [5] introduced by the encapsulation with high-quality  $Al_2O_3(15 \text{ nm})$  based on a modified recipe of [6]. The  $I_{on}/I_{off}$  ratio of these devices is as high as  $10^9$  (Fig.1a), which is already close to predicted values [7]. At the same time, the hysteresis is two orders of magnitude smaller than in bare exfoliated devices (Fig.1b). Furthermore, positive BTI (PBTI) in encapsulated CVD devices is weakly pronounced (Fig.1c), which is important for  $MoS_2$  n-FETs. Quite remarkably, PBTI is weaker than in previously reported exfoliated bare  $MoS_2/SiO_2$  [3], stacked  $MoS_2/hBN$  [3] and encapsulated  $BP/SiO_2$  FETs [8] (Fig.1d). The reason for the reduced hysteresis and BTI, as well as for the improved device perfromance, is that the encapsulation layer efficiently protects the device from adsorbent-type trapping sites on top of the  $MoS_2$  channel [3].

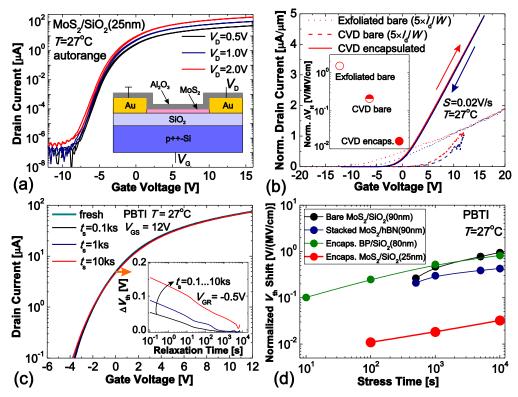


Fig. 1. (a) The  $I_{\rm D}$ - $V_{\rm G}$  characteristics of encapsulated MoS $_2$  FETs and schematic device layout (inset). (b) The  $I_{\rm D}$ - $V_{\rm G}$  characteristics (normalized by device width W) of exfoliated bare MoS $_2$ /SiO $_2$ (90 nm) and CVD grown bare and encapsulated MoS $_2$ /SiO $_2$ (25 nm) FETs (sweep rate S=0.02 V/s). (c) Evolution of the  $I_{\rm D}$ - $V_{\rm G}$  characteristics after subsequent PBTI stresses with  $V_{\rm GS}$ =12 V and  $V_{\rm th}$  recovery traces measured using  $V_{\rm GR}$ =-0.5 V (inset). (d) The PBTI shifts normalized by the stress oxide field are the smallest for encapsulated CVD grown MoS $_2$ /SiO $_2$ (25 nm) FETs.

Overall, we conclude that encapsulation of MoS<sub>2</sub> FETs strongly improves their reliability and performance, making this an important technological step toward reaching commercial quality standards. [1] P. Bolshakov *et al*, Microelectron. Eng., **178** (2017) 190. [2] Y. Guo *et al*, Appl. Phys. Lett., **108** (2015) 103109. [3] Yu.Yu. Illarionov *et al*, 2D Mater., **3** (2016) 035004. [4] K. Cho *et al*, ACS Nano, **7** (2013) 7751. [5] K.K.H. Smithe *et al*, 2D Mater., **4** (2017) 011009. [6] M.J. Mleczko *et al*, ACS Nano, **10** (2016) 7507. [7] Y.

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