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(Invited) Impact of Gate Dielectrics on the Threshold Voltage in MoS_2 Transistors

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Abstract

Introduction

MoS_2 is a next-generation 2D material which is considered for applications in digital electronics [1–3]. Although enormous progress has been made in the area of MoS_2 FETs, the available prototypes do not yet meet the high expectations. Commonly known reliability issues like the frequently observed hysteresis in the $I_D(V_G)$ characteristics [4–6] and the large drifts of the threshold voltage over time [7] prohibit stable device operation for this technology. Apart from fabrication related issues, these performance limiting issues are the most critical obstacles inhibiting industrial applications of MoS_2 FETs. Complementing our previous works [7–9], here we present a physical modeling approach for studying the charging and discharging of preexisting defects in the surrounding dielectrics.

Devices

We compare the hysteresis widths measured at the gates of MoS_2 based FET devices at different sweep frequencies. Additionally, we study the drifts of the threshold voltage on these devices in a systematic way by evaluating the threshold voltage shifts observed after stressing the devices for different time spans and stress voltages. From the wide range of samples available, we choose devices using a thermal SiO_2 layer as a back-gate dielectric. The MoS_2 is either exposed to the ambient or covered by an amorphous Al_2O_3 layer. This thin dielectric layer enables a top gate contact and is at the same time necessary to prevent any degradation of the device characteristics due to the impact of the ambient [4,8].

Degradation Modeling

For simulating the transfer characteristics we use a TCAD device simulator solving the drift-diffusion equations [10]. This approach is valid for devices with large dimensions and a large number of scattering centers, even if 2D channel materials are used [11]. The impact of interface defects is considered by using the standard SRH model. The transient charging and discharging of oxide defects leading to the hysteresis and the long-term drifts of the threshold voltage are described using the four-state NMP model [12,13]. The physical defect properties determining the degradation, such as trap positions and energy levels, depend on the respective oxide and have been studied in detail for SiO_2 [8,14] and Al_2O_3 [9].

Results

In accordance with our previous experimental work [7], we argue here that the common cause for the hysteresis in the $I_D(V_G)$ and the observed long-term drifts are charge capture and emission events in the surrounding dielectrics. Even though several groups claim that the hysteresis is due to charge trapping at the interface [6,15,16], we argue here that interface traps can only impact the threshold voltage via a change in the sub-threshold slope. An observed hysteresis provides information about fast-switching oxide traps, while the systematic stress measurements reveal details about slow-switching oxide traps. One important quantity, necessary for understanding the size of the observed threshold voltage shifts, is the band alignment of the defect bands in the dielectrics with respect to the band edges of the semiconductors, illustrated in Fig. 1.

Conclusions

We use a drift-diffusion based simulation methodology to describe the cause of the threshold voltage drifts observed in the $I_D(V_G)$ characteristics of MoS_2 FETs, namely the charge capture and emission processes in the gate oxide traps. Thus, it is of utmost importance not only to investigate the fabrication of 2D layers, but also to focus on the quality and the defect bands of amorphous dielectrics to enable further progress in the area of FETs based on 2D materials.

Acknowledgments

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Fig. 1: Band alignment of defect bands in Al_2O_3 and SiO_2.

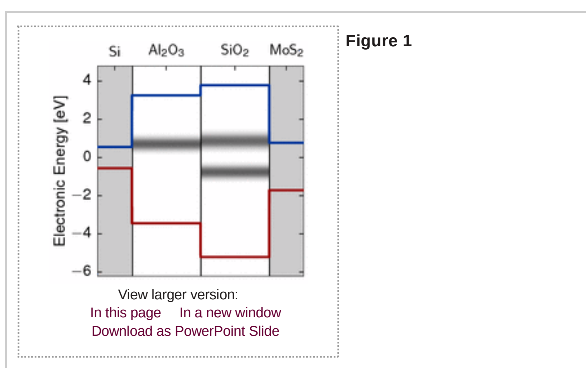

Figure 1

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