Vertically Stacked Nanowire MOSFETs for Sub-10 nm Nodes: Advanced Topography, Device, Variability, and Reliability Simulations

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***Abstract*—Using an advanced simulation framework we analyze a recent sub-10 nm technology demonstration based on stacked nanowire transistors (NW-FETs). The study encompasses (i) topography simulation which realistically reproduces the fabricated device, (ii) device simulation based on the subband Boltzmann transport equation (iii) a comprehensive set of scattering models for the gate stack, (iv) physical models for time-zero variability and BTI device degradation. We find that (i) the fabrication process introduces parasitic capacitances not present in a comparable FinFET, (ii) the device performance is significantly affected by interface-charge-induced Coulomb scattering resulting in up to 50% reduction in drain current compared to an ideal device, (iii) device time-zero variability is increased due to a lower amount of dopant atoms per device, (iv) the device is more affected by BTI than a comparable FinFET. Using physics-based TCAD for technology path-finding and device optimization, we are able to point out critical improvements required for the stacked NW-FET to surpass current FinFET technology.**

I. Introduction

Gate-all-around (GAA) architectures are considered the ultimate refinement of the classical MOSFET, and are likely candidates for CMOS scaling beyond the 10 nm node. A GAA imposes perfect electrostatic control upon the device's channel, allowing for a sub-threshold slope close to the theoretical minimum. However, the main concern is to attain an on-current large enough for applications. In recent work [1], this concern has been addressed by demonstrating a GAA FET with two vertically stacked nanowires as its channels, sharing a common gate, effectively doubling the on-current w.r.t. a single wire.

This work investigates the proposed architecture using a comprehensive framework of advanced simulators to assess the fabrication process and the resulting device characteristics, performance, variability, and reliability.

II. Device Topography

Due to its two isolated wires the proposed device features a more complex topography than any other comparable device. We use *process emulation* to generate a realistic representation of the device geometry. At its core, process emulation is physics-agnostic: etching, deposition, and epitaxial growth are modeled using rates, which can be made selective w.r.t. the surface material or orientation. The rate can be spatially controlled using *masks*, which are used in similar fashion to lithography masks. Masks can be loaded from GDSII files and combined using boolean operations. The computational foundation of our process emulator *ProEmu* [2] is the *level-set* method [3, 4].

The fabrication process of the stacked nanowire transistor is described in [1]. The process is reproduced in ProEmu, as illustrated by Fig. 1. The final structure is shown in Fig. 2 along with the doping profile. One peculiarity of the process is an effective *under-etching* of the spacer; since the spacer is formed before the nanowire release, the gate protrudes into the spacer region between the wires as shown in Fig. 3. The thin dielectric layer between gate and source/drain forms considerable parasitic capacitances.

Adjustment of the rates in the $Si_{1-x}Ge_x$ etch process gives two circular shaped cross-sections in the middle of the channel. However, the wire cross-section towards the access regions loses its circular shape and becomes rectangular in shape. The Si regrowth for the S/D regions is modeled with growth rates which depend on the surface orientation; different growth rates are assumed for the $\langle 100 \rangle$, $\langle 110 \rangle$, and $\langle 111 \rangle$ crystal orientations, which reproduces the diamond shape of the epitaxially grown S/D regions.

We apply a moment-based analytical implantation model [5]. It is capable of capturing complex shadowing effects during the fabrication process. The implantation process produces different doping profiles in the wire, which affects the conductivity and threshold voltage of the individual channels. The electrostatic coupling between the Gate and the Fin forms a parasitic channel below the wires; ground-plane doping has been proposed as a remedy [1].

The complex organic features of the presented topography, cannot be captured through constructive solid geometry modeling approaches. Tetrahedral meshing is performed on the output of the topography simulation to produce a geometry ready for device simulation. For the given example, the run time of the level-set algorithms, surface reconstruction, simplification, and meshing is typically less than half-an-hour on a recent desktop computer.

III. Device Performance and Physics

Device characteristics are simulated based on our *physical modeling* approach implemented as the GTS Nano Device Simulator (NDS) [6]. The core component for predicting

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device performance is a deterministic solver for the subband Boltzmann transport equation based on a phase space (i.e. position-momentum-space) approach. The simulator features a rich set of scattering models specifically designed for non-planar devices [7]. In this work, models for remote Coulomb, remote dipole, and remote phonon scattering were added to adequately model the dissipative transport in the stacked nanowire FET. All remote scattering processes are based on the electrostatic Green's function and include screening from both the channel and the metal gate [8, 9].

An idealized geometry based on the fabricated/emulated device was constructed, shown in Fig. 4, to allow for a better isolation of the various physical effects. Figure 6 shows a comparison between the measured [1] and simulated currents for a 28 nm NMOS device. The *ideal* characteristic is simulated without SiO_2/high-k interface charges and with a surface roughness typical of planar devices ($\Delta_{\text{rms}} = 3$ Å). This represents the expected performance for a mature technology. The measured characteristic, however, exhibits considerable degradation of the drain current owed to the high concentration of charged impurities at the SiO_2/high-k interface and an increased surface roughness of 4 Å. The influence of remote Coulomb scattering induced by interface charges specifically affects the region around V_{th}, as seen in Figs. 5 and 7 which is precisely the region with the highest discrepancy between the ideal and the degraded characteristic. Hence, we conclude that remote Coulomb scattering is the predominant source of performance degradation in the devices.

The comparison between simulation and measurement for slightly scaled 24 nm device is shown in Fig. 8. The same scattering parameters were used as for the 28 nm device resulting in a good match. The slight discrepancy is attributed to device variability which is not included in the performance simulation but is inevitably present in the measurement. Further scaling of the gate length appears feasible from the performance point of view: Fig. 9 shows good g_{m} characteristics for 14 nm and possibly beyond, and Fig. 10 shows a stable subthreshold slope up to the point where the channel length approaches the nanowire diameter. Although reduction of the nanowire diameter would allow for smaller channel length, it also adversely impacts the on-current, as show in Fig. 11. On the other hand, it can be improved by applying mechanical stress in the channel (see Fig. 12).

IV. Reliability and Variability

The stacked NW-FET and a comparable FinFET (without NW formation) are investigated for their susceptibility to random-discrete-dopant-induced effects [10]. A V_{th} distribution with a σ of 11.3 mV for the NW-FET and 5.1 mV for the equivalent FinFET is observed. Figure 13 shows a significant increase of V_{th} variation, which is due to a smaller number of dopants per device, making self averaging less effective. The improved electrostatic control of the channel provides no compensation to the variability. Further optimization of the junction profile is needed to reduce device-to-device variability.

We compare the positive bias temperature degradation behavior of an idealized 28 nm stacked nanowire structure to an equivalent idealized FinFET structure. Bias temperature degradation usually consists of two components, one of which recovers quickly when the stress is removed, and one that shows a more permanent behavior [11]. The discussion in the present work is restricted to an investigation of the recoverable component, which dominates the degradation behavior in constant stress experiments [11]. In our calculations we apply a gate voltage of $V_G = 1.5$ V at a temperature of 115 °C. Our modeling approach uses a four-state non-radiative multi-phonon model [12] to describe the trapping dynamics during BT stress and recovery. This model has been previously shown to accurately describe the *recoverable* component of both the negative and the positive bias temperature degradation [13]. As shown in Fig. 14, our calculations predict a stronger PBT degradation for the nanowire structure.

V. Conclusion

Using a comprehensive set of advanced physical models we have explored the performance, variability, and reliability limits of sub-10 nm technology based on stacked nanowire FETs. We pointed out issues that make the current state of the NW-FET technology inferior to current FinFET technology: (i) degradation of on-current due to impurities in the gate stack, (ii) increased time-zero variability, (iii) enhanced BTI-induced device degradation, and (iv) additional process-induced parasitic capacitances.

Acknowledgment

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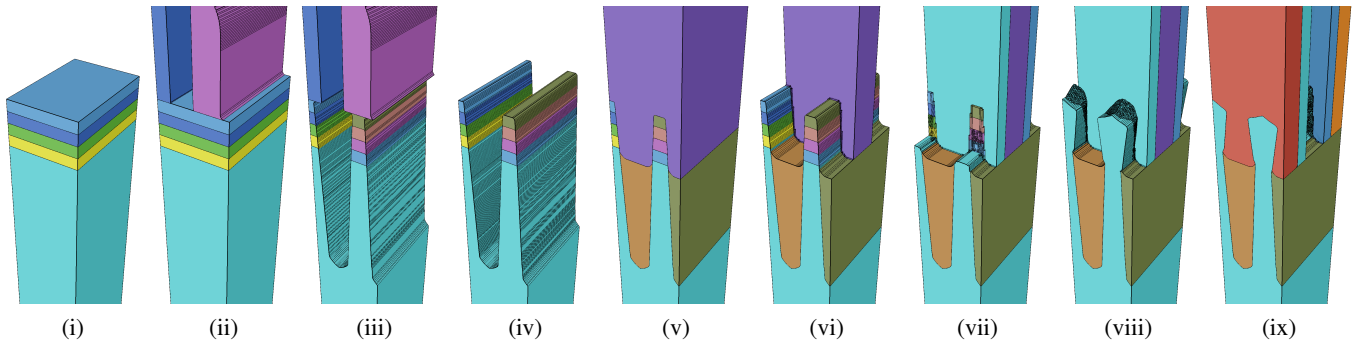

Fig. 1. Process flow: (i) $Si_{1-x}Ge_x$/Si layer growth, (ii) dummy spacer patterning, (iii) etching of fins, (iv) dummy spacer strip, (v) STI formation and dummy gate deposition, (vi) dummy gate patterning, (vii) spacer formation and fin removal in S/D regions, (viii) S/D regrowth by embedded epitaxy, (ix) dummy gate removal, nanowire formation by $Si_{1-x}Ge_x$ etch, gate stack and contact formation

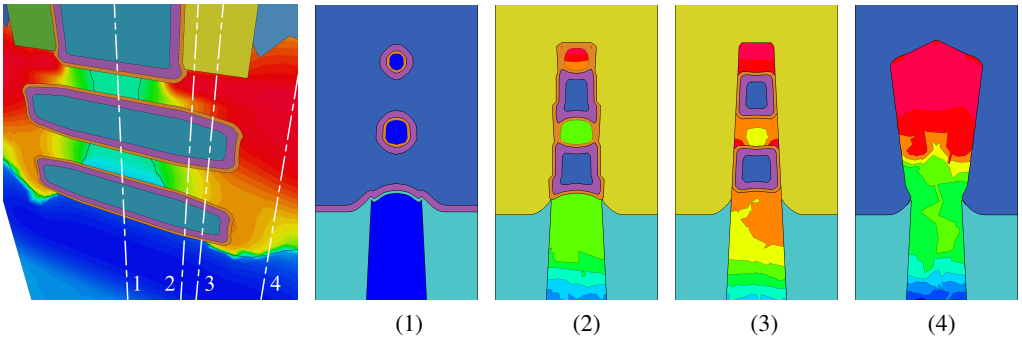

Fig. 2. Final structure delivered by the process emulator, cut along (left) the channel for a detailed view showing the structure and doping profile; cross-sections are shown at different positions along the channel (1-4).

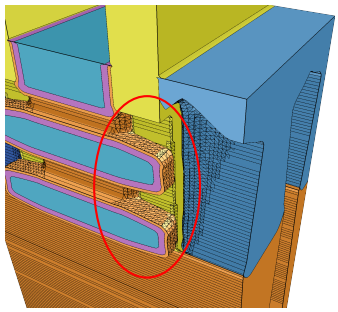

Fig. 3. Since the spacer is formed before the nanowire release, the gate protrudes between the wires, forming parasitic capacitances

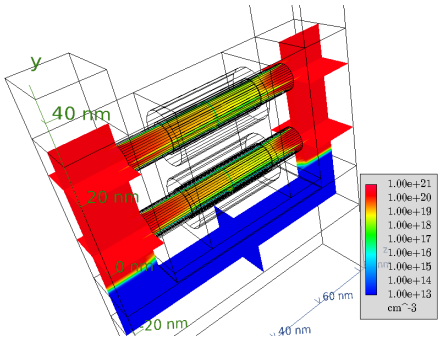

Fig. 4. View of the idealized stacked NW-FET used in the subband Boltzmann transport simulations, showing the electron concentration at $V_G = V_{th}$, $V_{DS} = 0.9\,V$

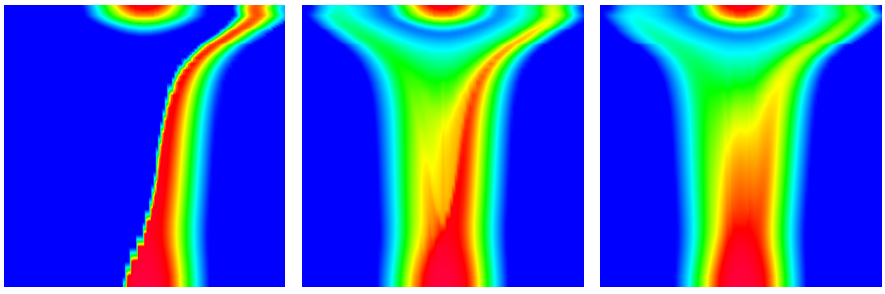

Fig. 5. Phase-space plots of the distribution function in the lowest unprimed subband at $V_G = V_{th}$, $V_{DS} = 0.9\,V$; remote Coulomb (RCS) induces *Coulomb drag* in the channel, giving electrons more time to scatter inelastically via remote and inter-valley phonons.

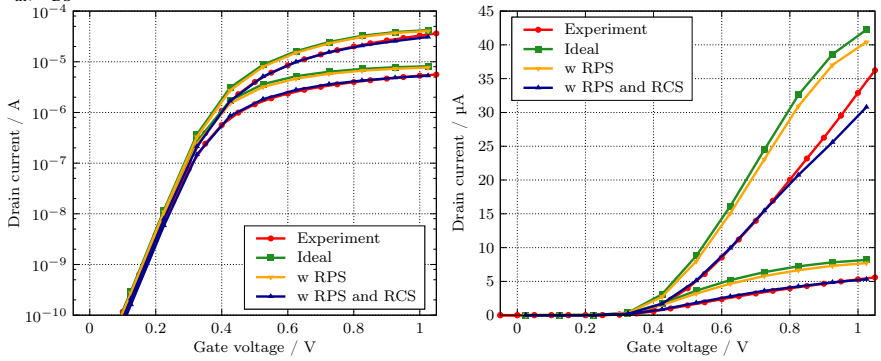

Fig. 6. Transfer characteristics of the 28 nm-channel device; the *ideal* characteristic represents the current achievable when no remote Coulomb scattering is included. The current is degraded by remote polar phonons in the high-k dielectric (RPS) and charges at the SiO_2/high-k interface (RCS). The largest relative degradation is around V_{th} which is typical for remote Coulomb scattering (see Fig. 7).

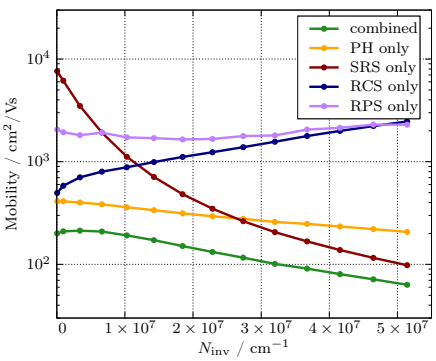

Fig. 7. Non-polar phonon (PH) scattering, surface roughness (SRS) scattering, and remote phonon scattering (RPS) do not depend on SiO_2/high-k interface quality. The added remote coulomb scattering (RCS) particularly affects mobility at low inversion.

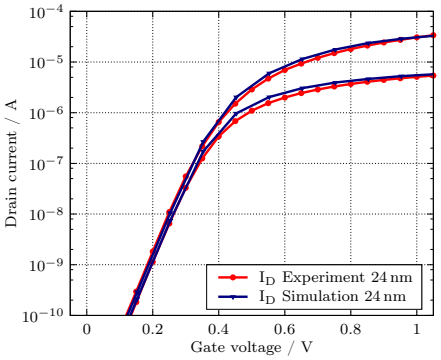

Fig. 8. Transfer characteristic of the scaled 24 nm-channel device; simulated results were obtained using the same parameters (incl. interface charges) as in Fig. 6. The simulations accurately predict the current characteristic of the scaled device.

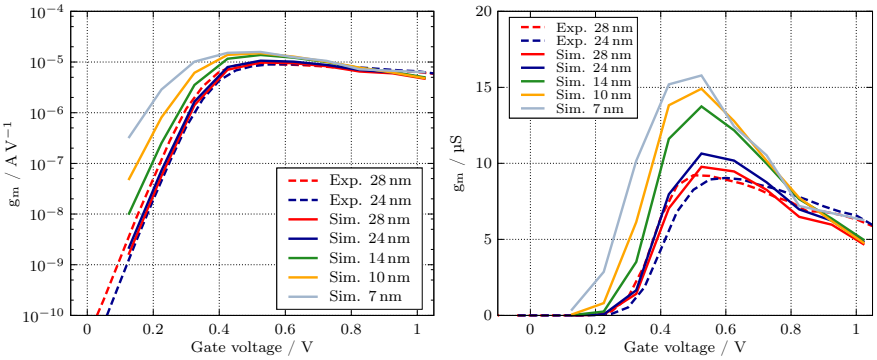

Fig. 9. g_m plots of measured and simulated 24 nm and 28 nm channel lengths together with projections of g_m for scaled channel lengths 14 nm, 10 nm, and 7 nm; peak g_m can be expected to increase with shorter channel lengths, accompanied, however, by a worsening of the sub-threshold slope.

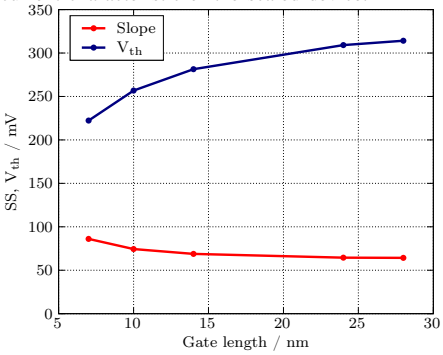

Fig. 10. Extracted subthreshold slopes and threshold voltages for varying gate lengths from 28 nm down to 7 nm; simulated results were obtained using the same parameters (incl. interface charge density) as in Fig. 6. The calculated subthreshold slopes of around 65 mV for the devices with 24 nm and 28 nm gate length match the experimental values from [1]. Subthreshold slope shows good behavior down to gate lengths matching the wire diameter.

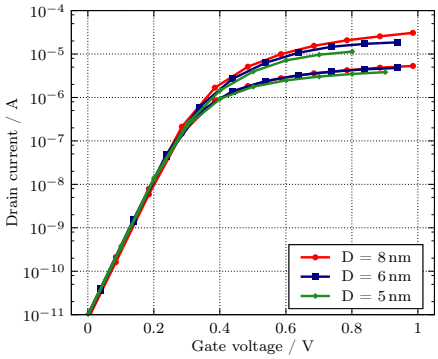

Fig. 11. Transfer characteristic of the 28 nm-channel device with varying channel diameters from 8 nm down to 5 nm; simulated results were obtained using the same parameters (incl. interface charge density) as in Fig. 6 and normalized to an off-current of 10 pA. With decreasing diameter the on-current gets reduced, which can be attributed to increased surface roughness scattering.

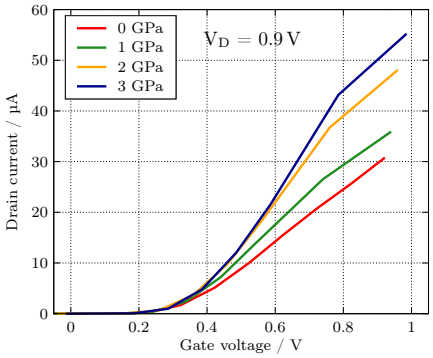

Fig. 12. Transfer characteristic of the 28 nm-channel device at high V_{DS} with applied tensile stress along the channel direction; simulated results were obtained using the same parameters (incl. interface charge density) as in Fig. 6 and normalized to an off-current of 0.1 nA. With increasing stress along the channel we observe a considerable improvement of the on-current in the saturation regime.

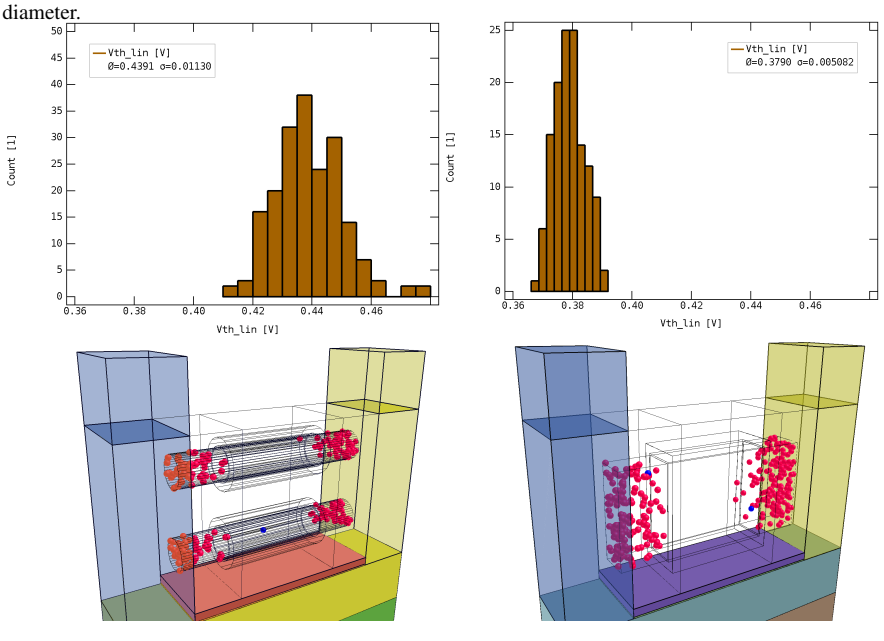

Fig. 13. Using statistical device simulation, the device-to-device variability due to random discrete dopants (RDD) is simulated. Due to self averaging being less effective in a smaller channel, the NW-FET shows increased susceptibility to RDD-induced fluctuations compared to the FinFET. In spite of its superior channel control, the GAA shows an increase of V_{th} variation.

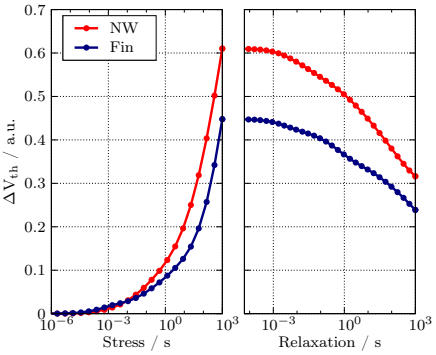

Fig. 14. Comparison of the PBT degradation and recovery transients of a stacked nanowire structure (red) and an equivalent FinFET structure (blue). The voltages applied to the gate during the stress and recovery phase are 1.5 V and 35 mV, respectively. The device temperature is 115 °C. The threshold-voltage shift caused by the traps is calculated in a post-processing step using the charge sheet approximation. The parameters for the trapping in both structures are taken from a recent calibration on a compatible FinFET technology [13]. The stacked nanowire structure shows strongly pronounced degradation compared to the FinFET structure, which is attributed to the higher fields in the cylindrical oxide as well as the stronger coupling of the defects to the channel.