On the Subthreshold Drain Current Sweep Hysteresis of 4H-SiC nMOSFETs

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***Abstract*—We study the subthreshold drain current hysteresis of 4H silicon carbide Si-face (0001) and a-face ($11\bar{2}0$) n-channel power MOSFETs between gate voltage sweeps from accumulation to inversion and vice versa. Depending on the direction of the gate voltage sweep, the MOSFETs show a different subthreshold drain current at the same gate voltage. The observed hysteresis between up-sweep and down-sweep can be expressed as a *subthreshold* voltage shift and may reach several volts. We show that the voltage shift is caused by hole capture in border traps during accumulation and is directly propotional to the charge pumping signal. The voltage shift is fully recoverable by applying a gate bias above the threshold voltage and does not impact device reliability.**

***Index Terms*—4H-SiC, MOSFET, subthreshold hysteresis, border states, Si-face, a-face**

I. Introduction

Silicon carbide (SiC) offers superior material properties for power metal oxide semiconductor field effect transistors (MOSFETs). Due to the larger band gap, critical field and thermal conductivity, MOSFETs based on SiC promise an operation at higher temperature, higher power density, higher frequency and higher voltage than silicon (Si) based MOSFETs. Although advanced processing techniques like post oxidation anneal (POA) in nitrogen (N) containing atmosphere have led to major improvements within the last couple of years [1]–[9], available devices still perform far below their theoretical limits [10]–[16].

In this work, we investigate the *subthreshold* drain current sweep hysteresis observed for SiC power MOSFETs, which behave significantly different from silicon based power devices. It will be shown that it is an intrinsic feature of SiC-MOSFETs, that the *subthreshold* drain current I_D at a certain gate voltage V_G depends on the preceding gate voltage. We define V_G at which I_D reaches 1 nA as *subthreshold* voltage $V_\mathrm{th}^\mathrm{sub}$. $V_\mathrm{th}^\mathrm{sub}$ depends on the sweep direction as indicated in Fig. 1. A V_G sweep in the positive direction (up-sweep) starting at $V_\mathrm{G} = -5\,\mathrm{V}$ results in a $V_\mathrm{th}^\mathrm{sub}$ of $-400\,\mathrm{mV}$. In contrary, a V_G sweep in the negative direction (down-sweep) starting at $V_\mathrm{G} = 5\,\mathrm{V}$ leads to a $V_\mathrm{th}^\mathrm{sub}$ of $+600\,\mathrm{mV}$. The total hysteresis is expressed as a *subthreshold* voltage shift $\Delta V_\mathrm{th}^\mathrm{sub}$ between down-sweep and up-sweep (e.g. $\Delta V_\mathrm{th}^\mathrm{sub} = -1\,\mathrm{V}$ in Fig. 1).

II. Experimental setup

All devices were fabricated on 4H-SiC n-doped substrates using an industrial process. The n-channel Si-face and a-face MOSFETs received a silicon dioxide (SiO_2) dielectric deposited via chemical vapor deposition (CVD). POA was done in a nitric oxide (NO) containing atmosphere for all samples. The measurements are performed on wafer level using an Agilent B1500A parameter analyzer, an Agilent E5250A switching matrix and an Agilent 4294A impedance analyzer. Temperature sweeps are performed via an ATT Systems P40 cooling unit.

III. Gate voltage, time and temperature dependence

Fig. 2 shows the drain current I_D during a gate voltage V_G sweep starting at a negative gate bias to $V_\mathrm{G} = 4\,\mathrm{V}$ (up-sweep, blue) and from $V_\mathrm{G} = 4\,\mathrm{V}$ back to negative bias (down-sweep, red) at a drain voltage of $V_\mathrm{D} = 0.1\,\mathrm{V}$. The down-sweep was performed right after the up-sweep and V_G was switched by a value of 0.1 V every 100 ms for the up-sweep and $-1.0\,\mathrm{V}$ every 100 ms for the down-sweep. While monitoring $V_\mathrm{th}^\mathrm{sub}$ ($I_\mathrm{D}(V_\mathrm{th}^\mathrm{sub}) = 1\,\mathrm{nA}$), we observe an increase in sweep hysteresis the more negative the up-sweep starting gate voltage. The dependence of $\Delta V_\mathrm{th}^\mathrm{sub}$ on the up-sweep starting voltage is shown in Fig. 3. Nearly no $\Delta V_\mathrm{th}^\mathrm{sub}$ is observed as long as the up-sweep starting voltage is higher or equal $-3\,\mathrm{V}$. From this point, the $\Delta V_\mathrm{th}^\mathrm{sub}$ grows linearly with decreasing up-sweep starting voltage until it saturates for $V_\mathrm{G} \leq -12\,\mathrm{V}$. Decreasing the up-sweep starting voltage further does not lead to an increasing hysteresis. Furthermore, the hysteresis is independent of the high level of the gate pulse as long as it is above the threshold voltage V_th. From the maximum $\Delta V_\mathrm{th}^\mathrm{sub}$ of approximately $-4.5\,\mathrm{V}$ we extract a density of trapped charges of approximately $1.4 \times 10^{12}\,\mathrm{cm}^{-2}$ assuming all charges at the SiC-SiO_2 interface. The mechanism behind the hysteresis growth becomes more comprehensible by analyzing the capacitance voltage curves (Fig. 4). The hysteresis emerges as soon as the up-sweep starting voltage falls below the intrinsic Fermi level E_i allowing for hole capture in border traps. The process becomes increasingly efficient until deep accumulation is reached and the hysteresis saturates.

As shown in Fig. 3, a negative bias of $V_\mathrm{G} = -15\,\mathrm{V}$ (accumulation) is sufficient to completely charge the border states and observe the maximum hysteresis. Therefore, switching directly from $V_\mathrm{G} = -15\,\mathrm{V}$ to $V_\mathrm{G} = 0\,\mathrm{V}$ results in a measurable I_D at $V_\mathrm{G} = 0\,\mathrm{V}$ due to the hysteresis effect. The hysteresis is only visible due to the very slow detrapping of charges for a Fermi level position around E_i. Fig. 5 shows the time dependent decay of I_D after the V_G switch for two a-face devices with different active area but otherwise identical. The corresponding voltage shift at $V_\mathrm{G} = 0\,\mathrm{V}$ is shown in Fig. 6. Typically no current

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should flow at $V_G = 0\,V$. However, due to the hysteresis effect caused by trapped positive charges, a drain current of approximately $1\,\mu A$ is detected 10 ms after switching the bias from $V_G = -15\,V$ to $V_G = 0\,V$. I_D scales perfectly with device area indicating a distribution of the current over the whole device. This proofs that the hysteresis is not due to a local device leakage current caused by local electric field variations e.g. at the edges of the device. The charge density driven trapping mechanism is supported by the fact that the hysteresis becomes increasingly smaller when approaching V_{th} and disappears for $V_G \geq V_{th}$ (see red pentagons in Fig. 5 and Fig. 6), where the high electron interface density will cause very fast electron capture (hole emission) leading to a complete recovery. Even after several hundred charging and discharging repetitions, no permanent ΔV_{th}^{sub} component is observed within the available measurement windows of 10 ms suggesting fully reversible trapping and detrapping for gate voltages above V_{th}. The slow recovery in depletion is explained by the low density of electrons available at the interface but needed for electron capture. The model is sketched in Fig. 7. Temperature dependence of V_{th}^{sub} is depicted in Fig. 8. The maximum extent of the hysteresis varies between $-4.2\,V$ at 150 °C and $-4.9\,V$ at 30 °C.

All measurements discussed above correspond to a-face $(11\bar{2}0)$ MOSFETs. We also investigated Si-face (0001) MOSFETs and observed the same trend although the observed ΔV_{th}^{sub} is in the range of millivolts and therefore not that pronounced in the I_D/V_G curves. Compared to the a-face, the mobility μ_0 of the Si-face device is 3 times lower, consistent with recent studies [10]. Despite the lower channel mobility, the border trap density calculated from ΔV_{th}^{sub} is about one order of magnitude lower on Si-face than on the a-face and depicted in Fig. 9. Also for Si-face MOSFETs, no permanent component in the hysteresis is observed.

IV. Charge pumping

Charge pumping (CP) [17] is a suitable technique to investigate the sweep hysteresis because it is sensitive to interface and border states. The technique was recently demonstrated on 4H-SiC MOSFETs in various studies [18]–[22]. The temperature dependence of the number of pumped charges per cycle N_{CP} in constant high level and constant base level CP measurements is shown in Fig. 10 for the Si-face device and Fig. 11 for the a-face device. The Si-face shows an increase in N_{CP} for lower temperatures indicating higher trap densities close to the band edges of 4H-SiC, whereas the a-face device shows minor and inverted temerpature dependence indicating most of the CP signal originates from states located around midgap. Fig. 12 shows N_{CP} depending on the low level of the gate pulse at 30 °C for both devices. Although the absolute number of trapped charges differ from Fig. 9, the same trend is observed. For the Si-face we extract a N_{CP} of approximately $0.6 \times 10^{12}\,cm^{-2}$ and for the a-face we extract a N_{CP} of $3 \times 10^{12}\,cm^{-2}$ which is about 5 times higher. The linear correlation between ΔV_{th}^{sub} and the charge pumping current I_{CP} for a-face devices is depicted in Fig. 13 (top). Devices which show an 5 % increased hysteresis also show an 5 % increased I_{CP}. In the bottom plot of Fig. 13 the correlation of N_{CP} and ΔV_{th}^{sub} for both crystal planes is depicted. The result suggests the same origin for the hysteresis and increased charge pumping current on both crystal faces. The discrepancy in the total number of trapped charges extracted via the sweep hysteresis and the CP technique originates from various experimental limits of the sweep measurements, e.g extraction piont of ΔV_{th}^{sub} and switching speed resulting in an narrower active energy window [23] (see Fig. 14).

The energetic distribution of the interface/border state density D_{it} was extracted using spectroscopic charge pumping [24], [25]. The result is shown in Fig. 15 for both crystal faces. For the Si-face device, we extract a D_{it} of approximately $0.25 \times 10^{12}\,cm^2\,eV^{-1}$ around midgap and an exponential increase close to E_C. Even though the a-face device has a 5 times higher D_{it} around midgap resulting in a more pronounced *subthreshold* hysteresis, the D_{it} is much lower close to E_C favoring higher mobility. A similar trend of the D_{it} close to E_C for both crystal faces was reported by Kimoto et al [26] using the $C - \psi_s$ method, which is based on the theoretical capacitance curve.

The atomic origin of the sweep hysteresis and the difference in hysteresis for a-face and Si-face 4H-SiC power MOSFETs might be a difference in interface structure for Si-face and a-face MOSFETs. Ion contamination as a cause of the hysteresis is excluded by the sign of the voltage shift, the speed of the capture and emission process and the temperature dependence.

V. Conclusion

We investigated the *subthreshold* drain current hysteresis ΔV_{th}^{sub} during gate voltage up and down-sweeps for 4H-SiC Si-face (0001) and a-face $(11\bar{2}0)$ MOSFETs, which behave significantly different from silicon based power devices. We show that ΔV_{th}^{sub} scales with the charge pumping signal and disappears for gate voltages above the threshold voltage within the available measurement window of 10 ms. The difference in ΔV_{th}^{sub} and mobility for a-face and Si-face devices is explained by the energetic distribution of the border states obtained via spectroscopic charge pumping: a-face devices show a more distinct hysteresis due to a higher border state density around midgap, but also higher mobility due to a lower border state density close to the conduction band edge of 4H-SiC. ΔV_{th}^{sub} is fully recoverable via biasing the device near or above its V_{th}. Thus, the normally off characteristics of the SiC-MOSFET is maintained in any switching case despite of the reported hysteresis effect in the subthreshold regime.

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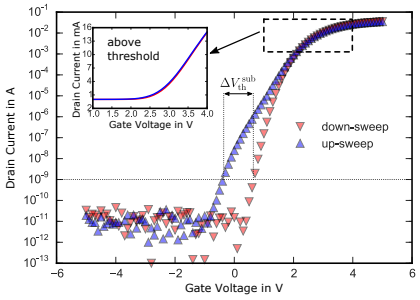

Figure 1. Sweep hysteresis between up-sweep starting at −5 V (blue) and down-sweep starting at 5 V (red). The dotted line corresponds to the readout current of the V_{th}^{sub} at 1 nA. The inset shows the characteristics above the threshold voltage where the hysteresis effect vanishes.

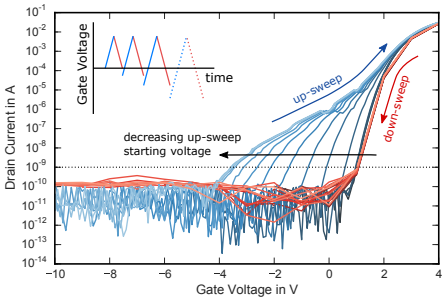

Figure 2. Increase of the sweep hysteresis depending on the starting voltage of the up-sweep (blue) with inset of the measurement procedure, a gate voltage sweep with varying low level and constant high level.

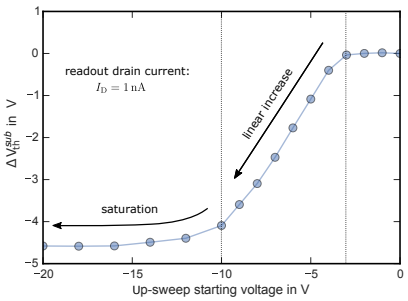

Figure 3. *Subthreshold* voltage shift at a drain current of 1 nA as a function of the up-sweep starting voltage. The hysteresis at 1 nA starts to increase linearly as soon as the up-sweep starting voltage falls below −3 V and satturates for up-sweep starting voltages below −12 V.

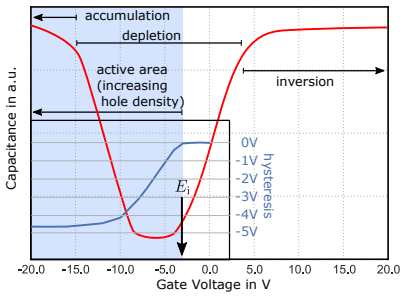

Figure 4. *Subthreshold* voltage shift (blue) and capacitance voltage curve (red). The hysteresis starts to grow, as soon as the Fermi level falls below the intrinsic Fermi level E_i and holes are available at the interface. The hysteresis satturates as soon as the Fermi level approches the conduction band of 4H-SiC (accumulation).

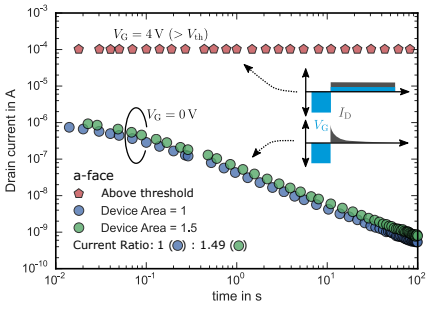

Figure 5. Recovery of I_D at V_G below and above the V_{th} after a charging pulse at $V_G = -15$ V on an a-face device. In the subthreshold regime at $V_G = 0$ V (circles), I_D recovery shows a logarithmic dependence in time and scales with active area indicating a uniform distribution of the hysteresis current above the whole device area. The hysteresis effect is not visible for $V_G > V_{th}$ (red, pentagons). The same trend is observed on Si-face devices. The measurement pattern is depicted in the inset.

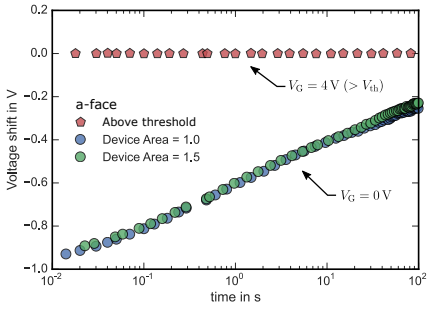

Figure 6. Voltage shift according to the recovery of the drain current in Fig. 5. After switching from accumulation at $V_G = -15$ V to depeltetion at $V_G = 0$ V, the voltage shift recovers with a logarithmic dependen in time. The voltage shift is independent of the active area (circles) and disappears for gate voltages above the threshold voltage, e.g. at $V_G = 4$ V (red, pentagons) within the measurement window of 10 ms after the bias change.

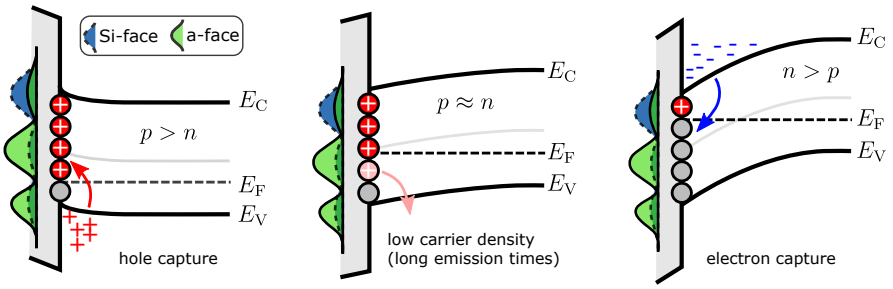

Figure 7. Schematic band diagram of the mechanism causing the sweep hysteresis. Left: hole capture in accumulation (Fermi level close to the valence band). Middle: At a Fermi level position close to midgap only a few carriers are available resulting in a slow recovery of the trapped holes. Right: recombination due to very high electron density at the interface for a Fermi level position close to the conduction band.

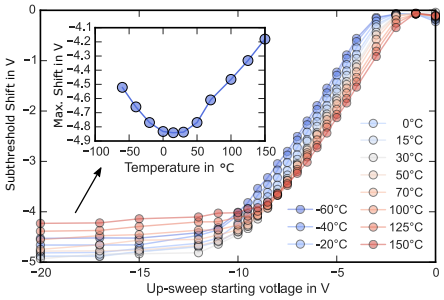

Figure 8. Temperature dependence of the hysteresis between −60 °C and 150 °C. The maximum of the hysteresis stays within −4.2 V and −4.9 V.

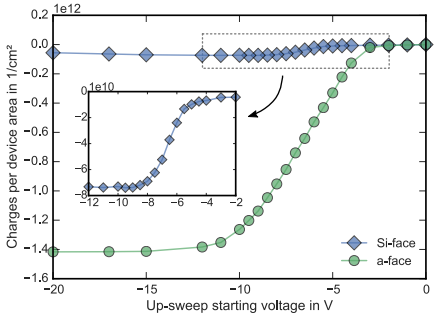

Figure 9. Trapped charges per device area as a function of the up-sweep starting voltage for a Si-face (diamonds) and an a-face (circles) device. The same trend is observed on both crystal faces although the effect is more distinct on the a-face.

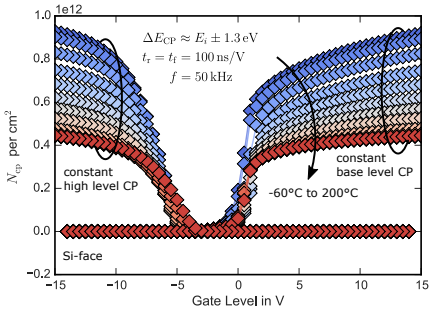

Figure 10. Charges pumped per cycle extracted from constant base level CP (right side) and constant high level CP (left side) for the Si-face device. The increase in CP current originates from trap states close to the the band edges of 4H-SiC.

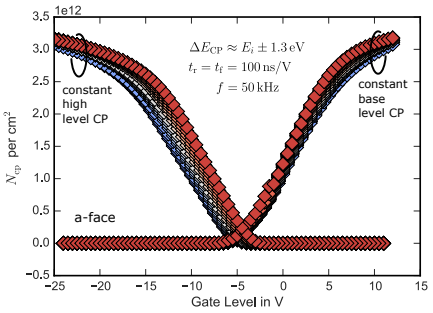

Figure 11. Same as Fig. 10 but now for the a-face device. We observe a minor and inverted temperature dependence indicating the major contribution to the charge pumping current originates from states around midgap.

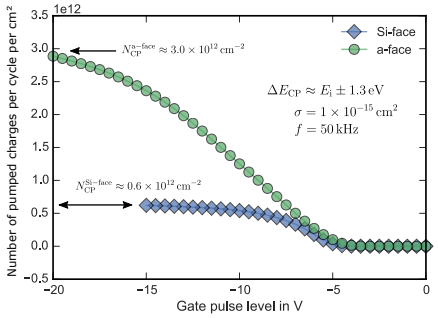

Figure 12. Number of charges pumped during a constant high level charge pumping measurement at 30 °C for the a-face (circles, green) and Si-face (diamonds, blue) device. Although the a-face devices show better mobility, the state density is a factor of 5 higher. The increase is most likely due to defect states close to E_i.

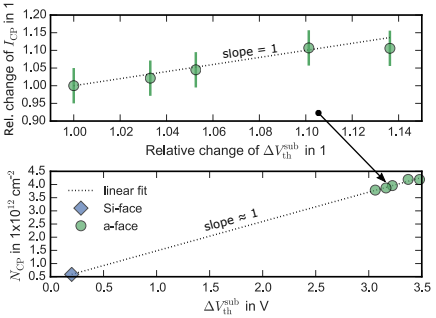

Figure 13. Top: linear increase of the charge pumping current I_{CP} with increasing sweep hysteresis ΔV_{th}^{sub} on a-face devices. Bottom: increase in the number of pumped charges per cycle N_{CP} with increasing hysteresis for the Si-face (diamonds, blue) and a-face (circles, green). Due to the linear dependency, ΔV_{th}^{sub} most likely originates from border states at the SiC-SiO_2 interface.

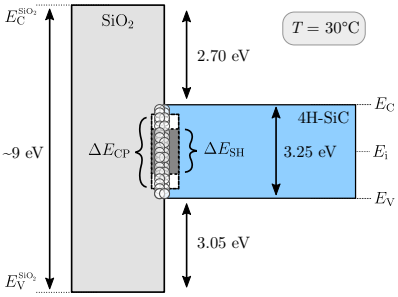

Figure 14. Schematic band diagram of the SiC-SiO_2 system to illustrate the difference in the active energy window in the charge pumping ΔE_{CP} and sweep hysteresis ΔE_{SH} measurements. Due to the slower slew rates, ΔE_{SH} is approximately 0.8 eV narrower at 30 °C resulting in a reduced number of interface and border states contributing to the measurement signal.

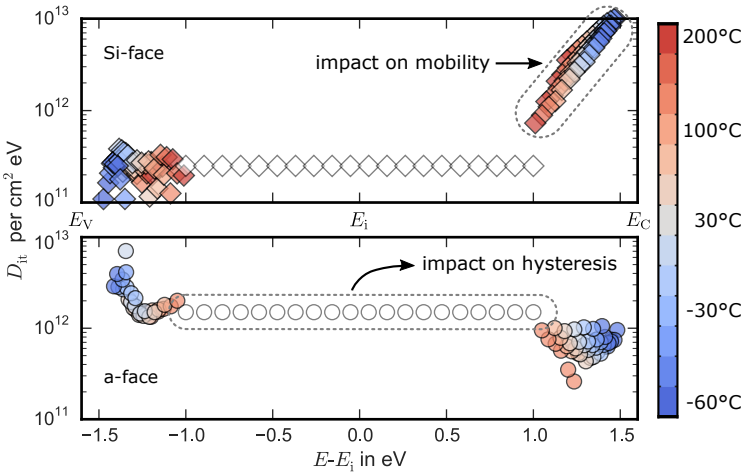

Figure 15. Energetic border/interface state distribution D_{it} for the Si-face (diamonds, top) and a-face (circles, bottom). Although the a-face shows 5 times higher D_{it} around midgap resulting in a more pronounced hysteresis, the D_{it} close to E_C is about one order of magnitude lower resulting in improved mobility.

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