Improved interface trap density close to the conduction band edge of a-face 4H-SiC MOSFETs revealed using the charge pumping technique

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Abstract. We study the interface properties of 4H silicon carbide Si-face (0001) and a-face $(11\bar{2}0)$ power MOSFETs using the charge pumping technique. MOSFETs produced on the a-face show a higher electron mobility than Si-face devices, although their charge pumping signal is 5 times higher, indicating a higher interface/border trap density. We show the main contribution to the interface/border trap density on a-face devices originates from deep states in a wide range around midgap, whereas Si-face devices show a higher and exponentially increasing interface/border state density close to the conduction band edge of 4H silicon carbide, resulting in reduced mobility.

Introduction

MOSFETs based on silicon carbide (SiC) promise better performance for power applications than silicon based MOSFETs because they allow an operation at higher temperature, higher power density, higher voltage and higher frequency than silicon based devices. Although power MOSFETs based on SiC have been available on the market for several years and advanced processing techniques like post oxidation anneal (POA) in nitrogen (N) containing atmospheres have led to major improvements within the last couple of years, available SiC-MOSFETs still perform below their theoretical limits as they show increased threshold voltage drifts and reduced mobility.

In order to better understand the responsible defects, we study the interface properties of 4H-SiC n-channel Si-face and a-face power MOSFETs using the charge pumping (CP) technique [1]. Depending on the oxidized crystal plane, 4H-SiC MOSFETs show significant differences in their electrical properties like mobility and drain current hysteresis.

Experimental Setup

All devices were fabricated on n-doped 4H-SiC substrates with a several μm thick low-doped epitaxial layer on top. To investigate the interface properties of the a- and the Si-faces, we used n-channel 4H-SiC power MOSFETs specifically designed for CP measurements. These measurements require the p-doped body regions to be electrically separated from the n-doped source regions. The gate oxides of the n-channel Si-face and a-face devices consist of a silicon dioxide bulk dielectric deposited via chemical vapor deposition (CVD) which is post oxidation annealed in a high temperature nitric oxide (NO) atmosphere. The Si-face devices have a gate length of 5.3 μm and a gate width of 100 μm and the a-face devices have a gate length of 0.5 μm and a gate width of 30 μm. All measurements are performed on wafer level using an Agilent B1500 parameter analyzer and an Agilent E5250A switching matrix. Temperature sweeps between -60°C and 200°C are performed via an ATT Systems P40 cooling unit.

The low field channel mobility of the devices was extracted from drain current vs. gate voltage characteristics. We extracted a low field channel mobility of $\mu_0 = 18$ cm²/Vs for the Si-face and an
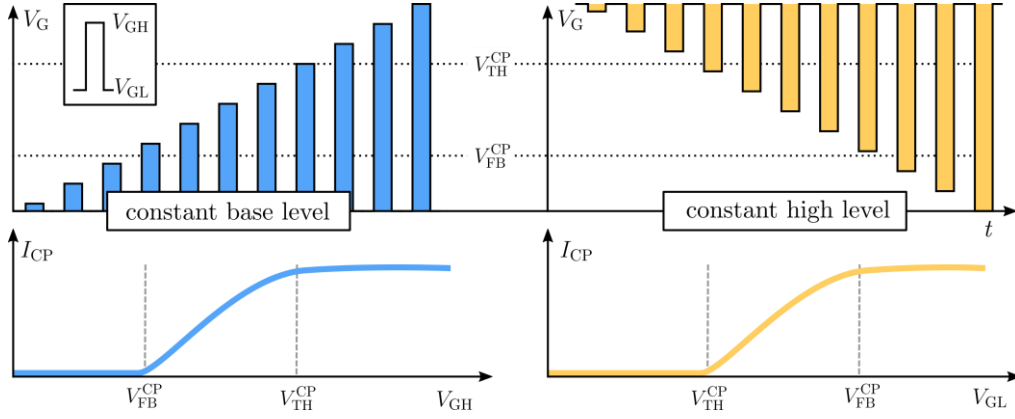
Figure 1: Schematic sketch of constant base level CP (left) and constant high level CP (middle) and corresponding charge pumping current at the bulk contact. The maximum charge pumping current is measured if the gate is biased above $V_{\text{TH}}^{\text{CP}}$ and below $V_{\text{FB}}^{\text{CP}}$.

about 3 times higher mobility of $\mu_0 = 60$ cm²/Vs for the a-face device, consistent with studies showing higher mobility values for a-face devices [2]. Constant high level and constant base level CP measurements (see Fig. 1) were performed on both devices to extract the number of charges pumped per cycle N_{CP} [3]. CP is an electrical measurement method for the quantitative determination of interface and border states in MOSFETs via their recombination current. The technique was recently demonstrated on 4H-SiC MOSFETs [4]. In CP measurements, the gate is pulsed at a frequency of several kHz while source, drain and bulk terminals are grounded. If the gate is pulsed between accumulation and inversion, a bulk current can be monitored as a consequence of consecutive electron and hole trapping via interface and border states (=charge pumping current I_{CP}). The measurement setup is sketched in Fig. 2. N_{CP} is extracted from I_{CP} via

$$N_{\text{CP}} = I_{\text{CP}}(A_{\text{eff}}qf)^{-1} \tag{1}$$

with the effective gate area A_{eff}, the frequency of the gate pulse f, and the electronic charge q. The average density of interface/border states per eV is given by

$$\overline{D_{\text{it}}} = qN_{\text{CP}}/\Delta E_{\text{CP}} \tag{2}$$

within the monitored fraction of the band gap (= active energy window ΔE_{CP}). We can estimate ΔE_{CP} by

$$\Delta E_{\text{CP}} = 2k_{\text{B}}T \cdot \log\left(\frac{\Delta V_{\text{G}}}{n_{\text{i}}\sqrt{\nu_{\text{thn}}\nu_{\text{thp}}}\sqrt{\sigma_{\text{n}}\sigma_{\text{p}}}\sqrt{t_{\text{f}}t_{\text{r}}}(V_{\text{TH}}^{\text{CP}} - V_{\text{FB}}^{\text{CP}})}\right) \tag{3}$$

with the temperature T, the Boltzmann constant k_{B}, the amplitude of the gate pulse ΔV_{G}, the intrinsic carrier density n_{i}, the average thermal velocity for electrons and holes ν_{thn} & ν_{thp}, the capture cross section of electrons and holes σ_{n} & σ_{p}, the pulse rise and fall times t_{r} & t_{f} and the CP threshold and flatband voltages $V_{\text{TH}}^{\text{CP}}$ & $V_{\text{FB}}^{\text{CP}}$ [5]. As indicated in Fig. 3, the active energy window ΔE_{CP} in which traps contribute to the CP signal narrows around the intrinsic energy level at elevated temperatures or decreased rise/fall times.

Constant high/base level CP measurements at $f = 50$ kHz and fixed transition times of $t_{\text{r}} = t_{\text{f}} = 100$ ns/V in a wide temperature range between -60°C and 200°C were performed on both devices. Fig. 5 shows the results for the Si-face device and Fig. 5 for the a-face device.
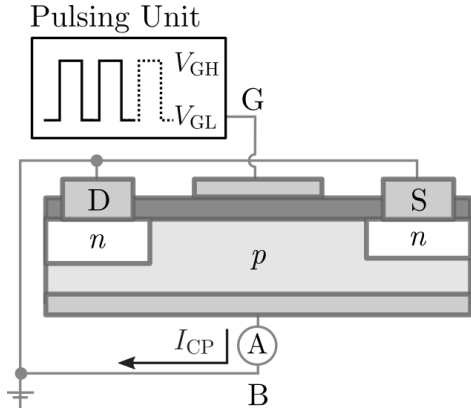
Fig. 2: Schematic of the CP measurement. The gate is pulsed at 50 kHz while drain, source and bulk are grounded. The recombination current I_{CP} is monitored at the bulk.
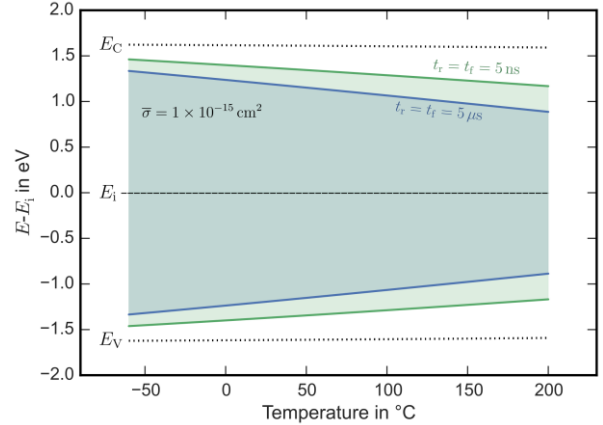

Fig. 3: Active energy window around E_i as a function of T according to Eq. 3 for two different transition times. We used a value of $\sigma = 1 \times 10^{-15}$ cm^2 for the calculation.
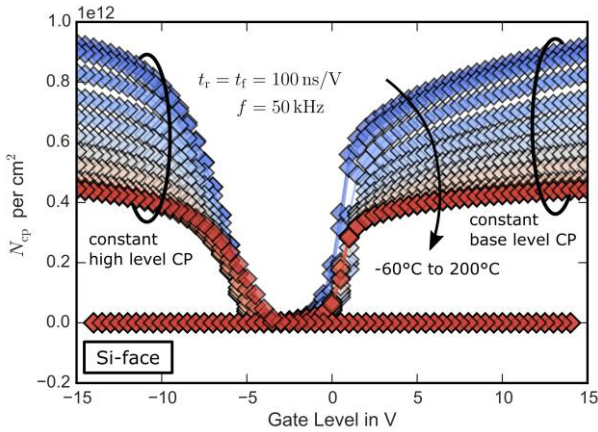

Fig. 4: N_{CP} extracted from constant base level CP (right side) and constant high level CP (left side) for the Si-face. The increase in N_{CP} for lower T indicates a high density from states close to E_V and E_C.
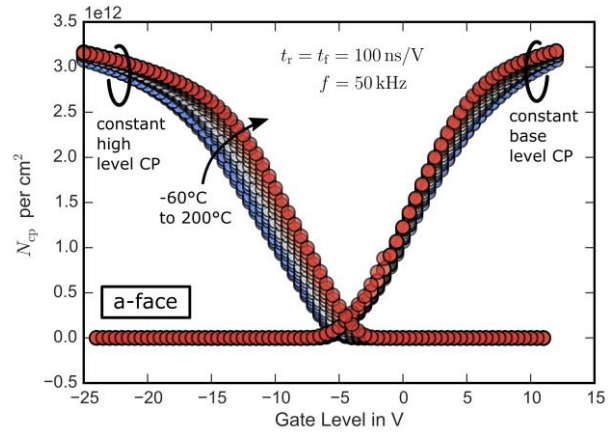

Fig. 5: Same as Fig. 4 but now for the a-face device. We observe a minor and inverted temperature dependence, indicating a low defect density close to E_V and E_C.
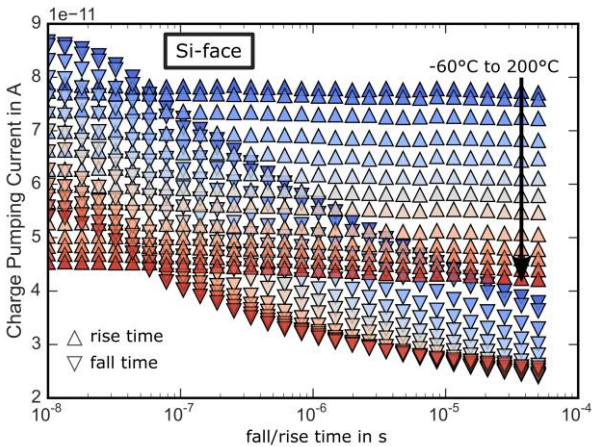

Fig. 6: I_{CP} as a function of T and the rise and fall times of the gate pulse for the Si-face device. The strong change in I_{CP} with t_f indicates a high D_{it} close to the conduction band edge.
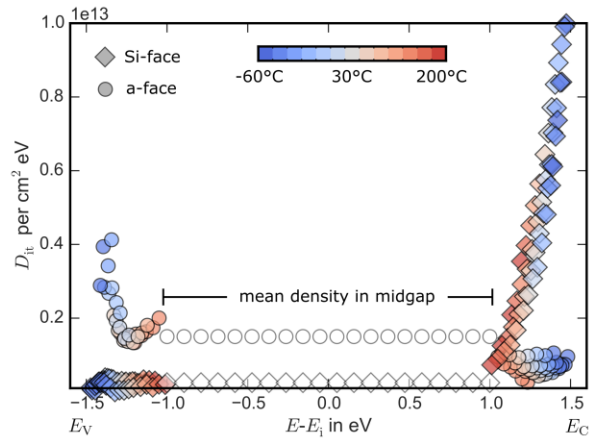

Fig. 7: Interface/border trap distribution of the Si-face (diamonds) and a-face (circles) device. The mean in a wide range around midgap is indicated in white symbols.

Although the a-face device shows a 3 times higher mobility of 60 cm²/Vs, the average D_{it} extracted from CP measurements is about five times higher for the a-face device ($D_{it}^{Si} = 0.25 \times 10^{12}$ cm²eV^{-1} and $D_{it}^{a} = 1.20 \times 10^{12}$ cm^{-2}eV^{-1}) resulting in a more pronounced sub-threshold drain current hysteresis.

Spectroscopic charge pumping

The discrepancy between mobility and D_{it} is a result of the different energetic distribution of interface/border traps for both crystal planes. We extracted the energetic distribution of D_{it} using spectroscopic CP following the approach of van den Bosch [6]. A change in ΔE_{CP} by varying T, t_f and t_r (see Eq. 3) results in a change in I_{CP} (shown in Fig. 6 for the Si-face device) and therefore the D_{it} according to Eq. 1 & Eq. 2. We obtained a spectroscopic plot of D_{it} for both devices, which is shown in Fig. 7. Even though the a-face device has a higher D_{it} around midgap ($D_{it}^{a} = 1.20 \times 10^{12}$ cm²eV^{-1} against $D_{it}^{Si} = 0.25 \times 10^{12}$ cm²eV^{-1}), resulting in a more pronounced subthreshold hysteresis, the D_{it} is much lower close to E_C favoring higher mobility. The difference in D_{it} close to E_C in a-face and Si-face devices annealed in NO is supported by Kimoto et al [7] using the $C-\psi_s$ method, which is based on the theoretical capacitance curve and does not give information about deep states.

Conclusion

NO annealed SiC-MOSFETs with channels on the Si-face (0001) and a-face $(11\bar{2}0)$ vary in electrical properties such as mobility and drain current hysteresis. The reason lies in different energetic distributions of interface/border states. We directly extracted the interface/border state distribution for both crystal planes using CP measurements. Although the a-face device has a 5 times higher D_{it} than the Si-face device in a wide range around midgap ($E_i \pm 1$ eV), resulting in a more pronounced hysteresis, its significantly reduced D_{it} close to E_C is the main reason for the improved mobility.

Acknowledgements

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