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Mapping of CMOS FET degradation in bias space—Application to dram peripheral devices

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Mapping and visualization of all degradation modes in both n- and p-channel field effect transistors, specifically devices for dynamic random access memory periphery, is performed in the (V_G, V_D) bias space applicable for complementary metal–oxide–semiconductor operation. This "all-in-one" approach allows for tracking and studying in parallel all degradation regimes, including bias temperature instability, hot carrier degradation, and off-state stress, as well as the transitions between them. It should prove beneficial when developing new very large-scale integrated technologies, since it allows for simultaneous comparison and checking of all degradation regimes and promptly identifying "weak spots" of each technology option. It also allows to choose the correct criteria (voltages or fields) at a later time and postprocessing the data as necessary. © *2016 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4972872]

I. INTRODUCTION

During operation of complementary metal–oxide–semiconductor (CMOS) digital circuits, transistors experience a range of combinations of gate V_G and drain V_D biases. An example for an n-channel and a p-channel Field Effect Transistor (nFET and pFET) in a logic inverter powered with supply voltage V_{DD} is given in Fig. 1.[1] As the inverter input switches between logic levels, the V_G and V_D biases change, and consequently, the inverter FETs operate in different regimes.

In today's very large-scale integrated (VLSI) technologies, FET operation is accompanied by aging of the FETs, with a range of degradation regimes mapping onto the FET operation regimes. Specifically for the inverter at hand, when logic one, i.e., V_{DD}, is applied to the gate, the nFET is "on" while the pFET is "off," and the inverter output V_D is 0 V. Consequently, no voltage is applied across the nFET source/drain terminals, while full V_{DD} is applied across the pFET source/drain terminals. In this condition, the nFET is biased in a regime corresponding to bias temperature instability (BTI; $|V_G| \sim V_{DD}$, $V_D \sim 0$ V),[2] while the pFET is biased in a regime referred to as off-state stress (OSS; $V_G \sim 0$ V, $|V_D| \sim V_{DD}$, assuming the pFET biases are offset by V_{DD} so the source bias $V_S = 0$ V).[3–8] Conversely, for logic zero on the inverter input, the nFET undergoes OSS degradation while the pFET experiences BTI.

During the rapid switching between the two logic states, the inverter output V_D voltage momentarily lags behind the input (due to the considerable FET and interconnect impedances) and a combination of both nonzero V_G and V_D is briefly applied. In this regime, the FETs will undergo degradation due to carriers accelerated in the FET channel; hence, the term hot carrier degradation (HCD; $|V_G|$ and $|V_D| \sim V_{DD}$) is used.[9,10] Hot channel carriers *in the subthreshold regime* are also responsible for OSS, while only thermalized "equilibrium" carriers are present in the BTI regime. Appreciable gate oxide electric fields accelerating BTI are also present in sections of the gate oxide during all degradation regimes—a combination of degradation mechanisms is therefore taking place simultaneously as the FETs operate.[11,12] The relative contribution of each degradation mechanism will depend on the actual function of each FET in the circuit and the actual (V_G, V_D) workload on that device.

Given the above, we find it highly instructional to map the degradation *in the entire (V_G, V_D) space applicable for CMOS FET operation*.[13] The approach, reported here, allows for tracking and studying in parallel all degradation regimes,

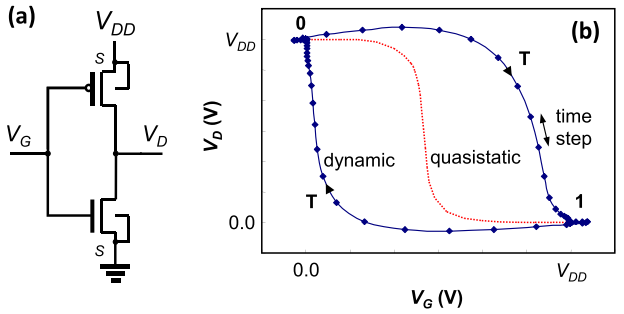

FIG. 1. (Color online) (a) Inverter with input (gate voltage) V_G and output (drain voltage) V_D. V_{DD} is the (arbitrary) supply voltage. (b) Simulation of (V_G, V_D) combinations applied to an inverter subjected to ~GHz digital signal (dynamic), compared to a slow sweep (quasistatic) (Ref. 1). "1" and "0" correspond to the logic state at the inverter input, "T" to the transition between states.

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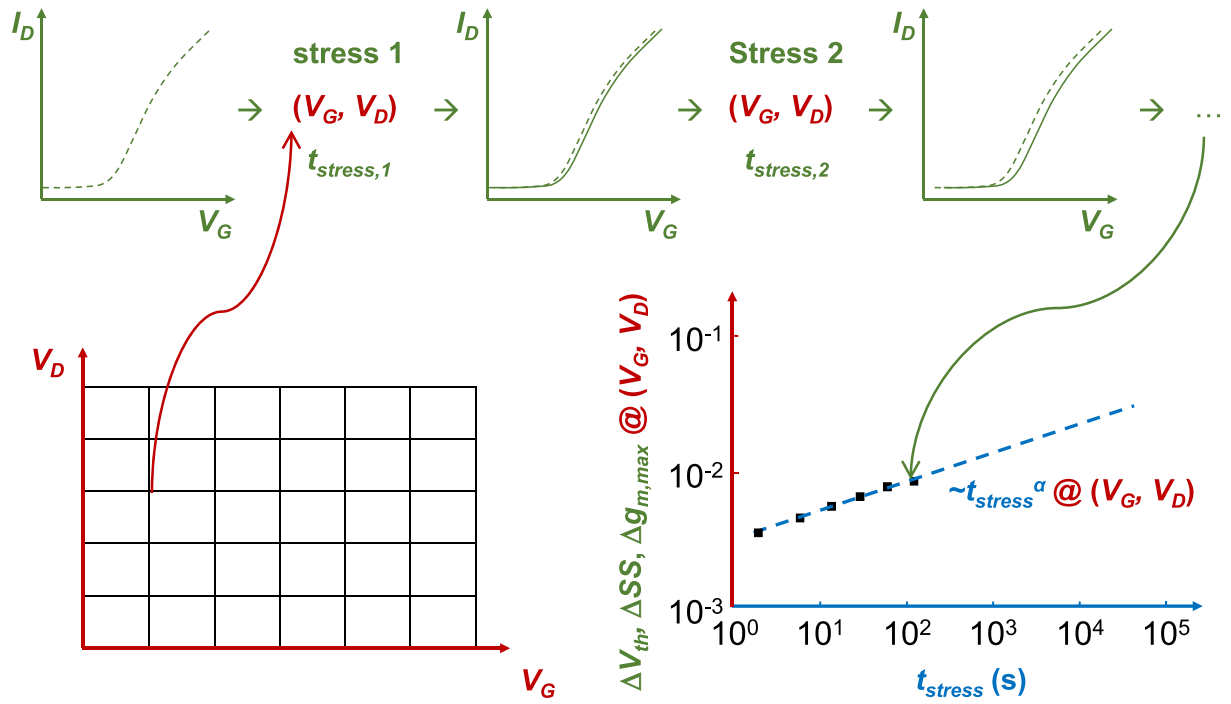

FIG. 2. (Color online) Schematic methodology applied in this work.

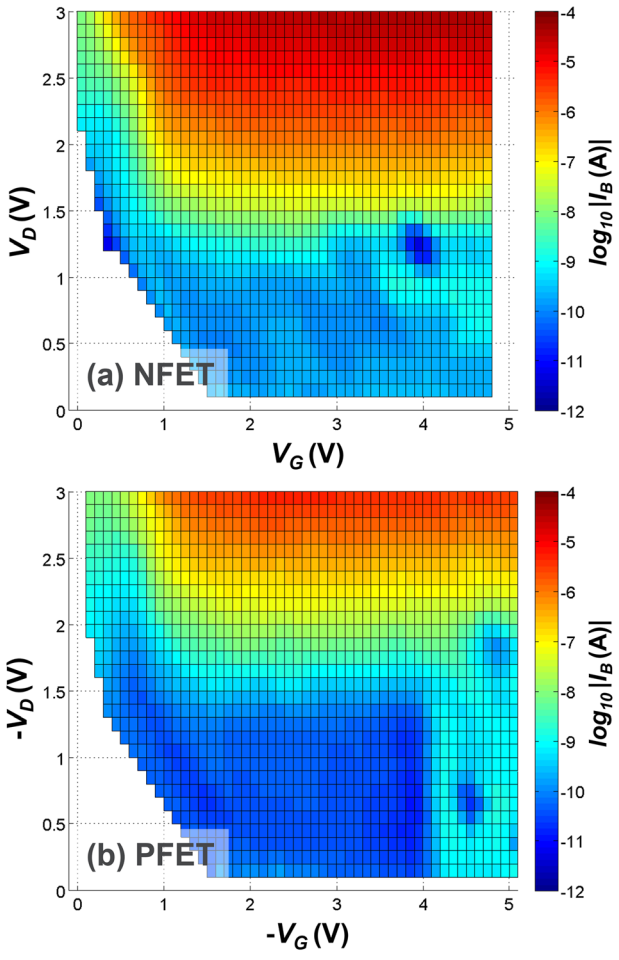

FIG. 3. (Color online) Substrate current I_B in unstressed (a) nFETs and (b) pFETs. A slight increase in background current in (b) for $V_G < -4$ V is due to using less sensitive instrumentation for that part of the (V_G, V_D) matrix.

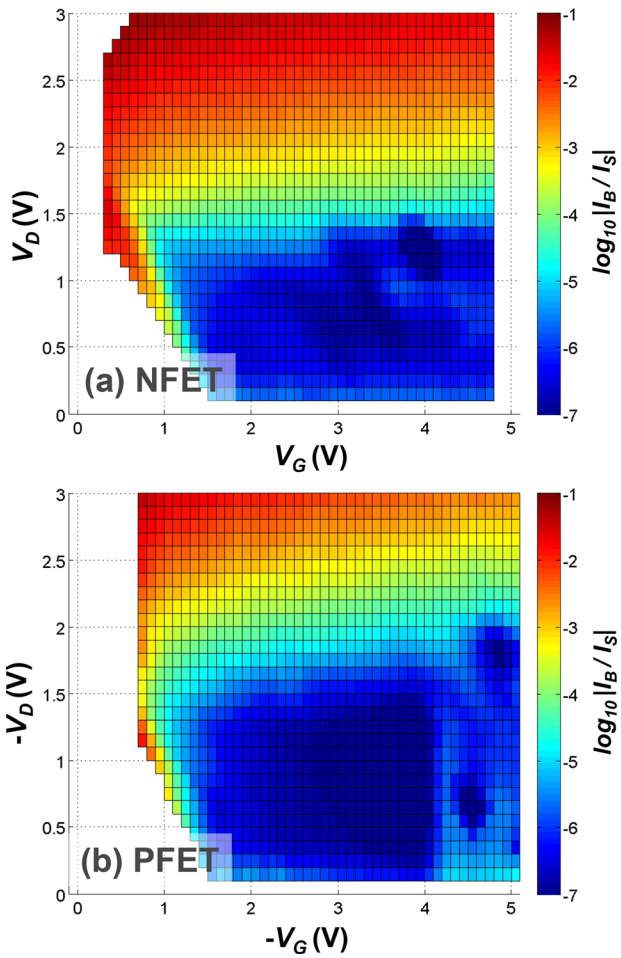

FIG. 4. (Color online) Multiplication factor I_B/I_S in unstressed (a) nFETs and (b) pFETs. Values at low $|V_G|$'s are not plotted as I_S is negligible there.

as well as the transitions between them. When developing new VLSI technologies, the "all-in-one" approach allows for simultaneous comparison and checking of all degradation regimes and promptly identifying "weak spots" of each technology option. Although not discussed here, the total degradation can be estimated by convoluting the actual device workload with the degradation maps. Furthermore, the simple and pragmatic methodology allows to gather sufficient reliability information in a systematic manner *in a single pass* and thus allows the experimenter to choose the correct criteria (voltages or fields) and postprocessing the data as necessary *at a later time*.

II. EXPERIMENT

The only requirement of the methodology is the availability of a sufficient number of identical devices. We use ~100 *individual*, nominally identical CMOS FETs, presently under development for dynamic random access memory periphery input–output applications (V_{DD} ~3 V),[14] to map the degradation in the entire applicable (V_G, V_D) space. The simple measurement methodology is illustrated in Fig. 2. A fresh device with as-drawn $L = 70$ nm, $W = 1000$ nm, and high-k gate oxide with equivalent oxide thickness (EOT) ~4.5 nm is used here for every (V_G, V_D) combination selected from the matrix (Fig. 2, bottom left); low (V_G, V_D) combinations resulting in no appreciable stress are skipped. "Forward" (designated as *fwd*; V_D biased) and "reverse" (designated as *rev*; V_S biased) linear-regime *I-V* characteristics are measured, interlaced with stress phases at (V_G, V_D) with (exponentially) increasing stress times $t_{\mathrm{stress},i}$ and room temperature (Fig. 2, top). The *I-V* is adjusted during the *I-V* measurement to always guarantee sufficient information but simultaneously to avoid stressing the device. For the latter reason, measurement of saturation-regime *I-V*$_S$ is omitted altogether. In the experiment presented here, the precise *I-V* curve measurement is relatively slow (~10 s per sweep); hence, relaxation effects are not monitored. However, the experiment can be easily redesigned to perform relaxation measurements for each (V_G, V_D) combination,[15] as well as evaluation of other parameters.

Afterward, the threshold voltage V_{th}, the subthreshold slope *SS*, and the maximum transconductance $g_{m,\max}$ are extracted from all *I-V*$_S$, and the *shifts* with respect to the initial prestress values, designated by Δ, are calculated, plotted versus the stress times t_{stress}, and fitted with a simple power

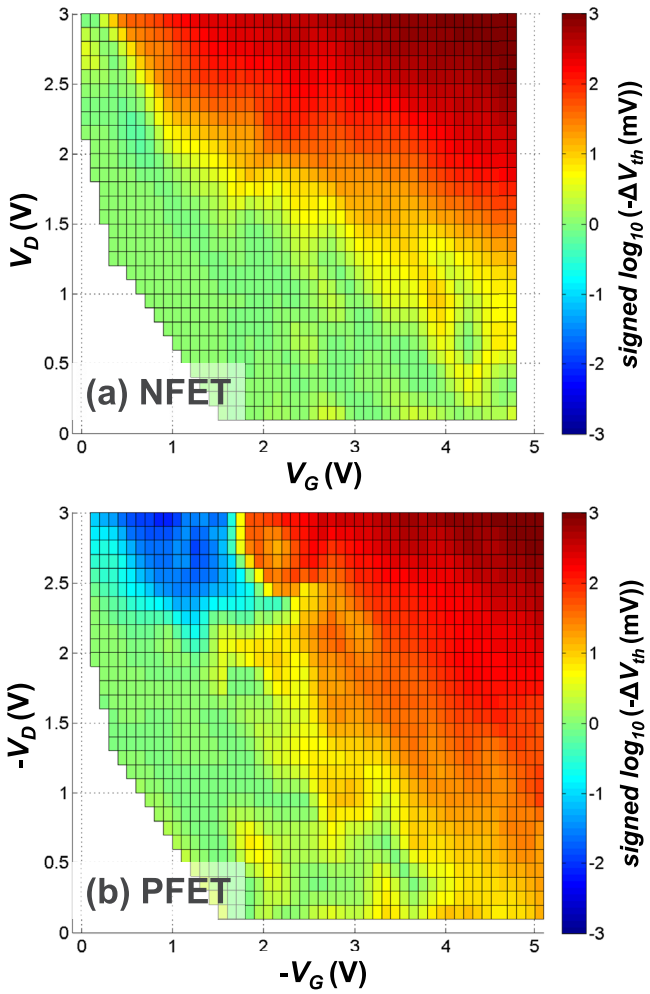

FIG. 5. (Color online) Degradation of threshold voltage V_{th} in (a) nFETs and (b) pFETs after 100 s, plotted vs (V_G, V_D). Note pFET ΔV_{th} changes sign between the OSS and HCD regimes.

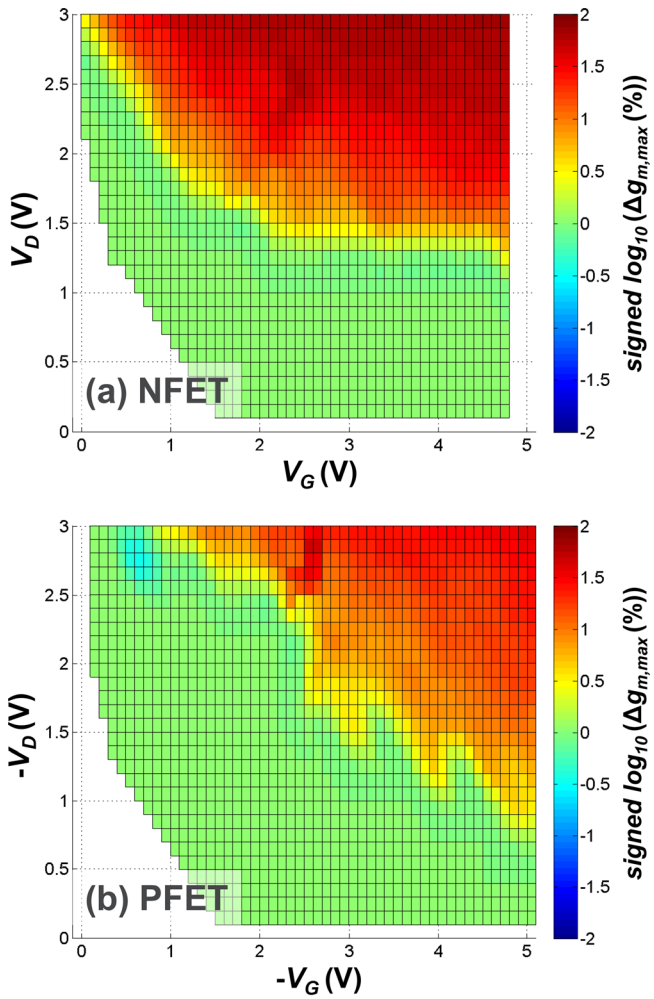

FIG. 6. (Color online) Degradation of maximum transconductance $g_{m,\max}$, normalized to the value before stress, in (a) nFETs and (b) pFETs after 100 s, plotted vs (V_G, V_D).

law with exponent α (Fig. 2). Fits of all quantities x at cumulative $t_{stress} = 100$ s are plotted for all (V_G, V_D) combinations (V_G and V_D step size = 0.3 V) and interpolated into contour plots. Function sign(x).log$_{10}|x|$, where $|x| < min\_value \rightarrow x = min\_value$ is used to visualize data where applicable.

III. RESULTS AND DISCUSSION

Figure 3 illustrates the typical contour plots resulting from the mapping of the entire applicable (V_G, V_D) space. Specifically, the figure shows the substrate current I_B extracted from unstressed devices at each (V_G, V_D) condition for both n and pFETs. The substrate current is a measure of impact ionization, which itself is indicative of the channel hot carrier energy.[16,17] Clearly, the channel carrier energy increases with increasing $|V_D|$, while the channel carriers remain "cold" in the BTI regime ($|V_G| \sim V_{DD}$, $V_D \sim 0$ V).

The efficiency of hot carrier generation (hot carrier generation per channel carrier) can be assessed through the multiplication factor $|I_B/I_S|$, shown in Fig. 4.[17] It is apparent that the generation is the most efficient in the OSS regime ($V_G \sim 0$ V, $|V_D| \sim V_{DD}$).

Figures 5–7 show the degradation of three important FET metrics: the threshold voltage $V_{th,}$ the maximum transconductance $g_{m,max}$, and the subthreshold slope SS. From Figs. 5(a), 6(a), and 7(a), negligible positive BTI ($V_G \sim V_{DD}$, $V_D \sim 0$ V) degradation is apparent in the nFETs. This is understandable given the limited stress at room temperature. Some negative BTI (NBTI; $V_G \sim V_{DD}$, $V_D \sim 0$ V) degradation due to hole trapping is, however, already apparent in the pFETs [Fig. 5(b)]. It is also evident that NBTI still takes place at $|V_D| > 0$ V, as the degradation extends above the horizontal (V_G) axis [Fig. 5(b)]. Neither maximum transconductance nor subthreshold slope is affected [Figs. 6(b) and 7(b), respectively].

Strong HCD ($|V_G|$ and $|V_D| \sim V_{DD}$) degradation is visible in both n and pFETs (Figs. 5–7), partially due to the FET junctions not having been optimized to reduce the lateral electric field. The HCD degradation tracks the maximum substrate current I_B (Fig. 3) for this channel length for both channel polarities. Degradation due to both gate oxide bulk charge trapping and interface state generation can be inferred, respectively, from ΔV_{th} (Fig. 5) and ΔSS, $\Delta g_{m,max}$ (Figs. 6 and 7). The observed maximum ΔV_{th} of ~1 V corresponds to an effective bulk trap density of ~4×10^{12} cm^{-2} (equivalent interface charge sheet) in the investigated gate stack, while the maximum ΔSS of ~10 mV/dec corresponds to an interface state density of ~6×10^{11} cm^{-2}.

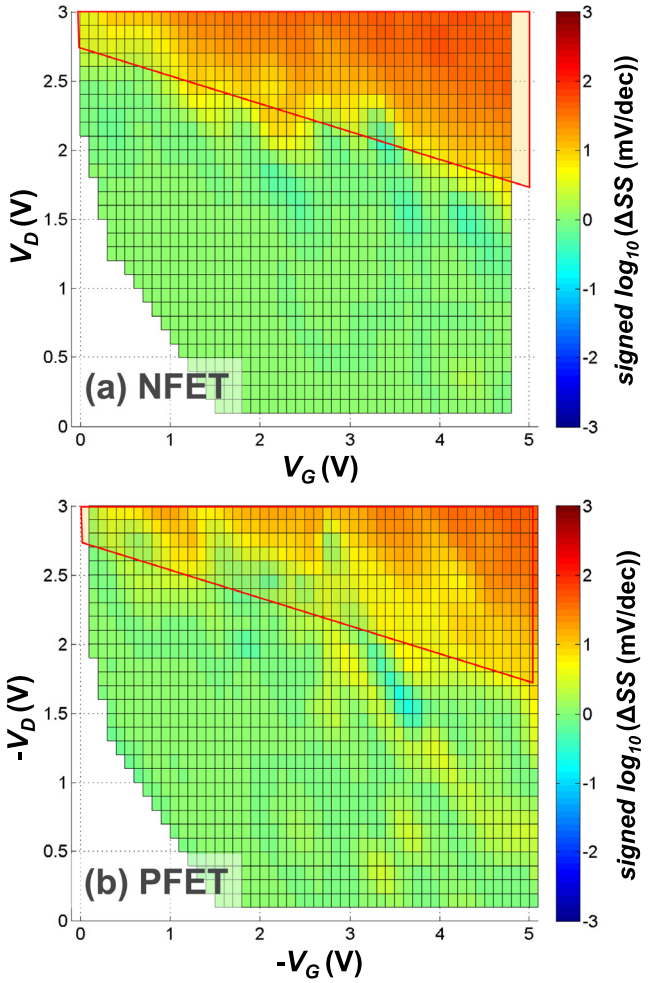

FIG. 7. (Color online) Degradation of subthreshold slope SS in (a) nFETs and (b) pFETs after 100 s, plotted vs (V_G, V_D). Parts of (V_G, V_D) space showing degradation are demarcated.

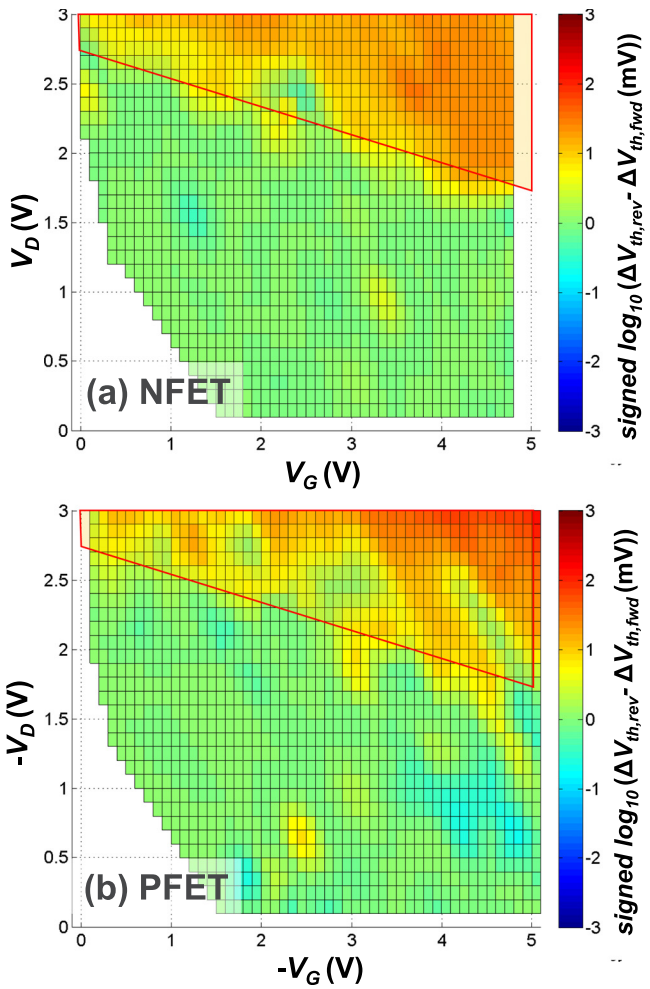

FIG. 8. (Color online) Localized degradation in (a) nFETs and (b) pFETs after 100 s, plotted vs (V_G, V_D), inferred from $\Delta V_{th,rev} - \Delta V_{th,fwd}$.

Localization of the damage at the drain side in the HCD and OSS regimes can also be discerned from the nonzero difference of reverse and forward ΔV_{th}'s in Fig. 8.[18] This particular quantity is sensitive to nonuniform charge formation in the channel. Clearly, a uniformly degraded FET will manifest the same ΔV_{th} when measured in either source/drain direction (cf. Sec. II) and hence $\Delta V_{th,rev} - \Delta V_{th,fwd}$ in such a case will be $\sim$0 V, as is indeed the case outside the demarcated (V_G, V_D) space in Fig. 8. In contrast, nonzero $\Delta V_{th,rev} - \Delta V_{th,fwd}$ will indicate nonuniform trap generation and charge trapping along the FET channel (at the drain side in our case).[18] Note that the demarcated (V_G, V_D) spaces in Figs. 7 and 8 are identical, likely indicating a common degradation mechanism.

The stress-time power-law exponent α (cf. Fig. 2) can be evaluated only for the nFETs [Fig. 9(a)]. The largest nFET α values in Fig. 9(a) are observed in the delineated (V_G, V_D) region. At higher V_D's, substantial ΔV_{th} shifts are reached [cf. Fig. 3(a)] and saturation (i.e., a "deceleration") of the HCD t_{stress}-dependence takes place [cf. Fig. 9(a)]. Consequently, the values of α are decreasing there.

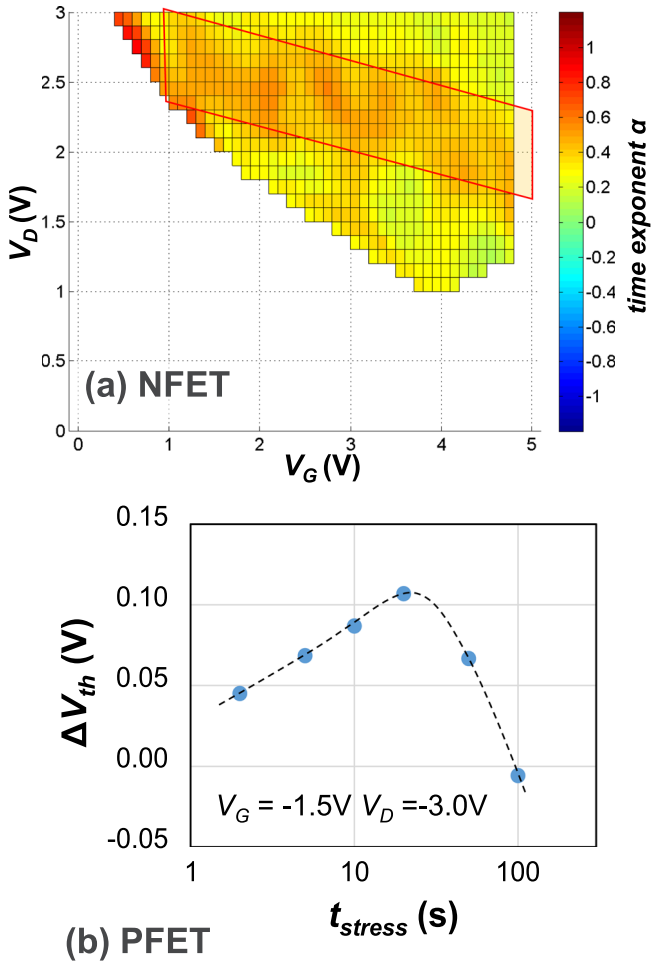

FIG. 9. (Color online) (a) nFET time power-law exponent α can be plotted in the entire (V_G, V_D) space since $\Delta V_{th} > 0$ V (areas with $\Delta V_{th} \sim 0$ V are suppressed in the plot). The region of (V_G, V_D) space with large α is delineated. (b) An example of pFET time dependence in the OSS/HCD range of biases shows two opposite-polarity mechanisms taking place, preventing power-law fitting.

In contrast to the nFETs, two concomitant opposite-polarity mechanisms take place in the pFET [Fig. 9(b)] between the OSS and HCD regimes [cf. Fig. 5(b)], preventing the extraction of α.[19] The additional mechanism is responsible for severe OSS ($V_G \sim 0$ V, $|V_D| \sim V_{DD}$) degradation in the pFETs, compared to the considerably weaker, albeit non-negligible OSS degradation in the nFETs [Figs. 5(a), 6(a), 7(a)]. The large positive ΔV_{th} shifts in the OSS region of the pFET (V_G, V_D) space [Fig. 5(b)] indicate that electron trapping is taking place in addition to channel hole trapping.[7] The trapped electrons are generated by impact ionization of channel holes in the drain region of the pFET. Recall that in the OSS regime the efficiency of this process is maximum [Fig. 3(b)].[20] We note that the final degradation can be calculated provided that the time dependences of both concomitant degradation mechanisms are properly modeled at each (V_G, V_D) combination.[21]

Finally, an example of postprocessing the data is shown in Fig. 10. Since the degradation data have been collected over the entire applicable (V_G, V_D) space, arbitrary "cut lines" can be taken in the space and the voltage acceleration of a given quantity can be extracted [Figs. 10(b)–10(d)] using a simple interpolation. The same methodology can be

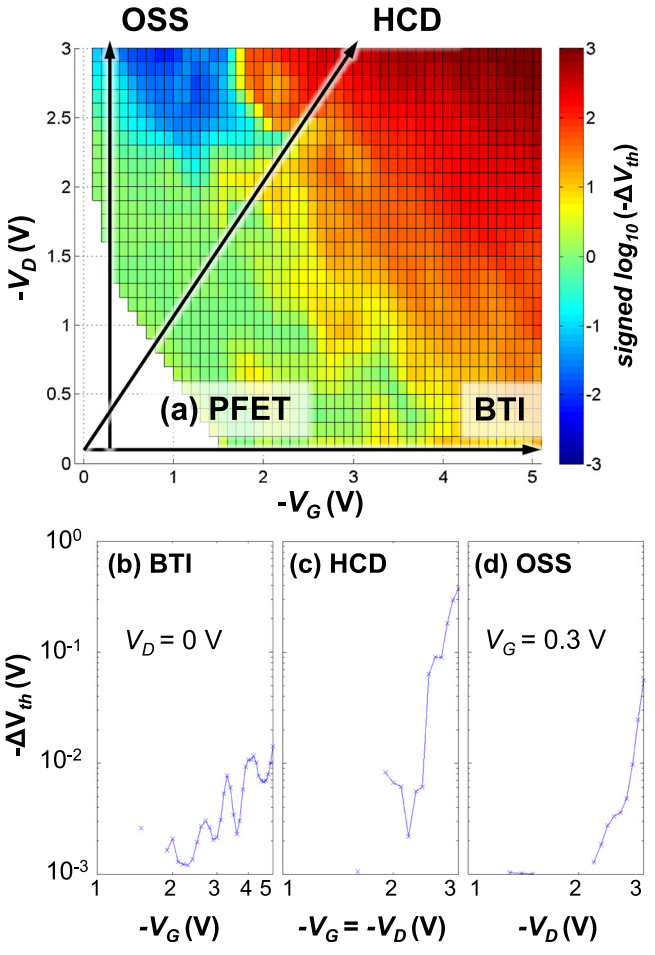

FIG. 10. (Color online) (a) When a given degradation-monitor quantity [e.g., ΔV_{th} from Fig. 5(b)] is collected over the entire applicable (V_G, V_D) space, its voltage acceleration can be extracted along any cut line. Values of ΔV_{th} pertaining to (b) BTI, (c) HCD, and (d) OSS cut lines are shown.

applied when comparing multiple technology options. In that case, however, the V_G axis and the given quantity have to be rescaled according to their respective V_{th} and EOT values or the electric fields, extracted, e.g., from the corresponding split C-V curves.

IV. CONCLUSIONS

In summary, mapping and visualization of all degradation modes in both n and pFETs has been performed in the applicable (V_G, V_D) bias space using a large number of nominally identical devices. This approach allows for studying all degradation regimes in parallel. The individual degradation regimes have been discussed here. This all-in-one approach should prove beneficial when developing new VLSI technologies, since it allows for simultaneous comparison and checking of all degradation regimes and promptly identifying weak spots of each technology option and postprocessing the data as necessary at a later time.

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