Superior NBTI in High-k SiGe Transistors–Part II: Theory

M. Waltl, G. Rzepa, A. Grill, W. Goes, J. Franco, B. Kaczer, L. Witters, J. Mitard, N. Horiguchi, and T. Grasser

***Abstract*— The susceptibility of conventional silicon p-channel MOS transistors to negative bias temperature instabilities (NBTIs) is a serious threat to further device scaling. One possible solution to this problem is the use of a SiGe quantum-well channel. The introduction of a SiGe layer, which is separated from the insulator by a thin Si cap layer, not only results in high mobilities but also superior reliability with respect to NBTI. In part one of this paper, we provide experimental evidence for reduced NBTI by thoroughly studying single traps in nanoscale devices. In this paper, we present detailed TCAD simulations and employ the four-state nonradiative multiphonon model to determine the energetical and spatial positions of the identified single traps. The found trap levels agree with the defect bands estimated in large-area devices. Our conclusions are also supported by the observation of similar activation energies for defects present in transistors of various device geometries. From the calibrated TCAD simulations data, an impressive boost of the time-to-failure for the SiGe transistor can be predicted and explained.**

***Index Terms*— Defect modeling, device simulation, negative bias temperature instability (NBTI), pMOSFET, reliability, SiGe.**

I. Introduction

THE device time-to-failure of modern MOS field effect transistors (MOSFETs) is seriously affected by bias temperature instabilities (BTIs) [1], [2]. Defects present in the gate-stack of the MOSFETs can exchange charge carriers either with the conducting channel or the gate during normal device operation. Charge trapping at electrically active sites affects the threshold voltage of transistors. For instance, complex circuits using MOSFETs rely on certain ON- and OFF-biases; hence a shift in the threshold voltage of a single transistor, which implicates a change in its operating regime, can be harmful to the proper operation of the entire circuit. Thus a detailed knowledge of the trapping kinetics of individual defects causing negative BIT (NBTI) is vital to correctly understand transistor operation in circuit design.

To further enhance the MOSFET performance, SiGe quantum-well devices have been fabricated [3]–[5] [see Fig. 1 (inset)]. Initially developed to take advantage of the higher carrier mobility of the strained SiGe layer, it was found that NBTI is considerably smaller in these devices [3], [6]–[10]. A strong dependence of the absolute threshold voltage shift on the Si passivation (Si cap) layer thickness together with a stronger oxide field acceleration with respect to Si devices was reported. It has been speculated

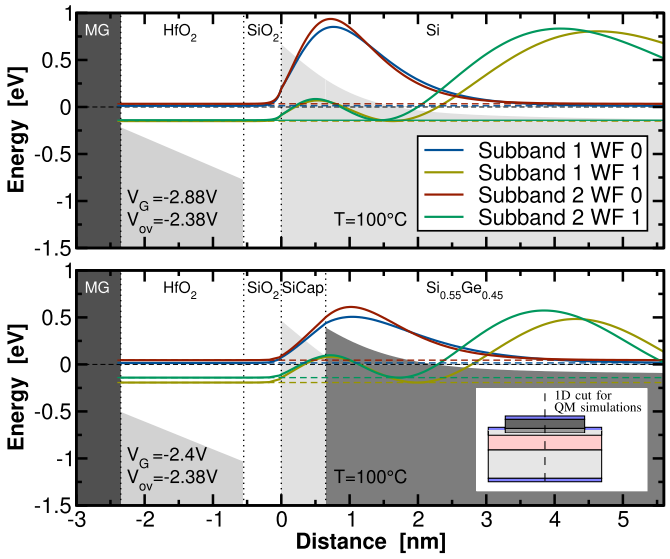

Fig. 1. Band diagrams of (**top**) the reference device and (**bottom**) the device with $d_{\mathrm{SiCap}} = 0.65$ nm (shown in the inset [13] at stress bias conditions). The WFs of the corresponding subbands highlighted are calculated with our Schrödinger–Poisson solver. Note that for the SiGe device, the peaks of the WFs are located in the SiGe and near the SiGe/Si cap interface. Consequently, the current is dominantly located inside the SiGe layer. In contrast, for the reference device, the peaks of the WFs, and as a consequence, the conducting channel are closer to the SiO_2/Si interface. This observation is very important, because the closer the traps are to the channel, the larger the step heights are, compared with the CCDF presented in part one [13]. As the device variants have different threshold voltages, the band diagrams are calculated at the same overdrive voltage in order to obtain compareable carrier concentrations in the inversion layer.

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that these observations are a consequence of the energetical realignment of the SiGe channel with respect to the dielectric stack [6], [11]. As the previous observations were made on large-area devices, a microscopic justification was difficult to give. On large-area devices, the average response of a large number of traps is unavoidably studied, thereby obscuring the contribution of the individual traps [12]. However, to provide a more detailed understanding of this phenomenon, the impact of the individual constituents has to be studied.

As has been demonstrated in the first part of this paper, the contribution of single defects can be studied in detail by applying the time-dependent defect spectroscopy (TDDS) to nanoscale transistors, which just contain a numerable number of defects [13]–[15]. This allows for a detailed study of CETs of single defects and their impact on ΔV_{th} as well as monitoring their temperature and bias dependence. Furthermore, as both the number as well as the impact of single traps on the threshold voltage can be studied, a much clearer interpretation of the average threshold voltage shift can be given. So far, the TDDS has been applied to conventional p-channel and n-channel MOSFETS with SiON gate dielectrics [14], [16] as well as to high-k gate-stacks [17]–[19]. In this paper, we apply it to novel SiGe channel pMOS transistors to shed light on the reduced NBTI degradation observed in these devices. To explain the observed charge capture and emission process, the four-state nonradiative multiphonon (NMP) model is used here, which was recently suggested for oxide defects dominating the recovery after stress [14].

The first part of this paper on SiGe devices [13] covers the experimental characterization of large-area and nanoscale SiGe pMOSFETs, whereas the focus of this paper is put on device simulation and explanation of our experimental data, extending our previous SiGe investigations [20]. By probing nanoscale devices, 23 single traps have been identified and their bias- and temperature-dependent CETs recorded. In addition, the recovery of large-area devices subjected to NBTI stress with different stress biases and stress times is recorded and discussed in part one [13]. Furthermore, negligible differences in the average step height of hundreds of traps and a similar bias dependence of the capture times were observed for the different device variants. However, a considerable reduced trap density is found for the devices with a Si cap layer of reduced thickness. In this paper of our SiGe study, we perform detailed TCAD simulations and demonstrate that the observed reduced trap density is due to a narrower active energy region (AER) for traps in the gate-stack. The narrow AER is thereby a consequence of the additional band offset between the conducting channel in the SiGe and the interfacial layer. Using the four-state NMP model, the energetical and spatial positions of the identified single traps are found to agree with the defect bands of the large-area devices confirming our explanation for reduced charge trapping visible in our SiGe devices. Additional evidence is provided by the observation that similar activation energies are extracted for defects present in all device geometries. Finally, the superior NBTI is confirmed by our lifetime prediction, showing a considerably improved lifetime is expected for SiGe transistors.

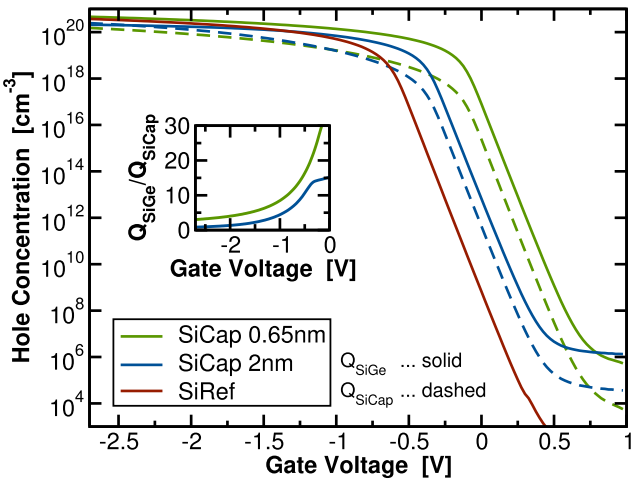

Fig. 2. Hole concentration for the Si cap layer and the SiGe layer is calculated at different gate biases from our QM simulations. As can be seen, the charge present in the SiGe layer exceeds the charge of the Si cap layer, confirming the channel to be more likely located in the SiGe. The inset gives the ration between the charge in the SiGe and Si cap layers. With increasing Si cap layer thickness, the channel in the SiGe is less pronounced, a behavior that weakens the superior NBTI of the SiGe devices.

II. Quantum-Mechanical Device Simulations

As the thin SiGe channel underneath the cap layer requires careful consideration, we begin our theoretical study with detailed quantum-mechanical simulations. For this, we use our QM Schrödinger–Poisson solver VSP to calibrate the device structures to the experimental $C(V)$ characteristics of the large-area devices with $W \times L = 10\ \mu\text{m} \times 10\ \mu\text{m}$ [21]. This is achieved by thoroughly inverse modeling of the unknown individual layer thicknesses as well as the bulk and channel doping to reproduce experimental $C(V)$ characteristics. For these simulations, a simplified 1-D structure represented by a cut perpendicular to the conducting channel is used [see Fig. 1 (inset)]. Note that, we simulated trap-free $C(V)$ characteristics as no traps were required to reproduce the experimental data. The band structure and the wavefunctions (WFs) of the first two subbands of the reference device and the device with the thinnest Si cap layer are shown in Fig. 1. Furthermore, the charge separately calculated for the SiGe and Si cap layer at different gate biases for the different device variants is notably larger inside the SiGe layer than in the Si cap layer [see Fig. 2]. This result confirms that the channel is primarily in the SiGe layer. As will be shown in the following, the prevalent channel inside the SiGe layer is the cause for the reduced susceptibility of the SiGe device to NBTI.

III. Classical Device Simulation

Based on the device structure obtained from the 1-D QM simulations, the 2-D device structures of the pMOSFETs are created. For this purpose, we use our classical device simulator Minimos-NT [22] to calculate the electric potential and the carrier concentrations by solving a quantum-corrected drift-diffusion model [23]. As can be seen from Fig. 3, the simulations performed using the calibrated 2-D devices nicely reproduce the experimental $I_D(V_G)$ characteristics.

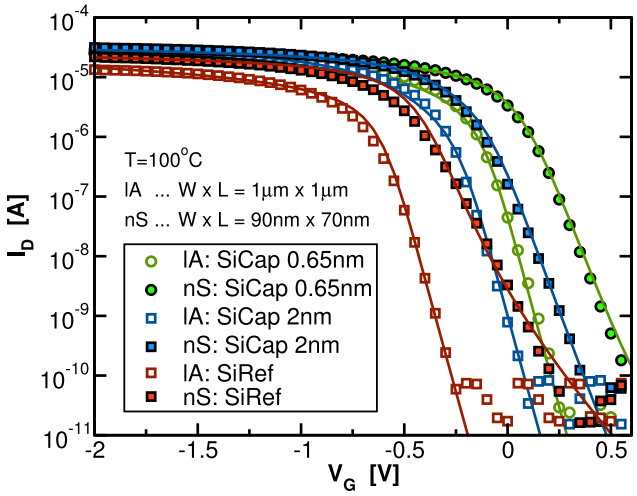

Fig. 3. Measured $I_D(V_G)$ characteristics of the large-area (open symbols) and the nanoscale pMOSFETs (closed symbols) can be nicely reproduced by using our device simulator Minimos-NT. This has been achieved using the same device structure with the corresponding Si cap layer thicknesses and an appropriate gate area.

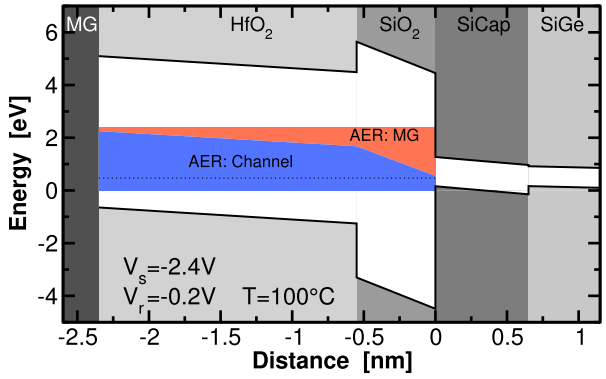

Fig. 4. Band diagram of the SiGe transistor with $d_{\mathrm{SiCap}} = 0.65$ nm is shown with the corresponding AER calculated for a stress bias of $V_G^s = -2.4$ V and a recovery bias of $V_G^r = -0.2$ V. As can be seen, the AERs are separated into an area, which can exchange their charge with the MG (red) and in an AER (blue) for charge exchange with the conduncting channel. As NBTI is observed to be significantly lower in SiGe devices compared with the reference transistor, a smaller number of traps have to contributed to the ΔVth. To illustrate the reduction of the number of active traps, the energetical position of the conducting channel at the Si cap/SiGe interface is shown in the AER (dotted line).

The band diagram in Fig. 4 shows the valance and conduction band edges together with the corresponding AER for charge trapping at stress bias conditions [24]. It is a necessary condition for a single trap contributing to NBTI that at defined stress and recovery bias conditions, the trap is energetically located inside such an AER, because only those traps can become charged during stress and become uncharged during recovery. The borders of the AER are defined by the stress and recovery gate bias under consideration. Thus at stress bias conditions, the energetic level E_T of a trap located at x_T inside the gate-stack has to lie above the corresponding Fermi level E_F

$$E_T + qV_G^s - q\phi^s(x_T) > E_F \tag{1}$$

and below the Fermi-level at recovery bias conditions

$$E_T + qV_G^r - q\phi^r(x_T) < E_F \tag{2}$$

with $\phi^s(x)$ and $\phi^r(x)$ are the position dependent potential drop across the gate-stack for stress and recovery bias conditions, respectively. By using these relations, the AERs are calculated according to the electric field during stress and recovery. Furthermore, the AER region can be separated into an AER for charge trapping from the MG and into an AER for charge trapping from the conduction channel. Both AERs can be described using (1) and (2) with its corresponding Fermi levels. Additionally, the energy level of the conducting channel located in the SiGe, which is by itself determined by the d_{SiCap} dependent band offset between the Si cap and SiGe, is visible in the AER in Fig. 4. As our QM simulations reveal that the carrier concentration is considerably larger in the SiGe than in the thin Si cap layer, only a very week contribution to charge trapping is expected from the carriers in the Si cap. As a consequence, we primarily attribute charge trapping in these devices to an interaction between defects and the channel prevalent in the SiGe. Thus, for our thin Si cap devices, we can consider the channel Fermi-level at the Si cap/SiGe interface as the energy level, which defines the effective AER. As a consequence, as the Fermi-level is higher in energy in SiGe as compared with Si and thus farther away from the defect band, a reduction in NBTI is expected, which is fully consistent with our experimental data presented in part one [13] of this paper.

IV. Modeling of Charge Trapping Using the Four-State NMP Model

To explain the intricate CETs of defects in HKMG p-channel SiGe transistors, we employ the four-state NMP model incooporated in our device simulator Minimos-NT to calculate the NMP transition rates. Afterward, the defect parameters of the four-state NMP model are adjusted to reproduce the experimental CETs of the single defects [20]. In the particular context of our SiGe devices, it was found to be of utmost importance that the four-state NMP model not only considers the charge exchange with the *conducting channel*, but also with the *metal-gate*, as recently demonstrated for very thin oxides [25].

In all single trap investigations, the bias dependence of the capture time plays an important role as it is determined by the trap depth. According to the NMP model, the charge capture time is given by

$$\tau_c = \tau_{12'} + \tau_{2'2}\left(1 + \frac{\tau_{12'}}{\tau_{2'1}}\right) \tag{3}$$

with τ_{ij} the first passage times between the individual states [24]. Considering the transitions $1 \rightarrow 2'$ and $2' \rightarrow 1$ as NMP barriers and the transition $2' \rightarrow 2$ as a thermal barrier, the capture time dependence on the stress bias is

$$\frac{\partial \tau_c}{\partial V_G^s} = -\beta q \underbrace{\frac{\partial \phi(x, V_G^s)}{\partial V_G^s}}_{\phi'(x, V_G^s)} \left(\frac{1}{2}\tau_{12'} + \tau_{2'2}\frac{\tau_{12'}}{\tau_{2'1}}\right) \tag{4}$$

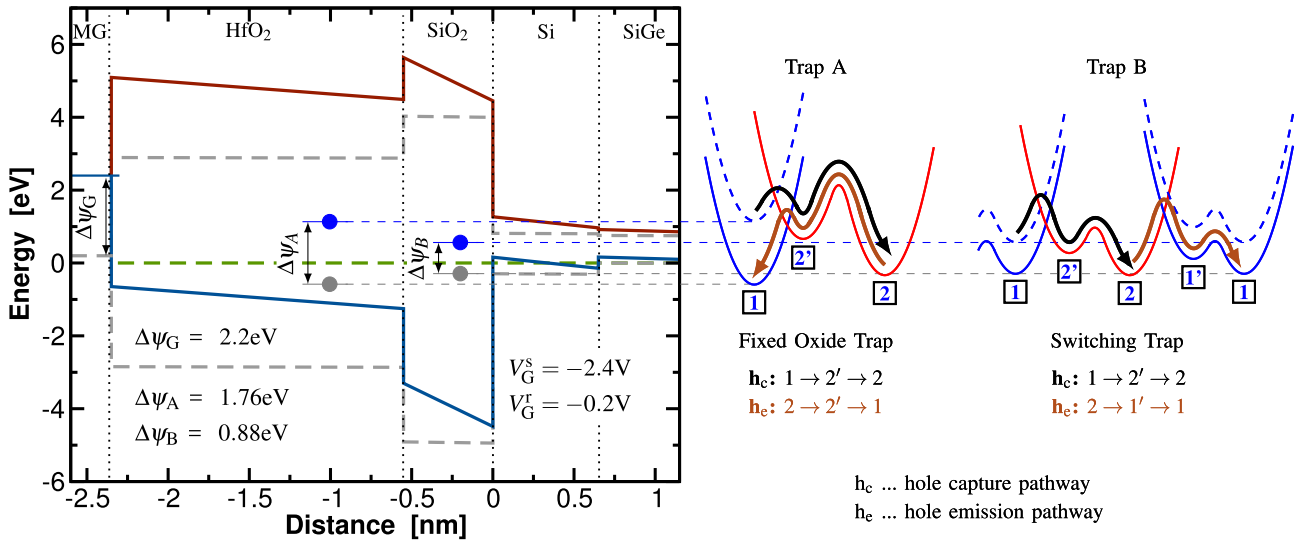

Fig. 5. At the left, the band diagram is shown for stress (colored solid) and recovery bias conditions (gray dashed) together with two exemplarily traps, one located in the HK (Trap *A*) and one in the IL (Trap *B*). The trap energy levels are shown for recovery (gray symbols) and stress bias conditions (blue symbols), respectively. When the gate bias changes from $V^r_G = -0.2$ V to $V^s_G = -2.4$ V, the trap levels change by ${}_1\psi_A$ and $\Delta\psi_B$; however, ${}_1\psi_A \not\propto {}_1\psi_B$, hence, a depth dependent change in the trap level is obtained. This causes a position-dependent relation between stress bias and the capture time. It turns out that the stronger the capture time depends on the stress bias, the closer the trap is located to the MG. Furthermore, the configuration coordinate diagrams for the fixed charge trap and the switching trap are shown on the right. Note that these are *exemplary* cases, as we found switching and fixed traps in both, the HK and IL.

with $\beta = 1/(k_B T)$ and $\phi(x, V^s_G)$ the potential inside the gate-stack. For the employed gate-stack we get

$$\phi'(x, V^s_G) = \begin{cases} x \le d_{\mathrm{SiO_2}} & 1/(1+\alpha^{-1}) \times x/d_{\mathrm{SiO_2}} \\ x > d_{\mathrm{SiO_2}} & 1/(1+\alpha^{-1}) + 1/(1+\alpha) \\ & \quad \times (x - d_{\mathrm{SiO_2}})/d_{\mathrm{HfO_2}} \end{cases}$$

with $\alpha = (d_{\mathrm{HfO_2}}/d_{\mathrm{SiO_2}})(\epsilon_{\mathrm{SiO_2}}/\epsilon_{\mathrm{HfO_2}})$, whereas $x = 0$ is at the IL/Si cap interface. The farther the trap is away from the IL/Si cap interface, the larger $\phi'(x, V^s_G)$ becomes and $\partial\tau_c/\partial V^s_G$ increases. Thus for a strong bias dependence of the capture time, the trap must be located more closely to the MG, and in case of a weaker bias dependence, the trap resides near the Si cap layer [see Fig. 5]. For all device variants, no correlation between the bias dependence of the capture time and the Si cap layer thickness has been found among our 23 single defects [13]. Thus a similar trap depth distribution among the device variants must be present.

V. Results and Discussion

By probing transistors with SiON or SiO_2 gate dielectrics, BTI in large-area and nanoscale devices has been attributed to defects with similar atomic configuration. Thus once the trapping kinetics of single defects is known, the occurrence of BTI in large-area devices can be reproduced. In our particular case, we performed TDDS experiments to extract detailed bias- and temperature-dependent trapping kinetics of single defects in our SiGe device variants. In the following, the four-state NMP model is used to explain the extracted charge CETs. Afterward, the same model is applied to reproduce BTI measured in large-area SiGe devices.

A. Single Defects in Nanoscale Devices

From our TDDS investigations performed on three different device variants, a total number of 23 single defects have been identified. Among them, five *fixed hole traps* that are ~22% of all traps, with bias-independent emission times, and 18 *switching traps* that are ~78% of all traps, with strong bias-dependent emission times, are found. As a consequence, a suitable model, which properly explains charge trapping in such devices, has to be able to reproduce bias-independent and bias-dependent emission time characteristics. This cannot be achieved by using a simple two-state model, and thus the four-state NMP model has been used [14]. As can been seen in Fig. 6, the trapping kinetics of fixed hole traps and switching traps can be very well explained using the four-state NMP model. Furthermore, using our detailed TCAD simulations and the four-state NMP model, we obtain an estimate for the trap level and spatial trap position of our single defects, which will be presented in the following.

B. Continuous Recovery of Large-Area pMOSFETs

Next we study the recovery behavior of the large-area SiGe device variants with dimensions of $W \times L = 1\ \mu\mathrm{m} \times 1\ \mu\mathrm{m}$. As can be seen in Fig. 7 for the $d_{\mathrm{SiCap}} = 2$ nm and reference Si transistors, the recovery recorded at different stress biases and stress times can be nicely reproduced by our simulations. This is achieved by using the four-state NMP model considering around 50k defects with normally distributed NMP model parameters. Quite remarkably, the *same set of trap parameters* is used to capture the recovery of all three pMOSFETs. From the good quality of our fit, we conclude that the trap parameters are a property of the gate-stack rather that a property of the different channel layouts. It has to be noted that the NMP model parameters used to explain our single traps are well within the model parameter distributions used for the large-area counterparts. In agreement with the previously presented analysis of the AER for charge trapping, the device lifetime is solely determined by the band offsets in the channel/cap layer [6].

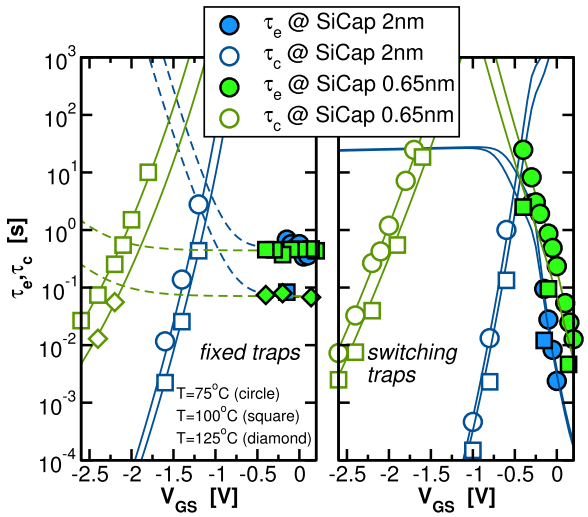

Fig. 6. Example of *fixed hole traps* (left) with their typical bias-independent emission times around the threshold voltage. In addition, *switching traps* with strong bias-dependent emission times are also found. The four-state NMP model reproduced the bias and temperature dependence of the CETs very well.

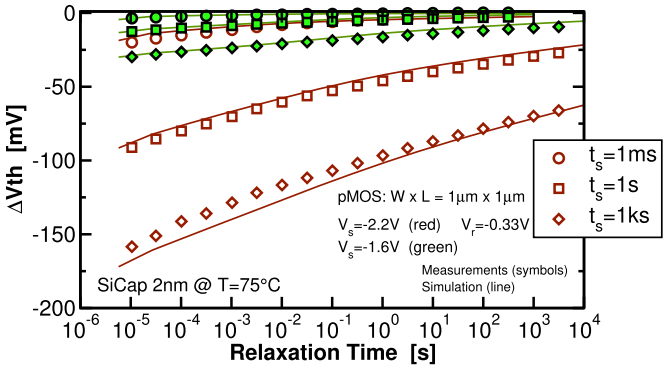

Fig. 7. Recorded recovery on large-area devices subjected to NBTI stress with increasing stress times and two different stress biases for the devices with $d_{\mathrm{SiCap}} = 2$ nm. The recovery characteristics for all the cases can be well described by our simulations and the four-state NMP model (not explicitly shown for the $d_{\mathrm{SiCap}} = 0.65$ nm and Si reference device variant). Furthermore, a considerably stronger stress bias dependence of the threshold voltage shift is visible for the devices with a SiGe quantum well, which is also explained by our simulations.

C. Nanoscale Versus Large-Area Devices

The energetical and spatial trap position of the 23 single defects identified in all our three technologies is shown in Fig. 8 together with the defect bands for traps used to describe the continuous recovery behavior of the large-area devices. Good agreement between the defect bands and the trap levels of our single defects confirms the accuracy of our results.

The atomistic origins of single defects found in SiO_2 and HfO_2 have been the subject of a wide number of experimental and theoretical studies. The most widely studied defects in SiO_2 fall into the E′ center family, first, identified experimentally by Weeks and Nelson [26] and characterized theoretically by Feigl *et al.* [27]. They typically consist of a three-coordinated Si with a dangling bond and come in a number of variants [28]–[30]. In addition, oxygen vacancies as well

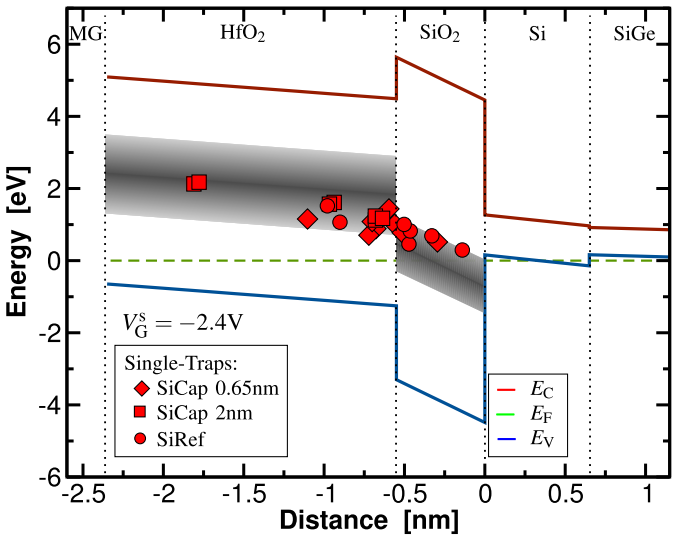

Fig. 8. Band diagram under stress bias conditions shows the trap bands used to explain the recovery of the large-area devices. Traps identified in the nanoscale devices are marked with larger symbols. It has to be noted that all single traps necessarily have a trap level above the the Si Fermi level when stress bias is applied and a trap level below the the Si Fermi level when recovery bias is applied. Otherwise the traps would not contribute to NBTI at the studied bias conditions. As can be seen, the single traps are found to be located in both the HK and the IL for all three studied device variants.

as intrinsic electron and hole traps have also been identified in SiO_2 [31], [32]. Among them, the hydroxyl E' center has been shown to be a promising candidate for hole defects in SiO_2 recently [33] using a similar TDDS setup. Since the hole traps identified in this paper are broadly consistent with our previous TDDS studies on Si/SiO_2 systems, we conclude that the hydroxyl E′ center is also a good defect candidate in the present SiGe devices. In HfO_2, the most widely studied defects are the oxygen vacancies [34]. Recent studies have shown that electrons and holes can also localize at intrinsic sites in *amorphous* HfO_2, creating deep polaronic states [35], [36]. All these defects produce localized states that sit in the band gap of the dielectrics and can interact with carriers flowing in the channel of a device.

Next, to study the distribution of the CETs, the CET maps of large-area devices can be calculated directly from the measurement data using [15]

$$g(\tau_c, \tau_e) \approx \frac{\partial^2 \Delta V_{\mathrm{th}}(\tau_c, \tau_e)}{\partial \tau_e \partial \tau_e}. \tag{5}$$

and compared with those obtained from simulations (see Fig. 9). As can be seen, the simulations reproduce the characteristics of the measurement data very well. According to (5), a narrow measurement window compared with simulations is achieved for the calculated CET maps due to experimental limits. Additionally, the CET data points from the analyzed single traps found are marked in the CET maps together with the measurement window used for our TDDS experiments on nanoscale devices. As can be seen, the extracted single traps lie well inside the CET distribution.

Based on the previous simulations, the effective activation energies for charge capture E_A^c and emission E_A^e are calculated (see Fig. 10). The continuous distribution shows the activation

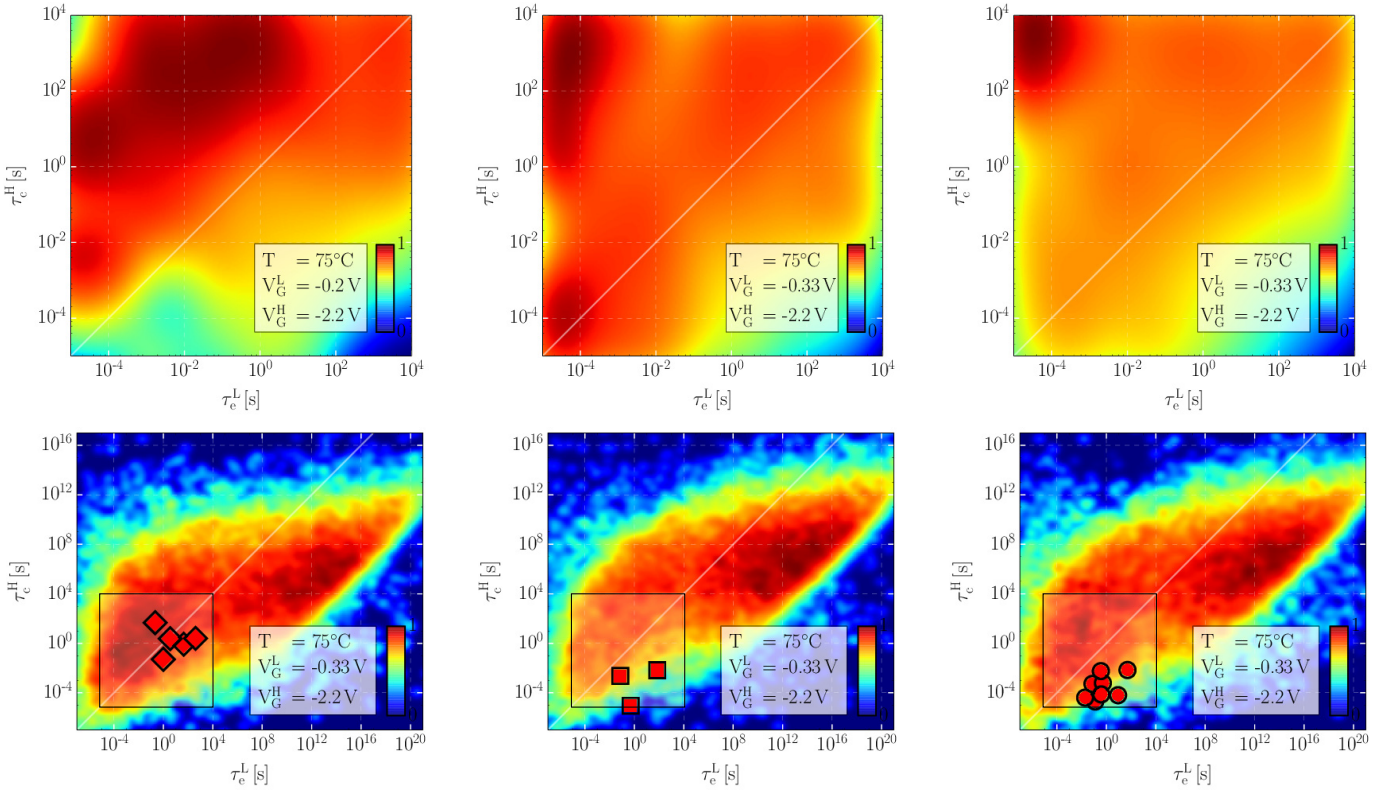

Fig. 9. CET maps calculated directly from the measured recovery traces (top row) and the CET maps obtained from our simulations (bottom row) are compared for the three different structures [d_{SiCap} = 0.65 nm (left), d_{SiCap} = 0.65 nm (middle), and the reference Si pMOSFET (right)]. For the simulated CET maps, the measurement window (the axis ranges of the measured CET maps) is highlighted. As expected, the characteristics of the measured CET maps are well reproduced by our simulations. Additionally, the single traps from the nanoscale devices are shown (symbols).

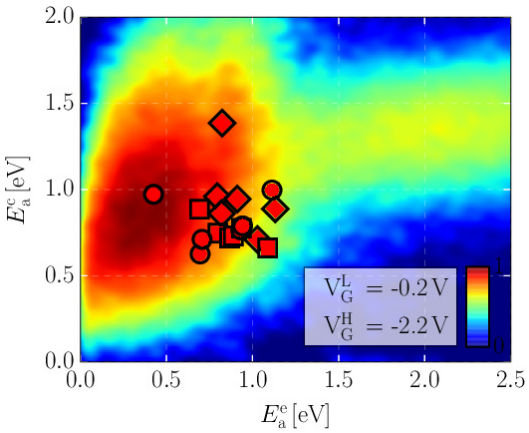

Fig. 10. Simulated thermal activation energy distribution calculated from the defects of the device with d_{SiCap} = 0.65 nm and symbols showing the activation energies of the single defects from the nanoscale transistors (*diamond* for d_{SiCap} = 0.65 nm, *square* for d_{SiCap} = 2 nm, and *circle* for reference pMOSFET). Single defects cover the same energy range as the simulated traps.

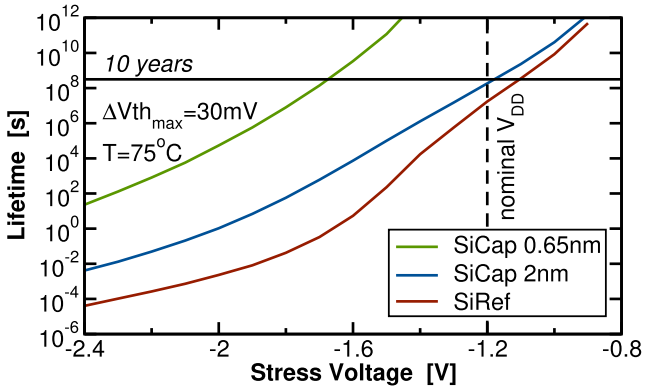

Fig. 11. Lifetime estimation based on the unified model is shown against the applied gate bias. Quite remarkably, at the nominal operating voltage of $V_{DD} = -1.2$ V, a lifetime of more than ten years is easily achieved for the SiGe devices. In particular, the devices with a thin Si cap layer have about four orders of magnitude higher lifetime although they show the lowest threshold voltage and thus have the highest overdrive voltage.

energies of the defect band used to explain the recovery of large-area SiGe devices. In addition, the activation energies from the single defect investigations are marked by symbols. As can be seen, both the distribution and the single data points are fully consistent. This confirms that a representative ensemble of single traps has been analyzed in this paper.

Finally, the device lifetimes can be extrapolated by using our calibrated TCAD model and is shown in Fig. 11. As can be seen, the SiGe devices with the thinnest Si cap provide a superior lifetime, easily outperforming the Si reference device. We underscore that this beneficial property is solely related to the favorable energy alignment shift of SiGe Fermi level with respect to the defect levels in the dielectric stack.

VI. Conclusion

To describe BTI in large-area and nanoscale SiGe transistors, the trapping kinetics of single defects are studied

in detail. Based on the experimental data presented in part one, we use our device simulator Minimos-NT to reproduce the electrostatics of three device variants with different Si cap layer thicknesses and a reference transistors. Our simulations demonstrate that the channel is indeed located deeply in the SiGe, provided a small Si cap layer is used. As a consequence, a considerably reduced AER is found for charge trapping for the transistor with the thin Si cap layer.

The CET characteristics of several identified single traps (*fixed* and *switching*) can be well explained by the four-state NMP model. In addition, we use the same model to reproduce the recovery behavior of large-area device variants with *the same set of trap parameters*, suggesting that charge trapping is solely determined by the energetic alignment of the defect band to the channel carriers.

Based on our simulations, we finally perform a lifetime projection, which clearly demonstrates that SiGe pMOSFETs with a reduced Si cap layer thickness provide superior lifetimes.

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Authors' photographs and biographies not available at the time of publication.