Thu-A-13:30

Comparative Soft Error Evaluation of Logic Cells in FinFET Technology

Laurent Artola[1], Guillaume Hubert[1], Massimo Alioto[2]
[1] ONERA - The French Aerospace Lab, France;
[2] National University of Singapore, Singapore

This work presents a comparative soft error evaluation of logic gates in bulk FinFET technology from 65- down to 32-nm technology generations. Single Event Transients induced by radiations are modeled with the MUSCA SEP3 tool, which explicitly accounts for the layout and the electrical properties of transistors. Good agreement between the calculated transient current, and TCAD mixed-mode simulations is demonstrated. This work allows for estimating the SER of such logic gates for ground applications, as well as for understanding the impact of voltage and drive strength through analysis of the sensitivity to soft errors.

Thu-A-13:50

A Quantitative Study of Phosphorus Implantation Damage on the thick Gate Oxide of the 28nm Node

Xinggong Wan[1], Sandhya Chandrashekhar[1], Boris Bayha[2], Martin Trentzsch[2], Torben Balzer[2], Mahesh Siddabathula[2], Oliver Aubel[2]
[1] GLOBALFOUNDRIES, United States;
[2] GLOBALFOUNDRIES, Germany

The tilted Phosphorous implantation has for a long time been adopted to form the lightly doped drain (LDD). For the first time, we report the implantation damage due to this on the thick gate oxide of the NMOSFET devices for 28nm technology. During the Time Dependent Dielectric Breakdown (TDDB) test, the breakdown time of the thick gate oxide of NMOSFET was found to be a function of implantation energy and dosage. In this work, an empirical model was established to characterize the implantation induced gate oxide lifetime reduction, which was correlated to the effective oxide thickness reduction. Our results showed that a careful implantation scheme needs to be chosen to balance the reliability requirements and the device performance for the scaled 28nm process and beyond.

Thu-A-14:10

Mixture of Negative Bias Temperature Instability and Hot-Carrier driven Threshold Voltage Degradation of 130nm technology p-channel Transistors

Gunnar Andreas Rott[1], Karina Rott[1], Hans Reisinger[1], Wolfgang Gustin[1], Tibor Grasser[2]
[1] Infineon Technologies AG, Germany; [2] Institute for Microelectronics, Technische Universität Wien, Austria

We present measurement results in form of threshold voltage drift plots, recovery traces and continuous capture emission time maps (CET maps) including Negative Bias Temperature Instability (NBTI) and Hot-Carrier driven Degradation (HCD). The measurements were performed on a 130nm MOS Transistor technology which is used for automotive and analog applications and has a nominal voltage of 1.5V. Devices of l = 100nm, w = 10µm have been stressed using a 2-dimensional parameter space of gate and drain voltage combinations at elevated temperature (125°C). The chosen stress conditions include the homogeneous (Vds = 0) and inhomogeneous (Vds << Vnom) NBTI case, the pure HCD (Vgs < Vnom) case as well as the mixture of NBTI and HCD. The results clearly show that for increasing Vds > Vnom NBTI recovery becomes less severe and mainly the permanent degradation due to HCD endures after the end of stress. Furthermore there is a drift minimum of NBTI observable for a specic Vds. Using CET maps it is quite evident that for high stress times the probability density of emission becomes very small whereas for shorter stress times there is a recoverable component notable.

Thu-A-14:30

Predictive evaluation of electrical characteristics of sub-22nm FinFET technologies under device geometry variations

Cristina Meinhardt, Alexandra Lackmann Zimpeck, Ricardo Reis
UFRGS, Brazil

This work evaluates the impact on ION and IOFF currents of variations in process parameters for a set of predictive FinFET technologies from 20nm to 7nm. The main contribution of the present study is to identify relevant behavioural standards with respect to the use of FinFET technology in digital designs. It is no longer enough to focus only on the threshold voltage fluctuations in the development of projects and EDA tools considering the FinFET technology. It is necessary that EDA tools and designers evaluate all electrical characteristics.

Reliability & Failure Mechanisms of Wide Bandgap Devices

Thu-B-08:30

Single Pulse Avalanche Robustness and Repetitive Stress Ageing of SiC power MOSFETs

Asad Fayyaz[1], Li Yang[1], Michele Riccio[2], Alberto Castellazzi[1], Andrea Irace[2]
[1] University of Nottingham, United Kingdom; [2] University of Naples Federico II, Italy

This paper presents an extensive electro-thermal characterisation of latest generation SiCPower MOSFETs under unclamped inductive switching conditions. Tests are carried out to thoroughly understand the single pulse avalanche ruggedness limits of commercially SiC MOSFETs and assess their aging under repetitive stress conditions. Both a functional and a structural characterisation of the transistors is presented, with the aim of informing future device technology development for robust and reliable power system development.

Thu-B-08:50

Effect of gate trench fabrication technology on reliability of AlGaN/GaN heterojunction field effect transistors

Sergey Shevchenko, Matthias Schulz, Eldad Bahat-Treidel, Wilfred John, Stephan Freyer, Paul Kurpas, Hans-Joachim Würfl
Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik (FBH), Germany

A comparison of reliability by means of mean-time-to-failure (MTTF) determined from three-temperature accelerated life time tests for two groups of AlGaN/GaN hetero-junction field effect transistors is presented. The two groups differ by gate trench fabrication technology, namely by RF bias and power levels used for the reactive ion etching of gate trenches in a SiNx layer. The extrapolated MTTF at Tchannel = 150 °C was found to be ~2.6e8 h and ~2.6e5 h for transistors with gate trenches etched using RF power/bias 30 W/100 V and 15 W/30 V, respectively. The experimental results are explained based on the outcomes of simulations performed using Silvaco-“Atlas” 2D semiconductor device simulator. The simulations revealed higher electric field at the corner of the gate on a drain side and increased electron concentration in the vicinity of gate for the group of transistors processed with lowered RF power/bias. We conclude that the electric field and amount of electrons stipulated reliability degradation.