Reliability Perspective of 2D Electronics

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Owing to the fascinating properties of 2D crystals, several attempts to fabricate field-effect transistors (FETs) with graphene [1-4], MoS_2 [5-7] and black phosphorus (BP) [8-9] channels, as well as with the 2D insulator hBN [7], have been undertaken recently. However, although a huge amount of funding has been already invested into 2D materials research, no commercial device technology is available by now. We argue that in addition to fabrication related issues, a fundamental problem for the transition from device prototypes to industrial 2D FETs is the lack of attention paid to their reliability, which has to be understood for any material system that is to acquire some technological significance. For example, in Si technologies a comprehensive reliability study is always a must for the integration and commercialization of new device designs. As such, it is to be expected that reliability of next-generation 2D FETs will become a hot research topic in the nearest future.

During the last few years we have examined various prototypes of graphene [3-4], MoS_2 [7] and BP FETs [9]. We found that the reliability of all these devices is dramatically affected by charge trapping in insulator traps situated within few nanometers from the 2D channel. Since these traps typically have widely distributed time constants, charge trapping results in both a hysteresis as well as slow drifts of the transistor characteristics under electrical stress. The latter is known as bias-temperature instabilities (BTI), and is also one of the most important reliability issues in Si technologies [10]. While we have found that the BTI degradation/recovery dynamics are surprisingly consistent with the defect models previously developed for Si devices (e.g. [10]), the typically measured shifts for 2D FETs are several orders of magnitude larger than for their Si counterparts (Fig.1a). We argue that this poor reliability of 2D devices can be due to both non-optimized processing conditions and the unfavorable combination of insulator and channel materials (e.g. MoS_2 with SiO_2). The latter is extremely important, since every insulator has certain defect bands. Quite obviously, for better device reliability the defect bands should be energetically far from the channel conduction/valence bands in the n/p-FETs, respectively. Furthermore, the currently available 2D FETs have very large device area, which leads to a large number of defects. Based on our results for different 2D systems, we found devices have to be scaled considerably to reach the single-defect limit (Fig.1b). This would allow for the very powerful characterization of individual defects [11], thus leading to further understanding and optimization of the reliability of these new device technologies.

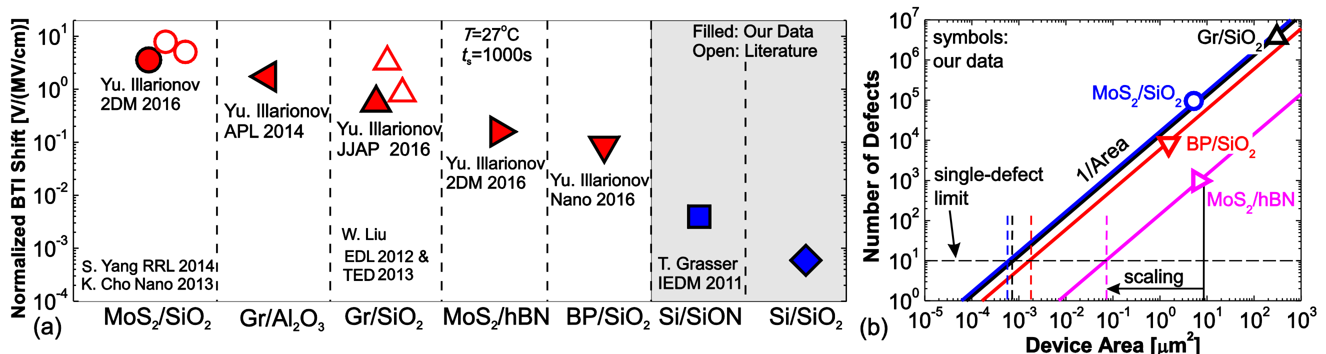

Fig. 1: *(a) The BTI degradation measured using the stress time t_s=1000s and normalized by the stress field for various 2D and Si FETs. (b) Extrapolated number of defects per device area, starting from our data.*

To summarize, our preliminary results demonstrate that the reliability of 2D FETs is currently not competitive compared to Si devices. In order to reach the threshold required for commercialization, the number of defects contributing to charge trapping issues has to be minimized, while the dynamics of unavoidable ones should be properly understood. To improve on this situation, combinations of 2D channels and insulators with maximally favorable defect band alignments have to be identified. Furthermore, devices have to be scaled towards the single-defect limit to allow for the characterization of individual defects.

[1] W. Liu *et al*, Electron Device Lett. **33**, 339 (2012). [2] W. Liu *et al*, Trans. Electron Devices **60**, 2682 (2013). [3] Yu. Illarionov *et al*, Appl. Phys. Lett. **105**, 143507 (2014). [4] Yu. Illarionov *et al*, Jpn. J. Appl. Phys. **55**, 04EP03 (2016). [5] S. Yang *et al*, Phys. Status Solidi RRL **8**, 714 (2014). [6] K. Cho *et al*, ACS Nano **7**, 7751 (2013). [7] Yu. Illarionov *et al*, 2D Mater. **3**, 035004 (2016). [8] J.-S. Kim *et al*, Sci. Rep. **5**, 1 (2015). [9] Yu. Illarionov *et al*, ACS Nano **10**, 9543 (2016). [10] T. Grasser *et al*, IEDM (2011). [11] T. Grasser *et al*, Phys. Rev. B **82**, 245318 (2010).