Study of (correlated) trap sites in SILC, BTI and RTN in SiON and HKMG devices

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ABSTRACT

Recently, several experimental groups have found correlations in gate and drain current fluctuations. In this paper, by studying single trap activated leakage paths, both evidence and a refined 4-state defect model are provided, ascribing additional gate tunneling current in nm-FETs to thermally activated defect states. The model is capable of explaining both positive and negative correlations in gate and drain current RTN, but also the mostly uncorrelated nature of these drain and gate RTN signals.

I. INTRODUCTION

Enormous CMOS device improvements have been achieved over the last few decades, both by scaling device dimensions as by reducing the equivalent gate oxide thickness. As a consequence of this, degradation and fluctuations in drain and gate leakage currents become more pronounced, even in a way that they could seriously affect device performance. Phenomena such as bias temperature instabilities and RTN have been extensively studied over the last years [1].

Studying these phenomena in nm-sized FETs can give insight in the underlying physical principles—it is well established that in small devices, charge trapping and detrapping of single defects can significantly alter the channel current, as shown in Franco et al.’s “ultimate” BTI experiment [2]. Also single leakage paths from the substrate to the gate electrode can be identified and extracted [3], as illustrated in Fig. 1. Finally, it has been shown [4-6] that correlated gate and drain current RTN exists in nFETs. Recently it was shown that even in one single device, both positive as negative correlations can be found [7].

A possible explanation for this latter phenomenon is the electrostatic screening in a direct tunneling model, affected by a discontinuous oxide banding. Conversely, it has been shown by [8] that electrostatic screening alone cannot alter the gate leakage current more than a few percent. Another theory based on trap-assisted tunneling (TAT) was proposed in [9] and [10], where a trap in the oxide acts as a (thermally activated) stepping stone for tunneling towards the gate electrode, as illustrated in Fig. 2.

This paper shows that the full $I_{GS}$ characteristics of individual trap site-induced leakage paths can be extracted and provides indications that trap-assisted tunneling can described with a refined 4-state defect model, in which the transition rates are crucial for describing all correlated gate leakage currents in nm-size FETs. Moreover, indications are given that most defects responsible for (de-)activating the SILC, also in HKMG devices, should be located in the SiO2 interfacial layer.

II. MEASUREMENT APPROACH

The measurements in this work were conducted on nanoscale nFETs (dimensions as indicated below) with SiON and HKMG gate stacks respectively. The stacks were specifically selected to have a comparable physical thickness. While the lateral dimensions of these devices are chosen small enough to increase the impact of single-defects on the drain current [2], the gate leakage current density has to be sufficiently high to be within measurement resolution at gate biases around the device’s threshold voltage. The FET currents were simultaneously measured with a pair of Keithley 2636 units, either with a voltage sweep or with a constant voltage at a rate of 10 samples/s. All the measurements reported here were performed at 25°C unless noted otherwise. The experimental procedures are depicted in Fig. 3. Experiment A reveals the properties of trapped-charge induced BTI-shifts, the voltage dependence of a single leakage path, and the effect of stress on the generation/activation of these gate leakage paths, whereas experiment B reveals the time-dependent characteristics and
only [Fig. 1(a)]. The latter can be found after scanning multiple devices. Note that the TAT-current is not necessarily stress-induced, but it can also be process-induced as shown for the initial IGVGs in Fig. 4. An inflected gate leakage current (thus with a TAT component) can be observed in both SiON as HKMG devices, but remarkably, it’s not observed substantially more in the latter, even though it’s known that the high-k and SiO2/high-k interface defect density is at least one order of magnitude higher. This is an indication that the enabling trap for the TAT is located in the SiO2 rather than in the high-k material, a conclusion similar to [11] and [12].

The voltage shift of the Id curves in the linear regime of the MOSFET when increasing V0 from 0 to 0.05V reflects the lateral position of the TAT path, as explained in Fig. 5. The linear drop of the channel potential influences the local field in the gate oxide, and thus the leakage current through the TAT-path, as shown in Fig. 1. Therefore, the ratio of voltage shift of this single TAT-path (ΔVIG_TAT) with the applied V0 thus determines the relative position of the trap in the channel:

\[ x_{\text{trap}} = \frac{I_{\text{channel}}}{\Delta V_{\text{IG,TAT}}} \frac{\Delta V}{V_0} \] (1)

This technique is a suitable alternative for the ‘s-ratio’ technique in inversion [13], which relies on the channel resistance differences between the leakage path and drain/source junction, which become unmeasurable in nanoscale and thus ultra-short FETs.

### IV. LINK WITH BIAS TEMPERATURE INSTABILITIES

The introduction of HKMG devices also leads to positive BTI, visible as a positive shift of the [\( I_{\text{d}} - V_{\text{g}} \)] characteristic. The TAT-paths after subsequent stresses are also influenced by the electrostatic charge accumulated in the oxide due to this BTI-induced charge trapping [Fig. 6(a)]. It is therefore necessary to compensate for this shift. This can be done trace by trace, as the channel current is measured simultaneously.

Our experiments cannot conclusively determine a correlation between the impact of the defects on the drain current (i.e. the position w.r.t. the percolation path) and the screening of the gate current: the trapped BTI-charges will have an electrostatic impact on the TAT-path, but not according to their impact on the Id, i.e. a trap close to a channel percolation path will not necessarily induce a large voltage shift on the TAT-path and vice versa.

However, based on BTI relaxation traces and simple charge sheet approximation (Fig. 6(a)), we can conclude that our HKMG devices (90x28nm) can easily contain a few tens of trapped charges after stress, and the ‘average’ BTI shift and IG shift are nearly equal, as shown in Fig. 6(b). Therefore, in these devices, correcting the IGVG traces with a ‘BTI’ shift measured on the drain, as shown in Fig. 7, is a crude yet useful fix, as it helps to reveal the smaller ΔIG TAT paths over the shifted background current.

Fig. 7(b) shows that the TAT-paths can both be induced or activated by stress, but also de-activated [Fig. 8(a)]. In some cases [Fig. 8(d)], the TAT-paths are activated and de-activated dynamically during the Id-Vg sweep. It is well known that the generation of defects and thus potential TAT-paths is gate bias dependent (a high stress voltage will induce new defects), but also the activation and de-activation of such a path can show a gate bias dependence during the sweep. For the case of Fig. 8(a)
Switching TAT-paths show RTN-like behavior if the gate leakage current is measured at constant bias, thereby proving that one trap can activate or de-activate these leakage paths. As the single path $\Delta I_G$ can be $\approx 2.5 \times 10^{-11} \text{A}$ [Fig. 8(b)], about 1.5x10^8 charges/s should be captured and emitted to the gate by the oxide trap. The slowest time constant in the inelastic TAT process (thus either $\tau_C$ and $\tau_T$) is thus the order of ns. The (in)elasticity of this tunneling current has no impact on the considerations in the proposed model.

At elevated temperature, the $I_G$ traces become unstable and vary between every sweep. This RTN-like $I_G$ is mostly not visible in $I_D$, Fig. 8(d) shows experiment A (Fig. 1) performed at a temperature typical for BTI experiments ($125^\circ\text{C}$). More charge trapping—observed as $V_{TH}$ shift in $I_D$—is apparent. Shifts up to 300mV are observed (not shown here), although the device remains fully functional.

Meanwhile, the gate leakage current is strongly increased to the point where the individual TAT-paths become indistinguishable. Their activation and de-activation time constants are strongly temperature dependent and decrease below measurement integration time, as predicted in the phonon relaxation model, and illustrated in Fig. 2 (b).

The results of experiment A and B show that PBTI of SiON is much lower than HKMG FETs. Typically, PBTI is attributed to defects in the high-k. In the latter, charge trapping occurs at much lower stress. Due to the defective nature of the high-k layer, phenomena as BTI and ID RTN are abundantly visible, thereby inhibiting individual characterization, but the TAT-paths remain similar.

V. GATE AND DRAIN CURRENT CORRELATION

$I_G$ and $I_D$ are measured simultaneously and $\Delta I_G/\Delta I_D$ correlations are well within the measurement window. For the devices tested, most discharging events in the drain show no

Our model, explained schematically in Fig 10, can describe no, positive and negative $I_G/I_D$ correlations for nFET devices, is consistent with the 4-state defect model as proposed by [14]. The no-correlation, which is mostly seen, is explained with an active TAT-path located near the channel. Even in its metastable position, the trap will have a net charge, as the time constant for inelastic tunneling from the channel towards the trap (1s $\rightarrow$ 2$'$) is slower than the time constant to tunnel from the trap towards the gate (2$'$ $\rightarrow$ 1g). The net charge is then defined by the product of the occupancy probability and the defect charge state. The trap’s de-activated complement state 2$'$ is by definition a charged defect state [Fig. 10(a)].

Therefore, no net charging in the oxide occurred whilst activating or de-activating the TAT-path.

Only the cases where the capture time is dominant (i.e. state 1s $\rightarrow$ 2$'$ is slowest, thus the trap located far from the interface) could show a positive correlation between $I_G$ and $I_D$, [Fig. 10]
negative ID and IG correlations. measurement observations, and in particular the positive and devices yields large insight in TAT/SILC, RTN and BTI mechanisms we propose a model capable of explaining the transition rate dependency of BTI parameters 

\[ \Delta I_D/I_G = 0 \]

\[ \Delta I_D/I_G > 0 \text{[4,7]} \]

\[ \Delta I_D/I_G < 0 \text{[5,6,7]} \]

\*Shieldline is determined by net charge – (occupancy probability) x (defect state charge)

(b)]. These correlations were already experimentally shown by \[4\] and \[7\] and are confirmed in these measurements.

Also the negative correlation observed earlier in [5–7] and now seen here, cannot just be explained with a TAT scheme and neither with direct electrostatic interaction. A plausible explanation for these correlations is by favorable transitions between the secondary defect states 1'g/1's and 2. The transition rates \( \tau_{tc} \ll \tau_{te} \) between the secondary states are 1) much shorter and 2) opposite in their magnitudes: \( \tau_{tc} \gg \tau_{te} \). The transition rate \( \tau_{tc} \) towards the secondary defect state has to be short as state 2’ is quasi unoccupied.

In both correlated cases, an indirect gate voltage dependence is expected ascribed to a change in occupancy probability of state 2’ influencing the 2’\rightarrow 2 transition, due to typical voltage dependency of BTI parameters \( \tau_{tc} \). This gate bias dependence can be further investigated with noise or RTN measurements.

**VI. CONCLUSIONS**

Extended analysis of currents on all terminals of nanoscaled devices yields large insight in TAT/SILC, RTN and BTI mechanisms we propose a model capable of explaining the measurement observations, and in particular the positive and negative \( I_D \) and \( I_G \) correlations.

**VII. REFERENCES**


