Characterization of Oxide Defects in InGaAs MOS Gate Stacks for High-Mobility *n*-Channel MOSFETs (*Invited*)

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Abstract**—**We review our recent studies of oxide traps in InGaAs MOS gate stacks for novel high-mobility *n*-channel MOSFETs. We discuss and correlate various trap characterization techniques such as Bias Temperature Instability, defect Capture-Emission-Time maps (applied here to InGaAs devices), Random Telegraph Noise, hysteresis traces, multi-frequency *C-V* dispersion, all performed on a variety of device test vehicles (capacitors, planar MOSFETs, finFETs, nanowires). Finally we demonstrate guidelines for developing sufficiently reliable IIIV gate stacks.

Introduction

High-mobility channel materials are considered for future CMOS nodes, as they can offer enhanced device performance at reduced voltage [1], and therefore reduced active power dissipation. For *n*-channel devices, IIIV materials offer a dramatic boost of electron mobility [2]. In particular, InGaAs also enables bandgap engineering by varying the In-to-Ga ratio. We have recently demonstrated $In_{0.53}Ga_{0.47}As$ devices in advanced VLSI-compatible architectures with performance almost on par with state-of-the-art Si devices but at a remarkably lower operating voltage (Fig. 1) [3-7]. Most commonly, Al_2O_3-based gate stacks are used on InGaAs, due to a surface self-cleaning effect of the relative ALD process [8].

An excessive interaction of carriers with oxide defects represents a crucial challenge for IIIV devices [9-11]. Various symptoms are observed in the device electrical characteristics (Fig. 2), e.g., frequency-dispersion of the capacitance-voltage (*C-V*) curve in strong accumulation [12]; instability of the device threshold voltage (V_{th}), subthreshold swing (*SS*), and transconductance (g_m) [9]; hysteresis in double-sweep *C-V* or I_D-V_G traces [13]; Random Telegraph Noise inducing abrupt jumps in nanoscale device *I-V's* [14]. While oxide defects are also observed and studied in Si devices [15], their impact is exacerbated in IIIV devices due to defective semiconductor-oxide interfaces, unsuitability of the semiconductor native oxides as interfacial layers [16], and process thermal-budget limitations affecting the quality of the high-k layers [17].

We first review the understanding of charge trapping in oxide defects based on Si literature. We then discuss Positive Bias Temperature Instability (PBTI) measurements in InGaAs devices, and compare the results with Si. We show that the PBTI signatures are common across all device architectures, while scaling introduces additional challenges such as quantization effects, Random Telegraph Noise and variability. We discuss the distribution of defect energy barriers, which dictates the charge trapping transients in Al_2O_3-based InGaAs gate stacks. We then discuss alternative characterization techniques, such as multi-frequency *C-V* dispersion and hysteresis, and correlate them to BTI. Finally we discuss our recent demonstrations of reliable gate stacks for InGaAs devices.

Charge Trapping in Oxide Defects

Based on the Si literature, the understanding of charge trapping in oxide defects can be summarized as follows (Fig. 3): distributions of allowed energy levels exist within the dielectric bandgap, originating from microscopic defects (e.g., hydroxyl *E'*-center in SiO_2, oxygen vacancies in high-k oxides). Depending on the position of the channel Fermi level, a fraction of these defects can (de-)trap carriers. Energy barriers are involved in the charge exchange process, related to the reconfiguration of the atomic bonds at the defect site, resulting in trapping being strongly temperature activated [$\tau_c \propto \exp(E_c/kT)$, $\tau_e \propto \exp(E_e/kT)$]. The process can be approx. represented as a two-parabolic-well system with *distributed* curvatures representing the spread of energy barriers within a population of defects in an amorphous oxide [15,18]. The behavior of an ensemble of defects can be described with a bi-variate Normal distribution of capture and emission energy barriers, which can be converted into the Capture-Emission-Time (CET) map observable at a given operating temperature [19,20,21]. This methodology is applied here for the first time to a typ. Al_2O_3-based InGaAs gate stack to project the device aging during operation in a digital circuit.

Positive Bias Temperature Instability

Fig. 4 reports typical PBTI measurements on an InGaAs MOSFET with a 10nm Al_2O_3 gate dielectric. A sequence of stress phases (V_G=V_{stress}) of increasing durations, alternated with sense phases (V_G=V_{th0} for a MOSFET, or =V_{fb0} for a MOS capacitor) is applied to the device to estimate the ΔV_{th} (or ΔV_{fb}) induced by charge trapping. The measurement is repeated on multiple pristine devices using increasing stress voltage overdrives, as increasing oxide electric field (E_{ox}) allows channel carriers to interact with a wider range of defect levels (cf. Fig. 3a). The ΔV_{th} follows a power-law-like kinetics with time exponent n~0.1 (typ. Si: ~0.16), and similarly a power-law-like dependence of the stress overdrive, with exponent γ~1.5 (typ. Si: 6~7). The measured data can be used to estimate for each stress voltage the time-to-failure, i.e., the time necessary to reach a failure criterion defined as ΔV_{th}=30mV, and consequently to determine the maximum operating voltage for 10 year reliability.

With BTI being accelerated by E_{ox}, it is convenient to define a benchmark which takes into account the oxide thickness when comparing different gate stacks. The ΔV_{th} measured after a fixed stress time (e.g., 1s) can be converted into an equivalent charge sheet density ΔN_{eff}=ΔV_{th}*C_{ox}/q, and plotted vs. the applied equivalent E_{ox}=V_{ov}/CET (Fig. 5). Data of Al_2O_3-based InGaAs gate stacks with various oxide thicknesses (EOT: 5~1.4nm) line up in such a plot. In order to meet a standard BTI reliability target of ΔV_{th}=30mV after 10 years, acceptable ΔN_{eff} values should be in the low $10^{10}cm^{-2}$ range (assuming a target EOT of 1nm and a power-law time exponent n of 0.1~0.16) or below, consistent with Si data. In contrast, InGaAs devices show ~10× larger ΔN_{eff}. The ΔN_{eff} plot also preserves the crucial information about the BTI voltage acceleration exponent: significantly lower γ values are observed in InGaAs gate stacks as compared to Si. This is ascribed to a wide distribution of oxide defect levels at energies close to the channel Fermi level: defects are accessible already at low E_{ox}, and therefore the device reliability is jeopardized irrespective of the operating V_{DD} (cf. E_{ox}~2MV/cm vs. ~3.5MV/cm marked as Low Power, 'LP', vs. High Performance, 'HP', in Fig. 5a). On the contrary, a narrow distribution of defect levels decoupled from the channel Fermi level results in a higher γ, as channel carriers can get trapped only at high E_{ox} (Fig. 5b).

A. Impact of the device architecture

The ΔN_{eff} measured at a given E_{ox} (e.g., 3.5MV/cm) is an indicator of the accessible defect density in an oxide. Similar ΔN_{eff} values are measured on various device test vehicles (from simple MOS capacitors, to finFETs, nanowires, and even tunnel-FETs despite their *SS* being insensitive to oxide traps [22]), irrespective of the oxide thickness and of the actual dielectric composition (Al_2O_3-

only, vs. Al_2O_3/HfO_2) [17]. However, for scaled nanowires, quantization effects are expected to enhance trapping: experiments on planar MOSFETs show larger ΔN_{eff} and lower γ for downscaled InGaAs channel thicknesses (15~3nm, Fig. 7). This is ascribed to channel carriers populating higher sub-bands, and therefore interacting with a wider range of oxide defect levels [9].

When scaling the device dimensions, the stochastic nature of charge trapping induces variability. Each individual charged defect causes a different ΔV_{th} depending on its location, as can be observed in RTN traces (Fig. 8). The single trap ΔV_{th} step heights are observed to be exponentially distributed, with mean value η scaling inversely with the device area. Each nanoscale device contains a Poisson-distributed number of oxide defects with exponentially-distributed impacts: as a consequence the ΔV_{th} measured on each device after an identical stress is also distributed. Our Defect-Centric model [23] describes the ΔV_{th} statistics, and allows to conveniently estimate η from the first two moments of a measured ΔV_{th} distribution in a device population. We have shown that in InGaAs finFETs η is ~2× larger than in Si counterparts, possibly due to epitaxial defects enhancing channel potential non-uniformity and in turn the impact of oxide defects on the channel electrostatics [14].

B. Capture-Emission-Time Maps

To characterize a wide range of defect capture/emission times, we performed extensive PBTI measurements (Fig. 9) on InGaAs MOSFETs with 1nm Al_2O_3/3nm HfO_2 gate stack at 3 different temperatures (-40, 25,100C), with stress/recovery times ranging from 30ms to 100ks. We then calibrated an energy barrier distribution model to reproduce the experimental transients. Two distinct bivariate distributions of capture/emission times (Fig. 10a) were necessary to reproduce the fast and slow ~log(t) transients observed in the relaxation traces. They can be converted into CET maps for each of the considered temperatures (Fig. 10b). Notice that, despite the microscopic thermal activation of the (de-)trapping process, when measuring ΔV_{th} within a fixed measurement window (e.g., t_{st}=10s, t_{meas}=1ms), an apparently non-Arrhenius temperature dependence can be observed [17,19,24].

The calibrated CET maps can be used to project device aging under periodic AC workloads of relevance for digital circuits (Fig. 11). Assuming a clock frequency of 1kHz and a 50% duty factor (half-period: 0.5ms, comparable with a typ. BTI measurement delay), device aging is dominated by the slow traps, as the fast traps discharge during each OFF-cycle. In contrast, a large fraction of the fast traps contributes to ΔV_{th} during AC operation at 1GHz, limiting the device stability at an early stage of the device lifetime.

Frequency dispersion of the C-V characteristics

Defects with comparable capture and emission characteristic times $\tau_c \approx \tau_e = \tau$ can respond (i.e., charge and discharge) to an applied AC stimulus with frequency $1/\tau$ and therefore affect the measured MOS impedance. Different defects can respond to different signal frequencies, inducing a dispersion of the measured multi-frequency *C-V* traces (Fig. 12). At cryogenic temperatures, the defect response times become significantly longer: therefore, their AC response is suppressed and dispersion-free *C-V*'s are measured [12].

Multi-frequency *C-V*'s are routinely performed to characterize electrical parameters of a MOS system (interface quality, doping levels, metal work function). It is therefore convenient to use *C-V* dispersion as a metric also for oxide defects. To account for the E_{ox} dependence of charge trapping, when comparing different gate stacks the dispersion should be quantified at constant E_{ox} instead of a fixed V_G (Fig. 13a). By multiplying the estimated dispersion for the gate stack *CET*, an oxide thickness-independent figure of merit (D_{eff}) is obtained (Fig. 13b) [25]. By correlating D_{eff} to the measured ΔN_{eff}, a quantitative target for an acceptable D_{eff} level can be defined (Fig. 13c). Refined modeling approaches can be used to model the MOS impedance and extract the density of active oxide defects, consistent with the one extracted with BTI tests (Fig. 13d) [26].

Hysteresis and Defect Level Profiling

Double sweep *C-V* or *I-V* traces, with increasing maximum voltage (V_{stop}) can be also used to estimate the distribution of oxide defect levels. The voltage-dependence exponent γ estimated by hysteresis measurements is consistent with the one estimated with whole BTI measurements (Fig. 14). Even the estimated ΔV_{fb} values are comparable, despite the different waveforms applied in the two tests—this is a consequence of the wide distributions of defect time constants inducing power law-like trapping kinetics with n~0.1 (i.e., comparable ΔV_{th} are observed for slightly different stress times).

For InGaAs gate stacks, the measured hysteresis is not determined only by the stop voltage (V_{stop}), but also by the used start voltage (V_{start}). This is due to the presence of defect levels also right below the channel conduction band (E_C): by applying a more negative V_{start}, more of these levels are depopulated at the beginning of the measurement, and therefore a larger hysteresis is observed when the gate voltage is swept back from a given V_{stop} (Fig. 15). This effect can be used to profile oxide defect levels above *and* below the channel E_C, assuming two Normal distributions of defect levels (i.e., defect bands) as we discussed in [13]. By using this methodology we have observed (Fig. 16) that in Al_2O_3 a shallow and a deep defect band overlap in the vicinity of InGaAs E_C. HfO_2 shows higher peak defect densities, but a lower density right below the InGaAs E_C, and is thus more favorable for nMOS gate stack engineering. The defect bands profiling can be similarly implemented by performing PBTI *and* NBTI stresses (Fig. 17) [27,28].

InGaAs Gate Stack Engineering

Charge trapping can be suppressed by i) reducing the defect density, or by ii) decoupling the defect levels from the channel Fermi level [29]. The latter approach yields an enhanced voltage-dependence (γ) and therefore an exponential reduction of the charge trapping at low operating voltages. Defect density can be reduced by post-metal anneals (Fig. 19). However, the thermal budget limitations for IIIV materials restrict the applicability of this approach. We have demonstrated sufficiently reliable InGaAs gate stacks [17], with enhanced channel mobility [30], by replacing Al_2O_3 with a novel IL developed by ASM, capped by a thin $LaSiO_x$ layer and HfO_2. Defect characterization revealed an enhanced γ~3.5, ascribed to a beneficial shift of the shallow defect band, yielding a minimum density in the vicinity of InGaAs E_C (Fig. 20) [27].

Conclusions

We have presented a review of our recent work about oxide trap characterization in InGaAs MOS gate stacks for novel high-mobility *n*-channel MOSFETs. A novel study of the transient response of the defects, relevant for digital operation, was also presented. A judicious characterization of oxide traps proves to be a crucial step towards the demonstration of sufficiently reliable IIIV gate stacks.

Acknowledgement: ASM is acknowledged for developing the novel IL's.

Ref.: **[1]** K. J. Kuhn, TED 59(7), 2012; **[2]** J. del Alamo, Nature 479, 2011; **[3]** A. Alian, IEDM 2013; **[4]** N. Waldron, VLSI 2014; **[5]** N. Waldron, EDL 35(11), 2014; **[6]** N. Waldron, IEDM 2015; **[7]** X. Zhou, VLSI 2016; **[8]** M.L. Huang, APL 87, 2005; **[9]** J. Franco, IRPS 2014; **[10]** S. Deora, TDMR 13(4), 2013; **[11]** G.F. Jiao, IEDM 2011; **[12]** A. Vais, APL 107, 2015; **[13]** A. Vais, JAP 121, 2017; **[14]** J. Franco, IEDM 2014; **[15]** T. Grasser, Micr. Rel. 52, 2012; **[16]** J. Robertson, JAP 117, 2015; **[17]** J. Franco, VLSI 2016; **[18]** G. Rzepa, IRPS 2017; **[19]** H. Reisinger, IRPS 2010; **[20]** T. Grasser, IEDM 2011; **[21]** B. Kaczer, IRPS 2014; **[22]** J. Franco, EDL 37(8), 2016; **[23]** B. Kaczer, IRPS 2010; **[24]** V. Huard, Micr. Rel. 45, 2006; **[25]** A. Vais, EDL 38(3), 2017; **[26]** A. Vais, IRPS 2015; **[27]** V. Putcha, IRPS 2017; **[28]** G. Rzepa, VLSI 2016; **[29]** J. Franco, IEDM 2013; **[30]** S. Sioncke, VLSI 2017.

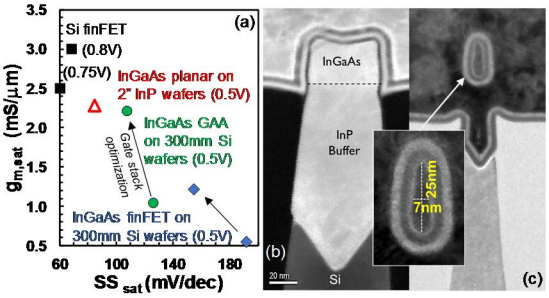

Fig. 1: **(a)** InGaAs device (planar MOSFETs [3], finFETs and Gate-All-Around nanowires [4-7]) performance benchmark: $g_{m,sat}$ vs. SS_{sat} (V_{DD}=0.5V), compared to Si finFETs (V_{DD}=0.75, 0.8V). TEM micrograph of **(b)** an InGaAs finfET, and **(c)** a scaled Gate-All-Around nanowire fabricated on 300m Si wafers.

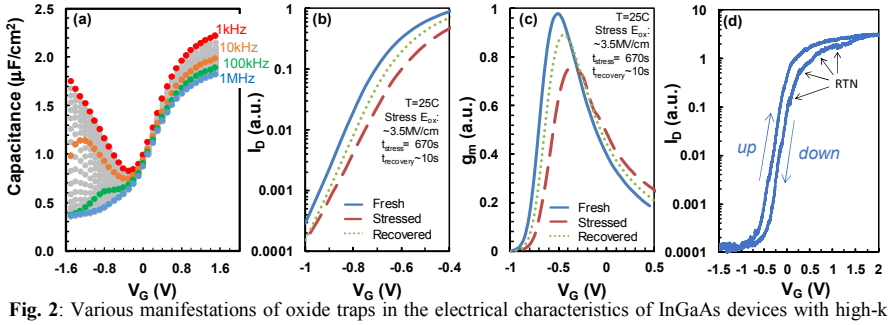

Fig. 2: Various manifestations of oxide traps in the electrical characteristics of InGaAs devices with high-k gate stacks: **(a)** frequency dispersion of MOS *C-V* characteristics (1nm Al_2O_3/3nm HfO_2); **(b)** V_{th} and *SS* instability (increase after stress, back towards original values after a recovery period), and **(c)** g_m instability in planar MOSFETs (10nm Al_2O_3); **(d)** hysteresis of the I_D-V_G characteristic of a finFET (2nm Al_2O_3/3nm HfO_2). Note: in nanoscale devices discrete charge (de-)trapping events are observed also as Random Telegraph Noise.

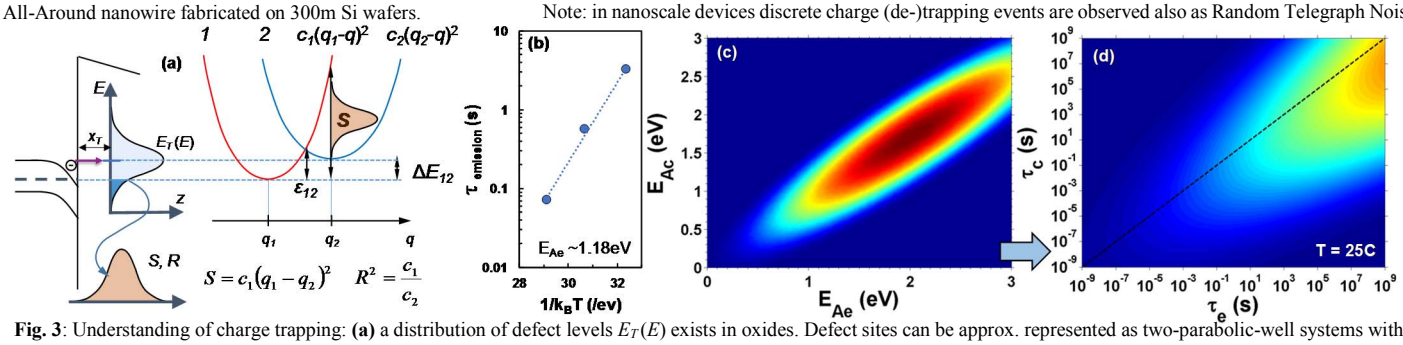

Fig. 3: Understanding of charge trapping: **(a)** a distribution of defect levels $E_T(E)$ exists in oxides. Defect sites can be approx. represented as two-parabolic-well systems with distributed curvatures (*S*, *R*), describing the energy barriers involved in the microscopic charging and discharging processes [15,18]. **(b)** An example of the experimental temperature activation of the charge emission from a single defect. **(c)** The spread of defect properties in amorphous oxides can be described with a bi-variate distribution of activation energies for capture and emission, which translates into a temperature-dependent Capture-Emission-Time map [19,20]. The transient response of an ensemble of defects to an applied waveform (cf. Fig. 4a) can be inferred by such a map. The example shown pertains to a commercial Si high-k nMOS gate stack [21].

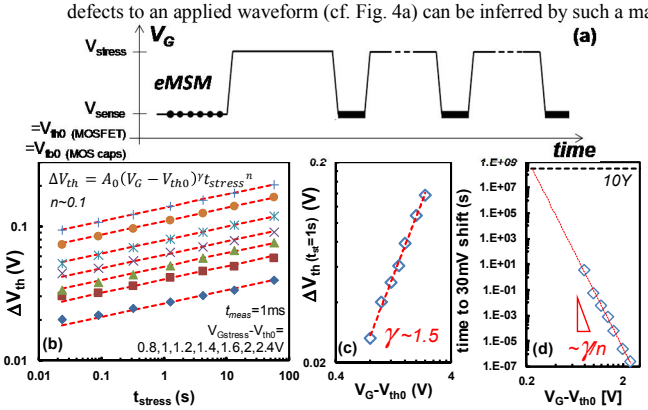

Fig. 4: **(a)** Typical BTI extended measure-stress-measure (eMSM) sequence. After each stress phase (V_G=V_{stress}) defect discharging is monitored at V_G=V_{th0} (cf. Fig. 9). **(b)** ΔV_{th}(t_{stress}, t_{meas}=1ms) measured for varying V_{stress} in InGaAs MOSFETs with 10nm Al_2O_3, showing power-law like behavior (*n*~0.1). **(c)** a moderate voltage dependence of the ΔV_{th} is observed (γ~1.5). **(d)** Times to 30mV shift: a 10 year operation is ensured only for overdrive voltages <0.23V in this case.

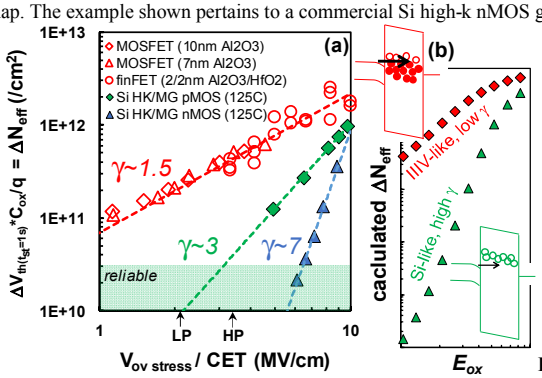

Fig. 5: **(a)** Charge-trapping-induced ΔV_{th} converted into an equivalent charge sheet (ΔN_{eff}= ΔV_{th}*C_{ox}/*q*) vs. the equivalent oxide field (E_{ox}~*Vov/CET*) for Al_2O_3-based InGaAs devices (EOT=5-1.4nm), compared to Si pMOS and nMOS. A weaker voltage dependence (γ~1.5) as compared to Si is consistently observed, ascribed to **(b)** a wide distribution of oxide defect levels around InGaAs E_c.

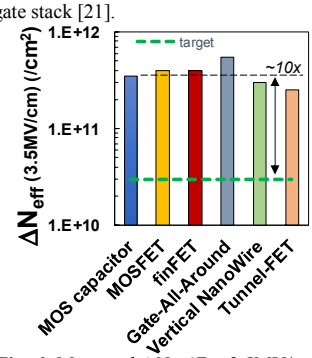

Fig. 6: Measured ΔN_{eff} (E_{ox}~3.5MV/cm) in a variety of InGaAs devices with Al_2O_3-based gate stacks. Regardless of the device architecture and of the actual gate stack composition, a ΔN_{eff} of ~4x10^{11}cm^{-2} is observed, i.e., ~one order of magnitude above the acceptable target.

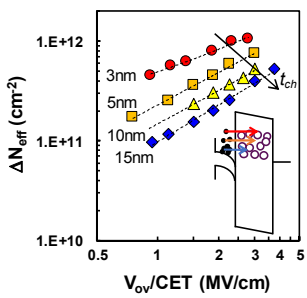

Fig. 7: ΔN_{eff} vs. V_{ov}/*CET* measured in InGaAs MOSFETs (10nm Al_2O_3) with varying channel thicknesses. The larger ΔN_{eff} and weaker voltage dependence observed in thin channels are ascribed to quantization effects: channel carriers populating higher sub-bands can interact with a wider range of oxide defect levels.

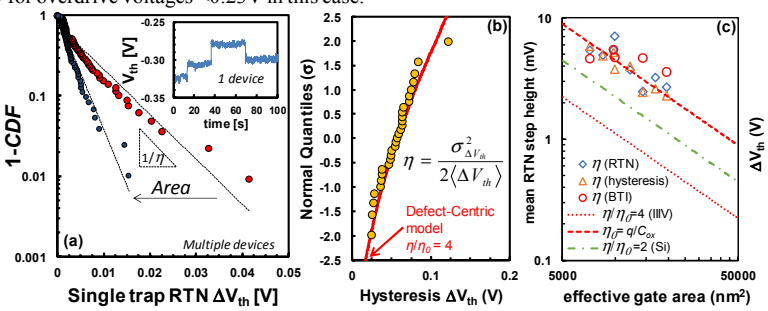

Fig. 8: **(a)** Single-defect-induced discrete V_{th} fluctuations (RTN) measured in InGaAs finFETs (2nm Al_2O_3/3nm HfO_2) appear to be exponentially-distributed, with mean value η scaling inversely with the device area. **(b)** η can be conveniently estimated by applying the Defect-Centric model [23] to a distribution of V_{th} hysteresis (or BTI-induced ΔV_{th}) measured in a population of nominally identical devices. **(c)** InGaAs devices show η values 4× larger than the simple electrostatic weight of a single charge (=*q*/C_{ox}), and 2× larger compared to Si devices, possibly due to epitaxial defects inducing additional channel potential non-uniformity.

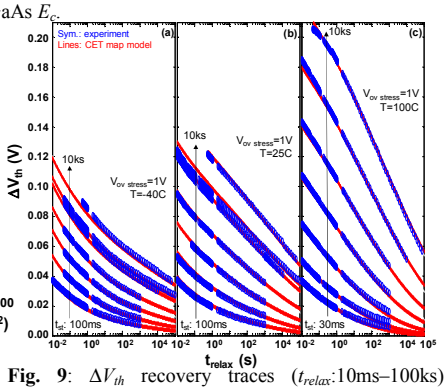

Fig. 9: ΔV_{th} recovery traces (t_{relax}:10ms–100ks) measured on InGaAs MOSFETs (1nm Al_2O_3/3nm HfO_2) after stress phases of increasing durations (t_{stress}: 30ms–10ks), at $V_{Gstress}$=V_{th0}+1V, at 3 temperatures **(a)** -40C, **(b)** 25C, **(c)** 100C. The extensive datasets are perfectly described by the distribution of activation energies (CET map) shown in Fig. 10.

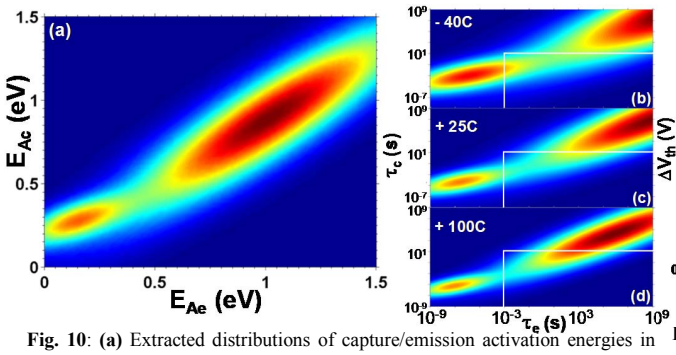

Fig. 10: **(a)** Extracted distributions of capture/emission activation energies in InGaAs/1nm Al_2O_3/3nm HfO_2/TiN MOS. Two subpopulations of electron traps are observed, both with mean activation energies notably smaller than in Si [cf. Fig. 3 (c)]. Corresponding Capture-Emission-Time maps at **(b)** -40C, **(c)** 25C, **(d)** 100C. A faster and a slower defect populations are observed. Note: the ΔV_{th} induced by the subsets of defects charged during a test (e.g., white rectangles, t_{stress}=10s, t_{meas}=1ms) can show apparently non-Arrhenius temperature dependences [19,24] , particularly in the presence of two defect populations [17].

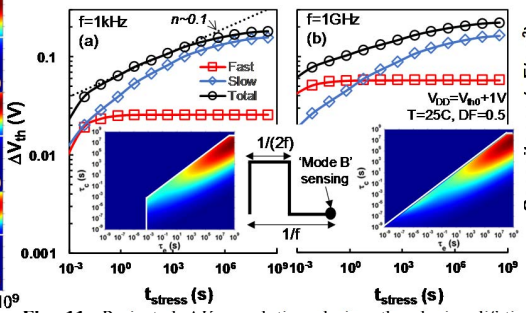

Fig. 11: Projected ΔV_{th} evolution during the device lifetime, assuming continuous AC operation (duty factor=50%) at **(a)** 1kHZ, and **(b)** 1GHz, assuming sensing at the end of an OFF-cycle ('Mode B' sensing, see inset). For AC operation at 1kHz (half period = 0.5ms, i.e., comparable with a typical experimental measurement delay), the device aging is dominated by the slow traps. At 1GHz, a larger fraction of the fast traps contributes to the V_{th} shift. The charged fractions of traps at 10 years are depicted in the insets.

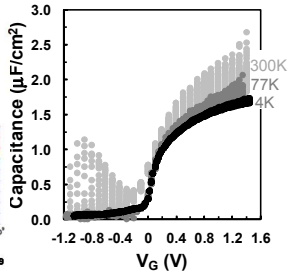

Fig. 12: Multi-frequency (1kHz-1MHz) *C-V* curves measured on InGaAs/2nm $GdAlO_x$/2nm HfO_2 at 3 different temperatures [12]. Note the strong temperature dependence of the dispersion in accumulation.

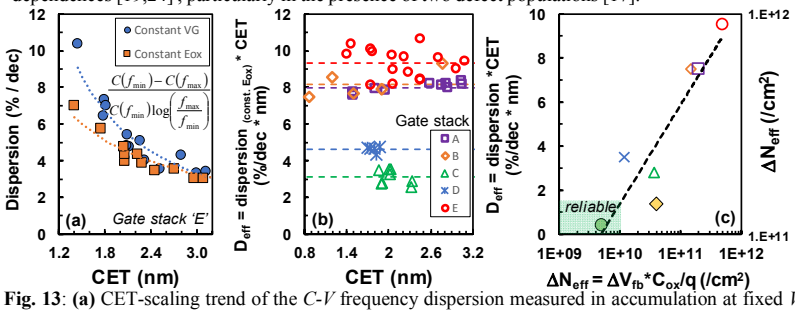

Fig. 13: **(a)** CET-scaling trend of the *C-V* frequency dispersion measured in accumulation at fixed V_G or at fixed E_{ox} in InGaAs/Al_2O_3/HfO_2 MOS (various thicknesses). **(b)** The product of the frequency dispersion and the CET yields a simple CET-independent figure of merit (D_{eff}) which can be used to compare gate stack quality [25]. **(c)** By correlating D_{eff} to the ΔN_{eff} measured by BTI measurements, a target value for D_{eff} can be defined (<2%/dec*nm). **(d)** Alternatively, frequency dispersion can be modeled to extract an effective trap density, which is consistent with BTI measurements [26].

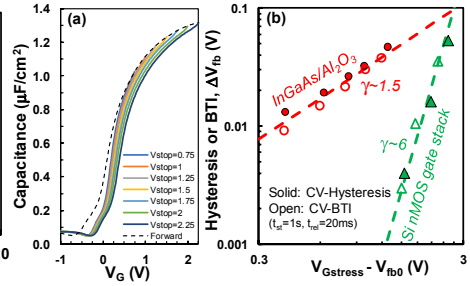

Fig. 14: **(a)** *C-V* hysteresis measurements of InGaAs/5nm Al_2O_3 MOS, for increasing V_{stop}. **(b)** The V_{fb} hysteresis values plotted vs. the applied overdrive voltage (V_{stop}-V_{fb0}), compared to the values obtained by BTI measurements, for an InGaAs gate stack and a Si gate stack.

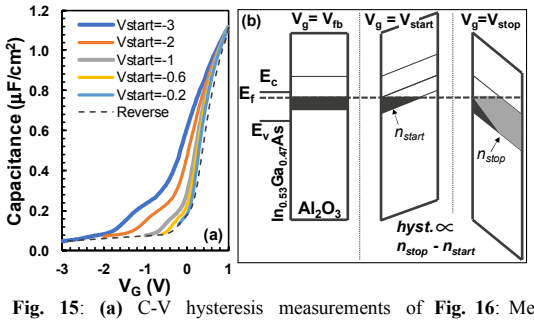

Fig. 15: **(a)** C-V hysteresis measurements of InGaAs/5nm Al_2O_3 MOS, for decreasing V_{start}. **(b)** In the presence of oxide defect levels above and below the semiconductor conduction band, the application of a negative V_{start} pre-discharges a fraction of the defect levels, inducing the observation of a larger *C-V* hysteresis for a fixed V_{stop}.

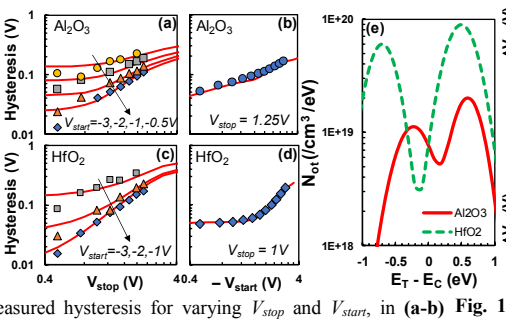

Fig. 16: Measured hysteresis for varying V_{stop} and V_{start}, in **(a-b)** InGaAs/5nm Al_2O_3, and **(c-d)** InGaAs/5nm HfO_2. **(e)** A defect band model [13], including two Normal distributions of defect levels above and below InGaAs E_C, calibrated to match the experimental data [cf. lines in (a-d)]. Al_2O_3 shows lower peak defect densities, but defect bands overlap, inducing a ~ uniform distribution around InGaAs E_C. HfO_2 shows a minimum defect density ~0.2eV below the channel E_C.

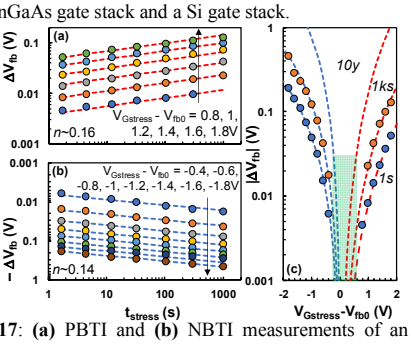

Fig. 17: **(a)** PBTI and **(b)** NBTI measurements of an InGaAs/ASM IL/HfO_2 nMOS gate stack characterize both the shallow and deep defect bands. For both polarities, ΔV_{fb} shows ~power-law kinetics (n~0.15), arising from the wide distributions of capture times associated with oxide defects. **(c)** Extrapolated data to assess the maximum overdrive and underdrive for 10 year reliability.

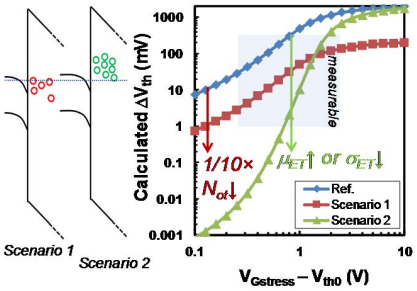

Fig. 18: Strategies for gate stack improvement: oxide defect density reduction ('scenario 1') can yield a proportional reduction of charge trapping; gate stacks with narrow defect bands, at energies unfavorable for channel carriers ('scenario 2'), can yield an exponential reduction of charge-trapping at operating voltages.

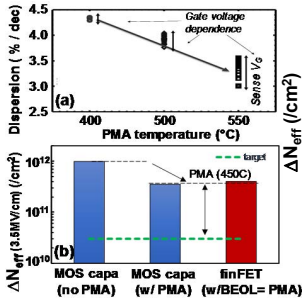

Fig. 19: Post-metal anneals (w/ TiN gate) in hydrogen-containing ambient reduce the oxide defect density yielding **(a)** a reduced frequency dispersion (note the stronger sense voltage dependence), and **(b)** a reduced ΔN_{eff}. BEOL fabrication provides an inherent PMA in fully integrated devices (e.g., finFETs).

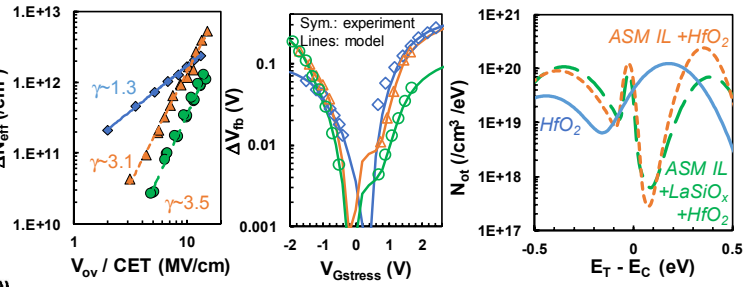

Fig. 20: **(a)** InGaAs gate stack optimization: by replacing the Al_2O_3 IL with a novel IL (ASM), a dramatic reduction of ΔN_{eff} at operating voltages is demonstrated, thanks to an enhanced voltage dependence (γ~3.1) [17]. Further improvement is demonstrated by stabilizing the IL with a thin $LaSiO_x$ layer before HfO_2 deposition [30]. **(b)** The PBTI and NBTI data modeled to extract **(c)** the defect level distributions in the optimized gate stack [27]. The novel IL shifts the energy level of the shallow traps, yielding a minimum defect density right above InGaAs conduction band.