Reliability of Next-Generation Field-Effect Transistors with Transition Metal Dichalcogenides

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***Abstract*—We perform a detailed reliability study of MoS_2, $MoSe_2$, $MoTe_2$ and WS_2 field-effect transistors fabricated on the same SiO_2/Si substrate. First we analyze the sensitivity of these devices to adsorbate-type trapping sites on top of the channel and show that their contribution can be minimized at high temperatures, which leads to a domination of charge trapping by oxide traps. Then we compare the high-temperature dynamics of the hysteresis and bias-temperature instabilities for different devices. Our results show that the observed differences can be partially explained by the alignment of known defect bands in SiO_2 relative to the conduction and valence band edges of the two-dimensional channel materials. As such, our study provides strong fundamental insights into the reliability of these new technologies and opens further perspectives on how to reach commercial quality standards.**

I. Introduction

Transition metal dichalcogenides (TMDs) present a wide class of two-dimensional (2D) materials which includes fascinating "beyond-graphene" semiconductors such as MoS_2, $MoSe_2$, $MoTe_2$, WS_2 and WSe_2 [1–5]. Contrary to graphene [6], TMDs have sizable electronic bandgaps ranging from 1.7 eV for $MoTe_2$ to 2.5 eV for MoS_2 in the single-layer (1L) limit [7]. Owing to this, these materials are potentially interesting for channel applications in next-generation digital 2D electronics. At the same time, the recently achieved epitaxial growth of semiconducting TMDs [8, 9] represents a breakthrough for very large scale integration.

By now, several research groups have succeded at fabricating field-effect transistors (FETs) with MoS_2 [10–14], $MoSe_2$ [15], $MoTe_2$ [16], WS_2 [17] and WSe_2 [5]. Both n-FETs and p-FETs with various TMD channels have been demonstrated, as well as the possibility to adjust Schottky barriers between source/drain and channel to obtain n-type and p-type transistors using the same TMD material [18]. These achievements are very important for future CMOS circuit integration of TMD-based FETs, which requires both n- and p-FETs. However, commercialization of these next-generation devices is not possible without proper understanding and improvement of their reliability, which should be urgently addressed. By now, more or less detailed reliability studies have been performed only for MoS_2 FETs [14, 19]. In particular, it has been found that these devices suffer from charge trapping by both oxide traps [13, 14, 19, 20] and adsorbate-type trapping sites (e.g. water molecules) on the MoS_2 channel [10–12, 14]. This charge trapping leads to considerable hysteresis [10, 11, 13, 14] and bias-temperature instabilities (BTI) of the gate transfer characteristics [12, 14, 20]. While the contribution from adsorbates can be minimized by treatment of the devices at higher temperatures [14], we argue that charge trapping by oxide traps, which are energetically aligned within certain defect bands [19, 21, 22], is dependent on the selected combination of the channel and insulator materials. In order to provide more insight into this hypothesis, we perform a detailed reliability study of MoS_2, $MoSe_2$, $MoTe_2$ and WS_2 FETs fabricated on the same SiO_2/Si substrate and compare the results obtained for different devices.

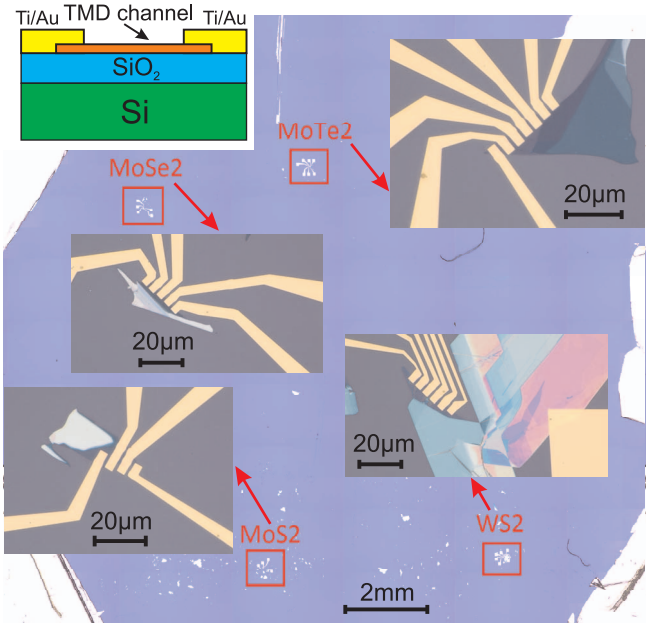

Fig. 1: Optical microscope images of our 1L MoS_2, $MoSe_2$, $MoTe_2$ and WS_2 FETs fabricated on the same chip. The devices are of a back-gated configuration with 90 nm thick SiO_2 as a gate insulator and Ti(5 nm)/Au(30 nm) source and drain pads (see the schematic cross-section on top). The channel length is $L = 1.5\,\mu$m and the widths W are between 0.5 and 8 μm for different devices.

II. Devices

Our devices are back-gated 1L MoS_2, $MoSe_2$, $MoTe_2$ and WS_2 FETs with 90 nm thick SiO_2 as a gate insulator. For a proper comparison of the reliability characteristics, the devices have been fabricated on the same SiO_2/Si substrate and using the same deterministic transfer method of [23]. First, the flakes of different TMD materials have been exfoliated from the bulk crystals using Nitto tape and a polydimethylsiloxane (PDMS) stamp. Then the PDMS surface containing exfoliated

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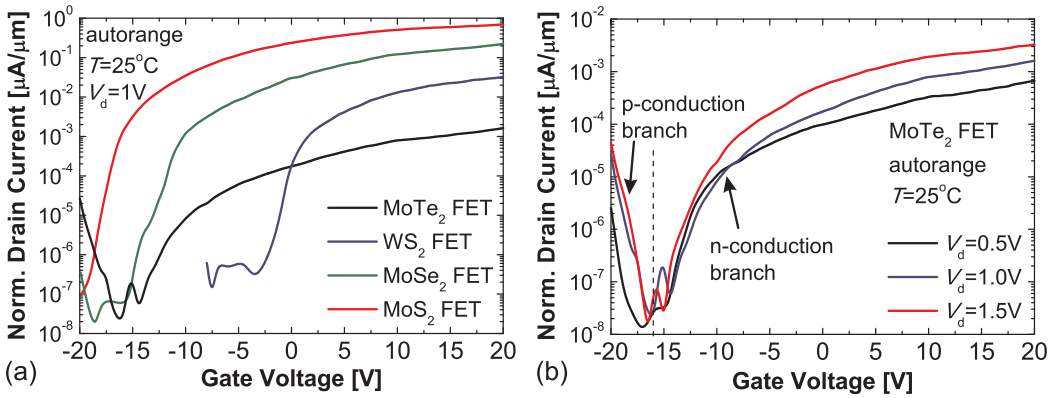

Fig. 2: (a) The I_D-V_G characteristics of four different TMD FETs measured at $V_D = 1\,V$ using the autorange mode. The current is normalized by the channel width W. (b) While MoS_2, $MoSe_2$ and WS_2 devices are n-FETs, the $MoTe_2$ FET exhibits clear ambipolar behaviour. This is likely due to the smallest bandgap of $MoTe_2$ (1.7 eV) and also a smaller Schottky barrier for holes.

crystals has been scanned with an optical microscope in transmission mode, in order to identify single-layer flakes. After this, the desired flakes have been transferred onto the SiO_2 surface. Finally, Ti(5 nm)/Au(30 nm) source/drain pads have been created using standard e-beam lithography. The optical microscope images of our chip with different devices and the schematic device layout are shown in Fig. 1. TMD flakes are contacted by several pads which allowed us to obtain several devices for each material.

III. Experiment

In order to avoid the detrimental impact of the ambient [11], all our measurements have been performed in a vacuum ($\sim 5\times 10^{-6}$ torr) at $T = 25°C$ and 100°C. First we have measured the gate transfer (I_D-V_G) characteristics using the autorange mode, which was necessary to verify the performance of our devices. Then we analyzed the hysteresis dynamics by measuring the I_D-V_G characteristics using forward (V^+) and reversed (V^-) sweep directions and different measurement frequencies $f = 1/(N t_{step})$, with N being the number of V_G steps given by the step voltage V_{step} and t_{step} the sampling time [14]. Finally, we examined the BTI degradation and recovery dynamics by applying subsequent stress/recovery cycles with logarithmically increased stress times t_s [14, 24]. Similarly to a technique previously used for Si devices [25] and encapsulated MoS_2 FETs [26], a constant gate voltage was applied during both stress (V_S) and recovery (V_R). The latter was necessary to minimize uncontrollable drifts of the potential at the back gate which is formed by the Si substrate, and thus make the results more reproducible. Furthermore, in order to maximally stabilize the device, we applied the recovery voltage V_R during few hours before the beginning of our BTI stress/recovery cycles. Also, in some cases we monitored the evolution of the I_D-V_G curves during both stress and recovery.

IV. Results and Discussions

In Fig. 2a we show the I_D-V_G characteristics measured using the autorange mode for all four TMD devices. The on/off current ratios vary from $\sim 10^5$ for $MoTe_2$ FETs to $>10^7$ for $MoSe_2$ devices. Also, in agreement with literature reports [16], $MoTe_2$ devices exhibit both electron and hole conduction, known as ambipolar behaviour (Fig. 2b). This feature originates from the comparably small electronic bandgap of $MoTe_2$ (~ 1.7 eV) [7] and likely a smaller Schottky barrier for holes compared to other TMDs. The presence of both n- and p-FET performance considerably extends possible applications of $MoTe_2$ FETs in integrated logic CMOS circuits, especially taking into account the reasonable on/off current ratio observed for these devices.

In Fig. 3a we compare the I_D-V_G characteristics measured for different TMD devices at $T = 100°C$ using the sweep rate $S = 0.02$V/s, which corresponds to a total time of a return sweep between -20 and 20 V of more than an hour. Following our methodology from [14], we extract the hysteresis width ΔV_H around the threshold voltage V_{th} from the I_D-V_G characteristics measured using different sweep rates and plot them versus the measurement frequency f (Fig. 3b). Clearly, the largest hysteresis is observed for the $MoTe_2$ and $MoSe_2$ devices and the smallest is visible for the MoS_2 and WS_2 FETs. In order to understand the origin of this hysteresis, in Fig. 3c we compare the slow sweep hysteresis widths measured at $T = 25°C$, 100°C and 25°C after a week at 100°C. In agreement with our previous study [14], for the MoS_2 FET the hysteresis becomes smaller during and after the 100°C treatment. We speculate that this is due to the evaporation of a considerable number of adsorbates, most of which do not return to the MoS_2 surface after the temperature is decreased to 25°C. As for the WS_2 and $MoTe_2$ FETs, we observe an insignificant increase of the hysteresis at $T = 100°C$, which likely means that the initial concentration of adsorbates is not that large. As such, in these devices thermal activation of charge trapping by oxide traps in SiO_2 and other remaining defects dominates over the annealing of adsorbates from the TMD surface. However, after the end of the 100°C treatment, the hysteresis in WS_2 and $MoTe_2$ FETs becomes even larger than it was before. This means that a number of new trapping sites have appeared on the TMD channel surface. Something similar is observed also for the $MoSe_2$ device, although at $T = 100°C$ the hysteresis was decreased, similar to the MoS_2 device. The latter means that the initial number of adsorbates on the surface of MoS_2 and $MoSe_2$ is relatively larger than for

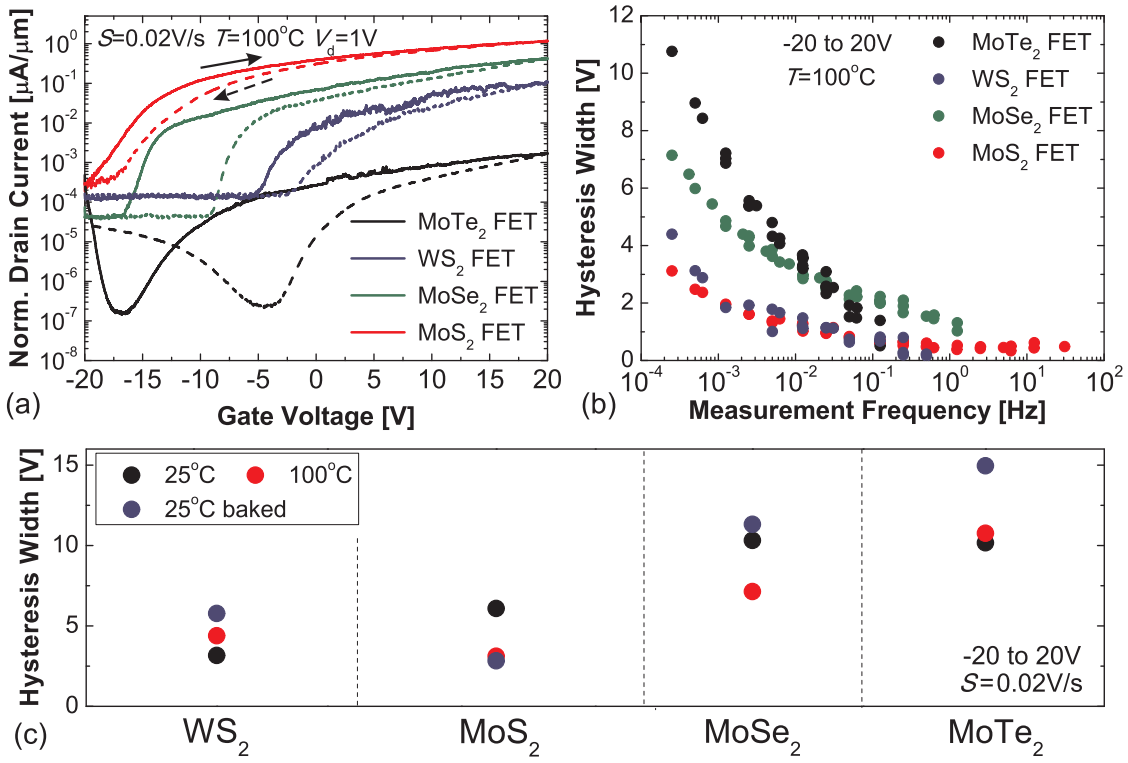

Fig. 3: (a) The I_D-V_G characteristics of four different TMD FETs measured at $T = 100°C$ using $S = 0.02$ V/s. (b) The corresponding $\Delta V_H(f)$ dependences. (c) Maximum hysteresis widths measured for our TMD FETs before, during and after the $T = 100°C$ treatment. A decrease of ΔV_H at higher temperature and its increase after temperature treatment observed for our devices presents a clear proof that the hysteresis is partially due to adsorbate-type trapping sites. In order to minimize their impact, all following measurements have been performed at $T = 100°C$.

WS_2 and $MoTe_2$, which makes their annealing dominate over the thermal activation of the remaining defects like oxide traps. At the same time, we believe that an increase of the hysteresis after the 100°C treatment in WS_2, $MoTe_2$ and $MoSe_2$ FETs is associated with the chemical properties of these TMDs. Namely, these materials are able to attract a large number of adsorbates which have been previously evaporated from the large area of the whole chip surface, which is in contrast to MoS_2. Taking into account this difference between MoS_2 and the other three TMD materials, we conclude that a proper comparison of the reliability characteristics for all four devices is more favourable at $T = 100°C$ rather than at $T = 25°C$ after baking. This is because the impact of adsorbates on the total drifts of the I_D-V_G characteristics is considerably reduced at $T = 100°C$. Together with some thermal activation, this makes the contribution of charge trapping by oxide traps in SiO_2, which we are mostly interested in, more visible.

In Fig. 4 we show the evolution of the I_D-V_G characteristics and the corresponding recovery traces for the threshold voltage shifts ΔV_{th} corresponding to positive and negative BTI (PBTI and NBTI, respectively) measured at $T = 100°C$ for our WS_2 device. While the extracted threshold voltage shifts are considerable, in the case of PBTI the degradation tends to recover completely after several hours. Furthermore, some over-recovery is observed, which is likely because the recovery voltage $V_R = -4$ V corresponds to NBTI bias condition. At the same time, the NBTI recovery at $V_R = -2$ V is incomplete and contains some permanent component. The latter likely means that $V_R = -2$ V is still within the NBTI bias range. This prevents relaxation of all defects which have changed their charge states during the NBTI stress at $V_S = -20$ V. The related results for our ambipolar $MoTe_2$ device (Fig. 5) show that the magnitudes of both PBTI and NBTI degradations are larger than for the WSe_2 device. At the same time, the PBTI degradation of $MoTe_2$ FETs is stronger than NBTI, though being recoverable by more than 90% after several hours. In contrast, the recovery of the originally less pronounced NBTI degradation contains a larger permanent component. Also, for smaller stress times the NBTI shifts tend to increase during recovery, which is somehow similar to our previous observations for Si technologies [27].

In Fig. 6 we continue our analysis of the PBTI and NBTI dynamics in the $MoTe_2$ FET by measuring the evolution of the I_D-V_G characteristics during both stress at $V_S = \pm 20$ V and recovery at $V_R = -4$ V, with stress and relaxation times of as long as $\sim 10^5$s. The stress traces obtained for NBTI and PBTI are more or less similar, with some domination of PBTI over NBTI, making the results consistent with Fig. 5. In contrast, the recovery traces for PBTI and NBTI are considerably different. Namely, the PBTI trace exhibits a complete recovery and saturates slightly below the original V_{th}. At the same time, NBTI recovery is not complete and contains some permanent component which is conserved even after a long relaxation time. These observations allow us to conclude that $V_R = -4$ V corresponds to NBTI bias condition.

Finally, in Fig. 7 we compare the PBTI and NBTI shifts

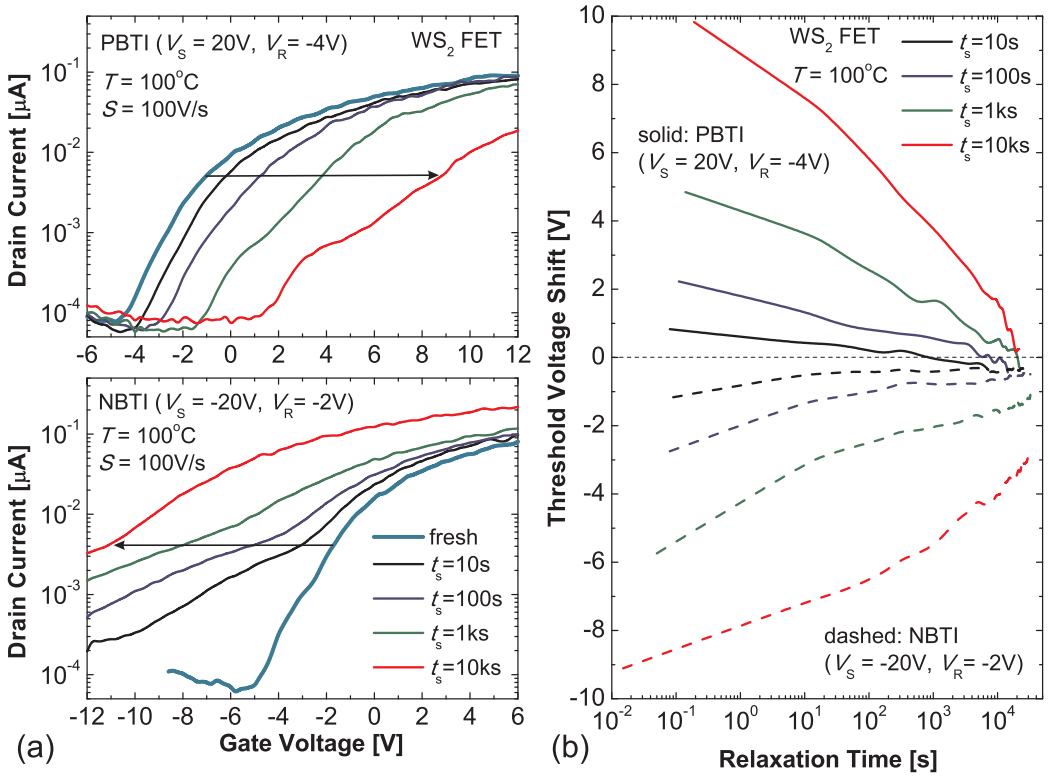

Fig. 4: (a) Evolution of the I_D-V_G characteristics of our WS_2 FETs after subsequent PBTI (top) and NBTI (bottom) stresses with increasing stress times measured at $T = 100$°C. (b) The corresponding recovery traces for ΔV_{th}. While the threshold voltage shifts are considerable, the PBTI traces exhibit weak over-recovery. This likely means that $V_R = -4$V corresponds to NBTI bias condition. Conversely, for the same reason NBTI recovery at $V_R = -2$V contains some permanent component.

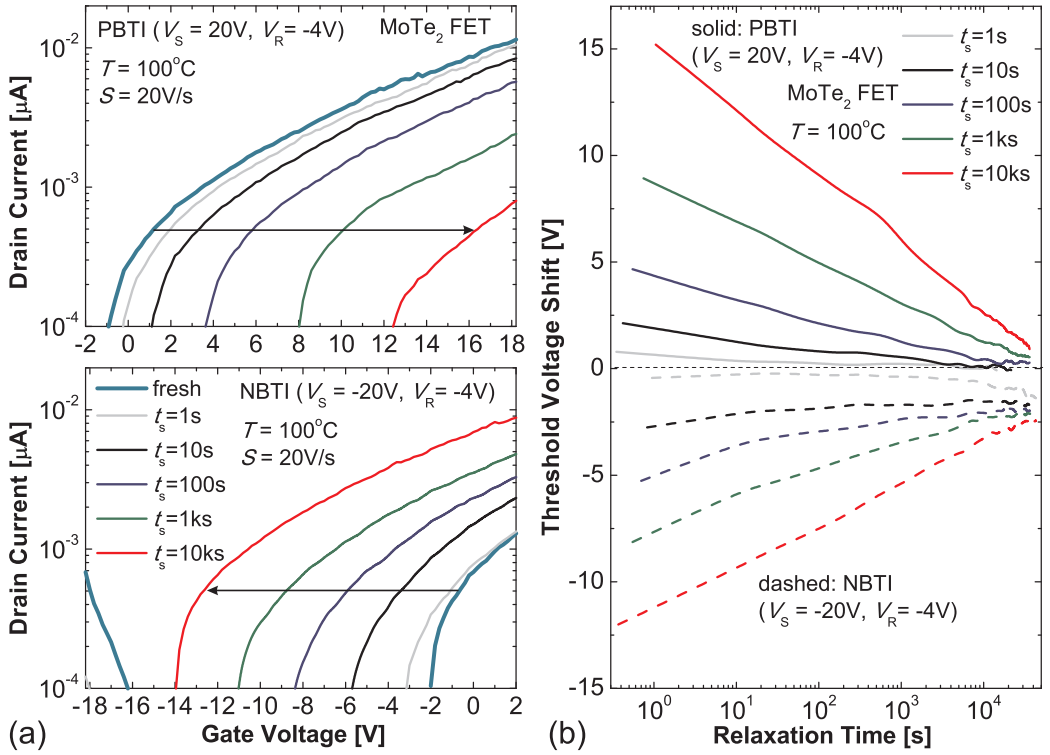

Fig. 5: (a) Evolution of the I_D-V_G characteristics of our $MoTe_2$ FETs after subsequent PBTI (top) and NBTI (bottom) stresses with increasing stress times. (b) The corresponding recovery traces. PBTI degradation is stronger and more recoverable than NBTI containing a larger permanent component. For smaller stress times the NBTI shift tends to increase during recovery.

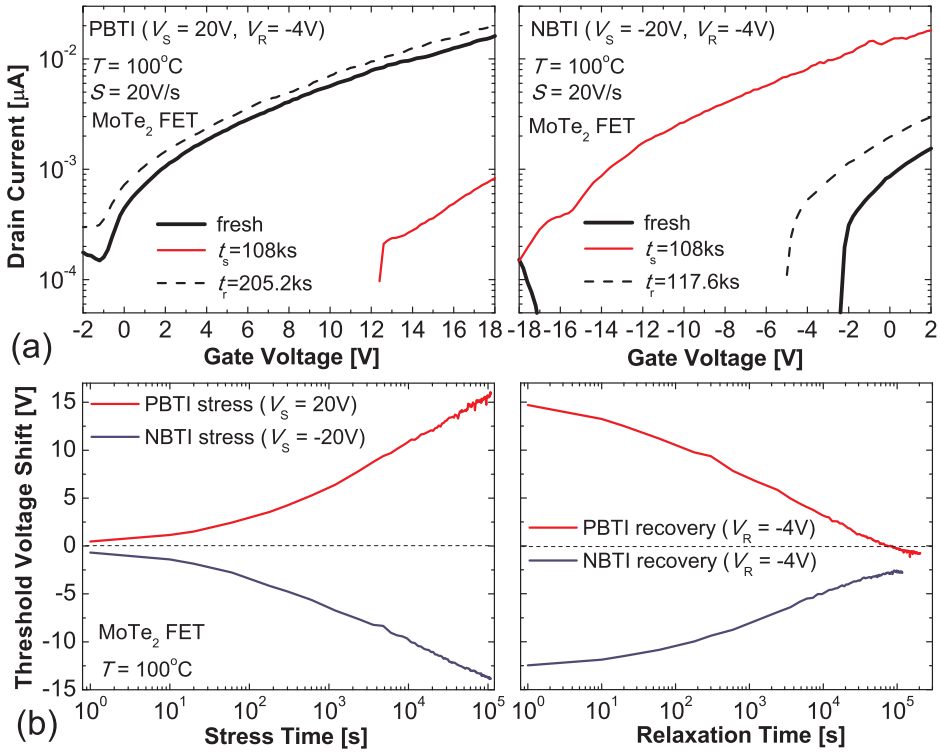

Fig. 6: (a) Evolution of the I_D-V_G characteristics of our $MoTe_2$ device after long PBTI (left) and NBTI (right) stresses and recovery. (b) The corresponding stress (left) and recovery (right) traces for ΔV_{th}. The PBTI trace exhibits slight over-recovery and NBTI contains some permanent component.

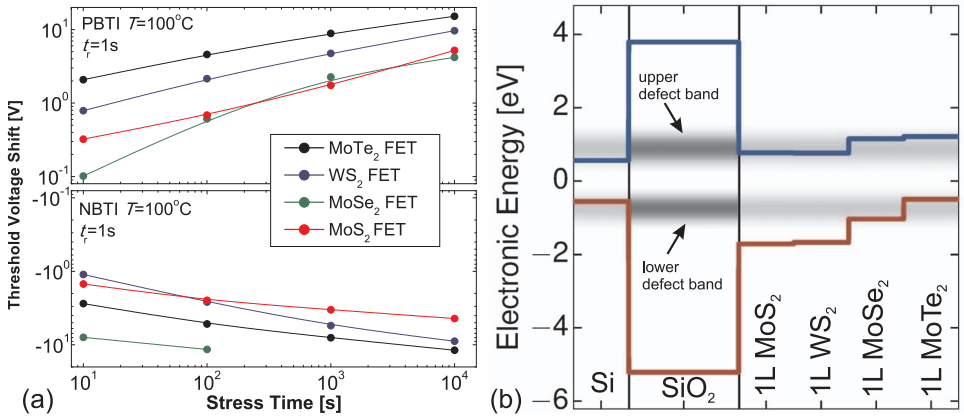

Fig. 7: (a) Comparison of PBTI (top) and NBTI (bottom) shifts at $t_r = 1$ s versus stress time for all four devices. (b) The band diagram showing the band edges of our TMDs aligned to SiO_2; two known oxide defect bands are shown in grey. In $MoSe_2$ and $MoTe_2$ FETs charge trapping is likely due to both defect bands, which leads to considerable PBTI and NBTI (especially for $MoSe_2$ FETs) degradation. In contrast, for MoS_2 and WS_2 FETs the lower defect band is relatively far from the valence band, which makes the contribution of the upper defect band dominant. This is consistent with comparably small NBTI shifts and hysteresis observed for these devices.

for all four devices at the relaxation time $t_r = 1$ s (Fig. 7a) and notice that the difference in the degradation magnitudes can be partially explained based on the band diagram provided in Fig. 7b. This band diagram shows the defect bands known for SiO_2 from our previous works for Si technologies [28], black phosphorus [21] and MoS_2 [19] FETs with the theoretical band offsets for our TMD materials based on [7]. We argue that if the contribution of adsorbates is minimized and charge trapping is dominated by oxide traps in SiO_2, as it should be at $T = 100$°C, the magnitudes of the hysteresis and BTI will be mostly determined by the energetic alignment of these defect bands relative to the conduction and valence band edges of a certain TMD channel material. In particular, the upper defect band in SiO_2 is quite close to the conduction bands of all four TMDs, which is consistent with sizable BTI shifts in all our devices. At the same time, for $MoSe_2$ and $MoTe_2$ FETs charge trapping is likely to have a sizable contribution also from the lower defect band, which is quite close to the valence band of these materials. This is fully consistent with the stronger NBTI shifts observed for the $MoSe_2$ FET, as well as with stronger PBTI and NBTI for the $MoTe_2$ device. In contrast, for MoS_2 and WS_2 devices the contribution of the lower defect band is

negligible. This is consistent with weaker NBTI and smaller hysteresis (Fig. 3b) in the MoS_2 and WS_2 FETs. At the same time, we can conclude that for all four TMDs the alignment of the SiO_2 defect bands is not very favourable, especially for the ambipolar $MoTe_2$ device. Therefore, in order to improve the reliability of TMD FETs, one would need to use gate insulators other than SiO_2.

V. Conclusions

We have performed a first comprehensive reliability study of different TMD FETs fabricated on the same SiO_2 substrate. First we have analyzed the sensitivity of these devices to adsorbate-type trapping sites. We found that in all TMD devices the contribution of adsorbates can be minimized at higher temperature. However, only the MoS_2 FETs conserve the reliability improvement after the temperature is decreased again. As such, we concluded that charge trapping by oxide traps in bare TMD FETs should be studied at higher temperatures. Then, we have compared the hysteresis and BTI degradation/recovery dynamics for different TMD FETs and found that the difference in the measured hysteresis widths and threshold voltage shifts can be partially explained by the relative alignment of the conduction and valence band edges of the TMDs with the defect bands in SiO_2. Although for the investigated TMDs this alignment is not favourable, our study provides fundamental insights into the understanding of the reliability of the next-generation TMD FETs and opens new possibilities for decreasing the impact of charge trapping by oxide traps in these devices.

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