Annealing and Encapsulation of CVD-MoS_2 FETs with 10^{10} On/Off Current Ratio

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Introduction: MoS_2 is a two-dimensional (2D) semiconductor which is now considered as a channel material in 2D FETs [1–3]. Recently we found that single-layer (1L) MoS_2 FETs grown by chemical vapour deposition (CVD) and encapsulated with high-quality Al_2O_3 layer exhibit superior performance and reliability compared to all previously reported 2D FETs [2]. However, while the I_{on}/I_{off} ratio ($\sim 10^9$) of the devices [2] already fulfills commercial standards, their reliability is still poorer than for Si devices [4]. In order to understand the physical origin of these aspects, here we analyze the impact of annealing at 300°C and Al_2O_3 deposition on the performance and hysteresis dynamics of 1L MoS_2 FETs.

Devices: Our devices are 1L MoS_2 FETs [2, 3] with the MoS_2 channel grown by CVD at T = 700°C or 850°C directly on SiO_2(25 nm)/p^{++}-Si substrate back gates [3, 5]. After detailed measurements on bare devices (Fig. 1a), a high-quality 15 nm thick Al_2O_3 encapsulation layer was grown by atomic layer deposition (ALD) at 300°C [6].

Experiment: We measured forward & reversed sweep I_D-V_G characteristics in vacuum ($\sim 5\times10^{-6}$ torr), either using the autorange mode or by varying the measurement frequency $f = 1/t_{sw}$ with t_{sw} being the total sweep time [1, 7]. First we examined bare devices at T = 25°C and 165°C. Then we tested the same devices after 1 hour baking at 300°C and after encapsulation with Al_2O_3 (Fig. 1a).

Results and Discussions: In Fig. 1b we compare the I_D-V_G characteristics measured for the same device at four different conditions. Similarly to [1], at T = 165°C we observe a negative shift of the threshold voltage V_{th}, which becomes more pronounced after baking at T = 300°C. This can be explained by the increased number of S vacancies in MoS_2 [8] due to the thermally activated reaction of S with residual H_2 [9]. At the same time, at T = 165°C bare devices exhibit *non-volatile memory behavior* similar to [10], which is more pronounced for slow sweeps (Fig. 1c). This issue is likely due to the interplay between the creation of S vacancies in MoS_2 and charge trapping in SiO_2, though this requires further study. Finally, after an additional baking step at 300°C followed by Al_2O_3 encapsulation, V_{th} becomes even more positive than it was for bare devices before baking. This is likely because S vacancies created during baking become substituted by O atoms [11], as well as due to some fixed charges at the newly created MoS_2/Al_2O_3 interface. Owing to the more positive V_{th}, the encapsulated devices exhibit I_{on}/I_{off} *ratios of up to* $\sim 10^{10}$ (Fig. 1d), which is limited only by the pad-to-gate leakage I_G becoming sizable at negative V_G.

In Fig. 2a we show that the main trends observed for the I_D-V_G characteristics of 12 best devices are similar. The main finding is a *strong increase of the* I_{on}/I_{off} *ratio after* Al_2O_3 *encapsulation*. While for bare unbaked and encapsulated devices the V_{th} values are close, the improvement of the I_{on}/I_{off} ratio in the latter case is likely due to passivation of some band gap states by the Al_2O_3 encapsulation. At the same time, the I_{on}/I_{off} ratio in bare baked devices is limited by the non-negligible pad-to-gate leakage, owing to a very negative V_{th}. In Fig. 2b we show the hysteresis widths ΔV_H versus the forward sweep V_{th}. Remarkably, after encapsulation the device-to-device variability is one of the smallest and no dramatic increase of the hysteresis is observed, even though the autorange sweeps take about ten times longer.

In Fig. 3a,b we compare the hysteresis dynamics for two bare devices with nearly identical I_D-V_G characteristics before and after 300°C baking. While for Device 1 with originally larger hysteresis we observe some improvement after baking, the smaller hysteresis of Device 2 remains nearly the same. This suggests that for Device 1 the hysteresis may be dominated by adsorbates on top of the channel [1], while for Device 2 it is dominated by oxide traps in SiO_2. Overall, partial annealing of adsorbates during baking leads to a decrease in the variability of the $\Delta V_H(f)$ dependences (Fig. 3c,d). Finally, in Fig. 4 we compare the hysteresis dynamics of two devices before baking, after baking and after encapsulation. Despite the initial difference in the $\Delta V_H(f)$ behavior, we observe the following common trends: First, baking at 300°C reduces the hysteresis. Second, encpasulation leads to a partial increase of the hysteresis and changes the $\Delta V_H(f)$ shape, making it more similar to the devices affected by adsorbates. While the former suggests that additional oxide traps from Al_2O_3 come into play, the latter suggests an interplay between the oxide traps in SiO_2 and Al_2O_3.

Conclusions: We reported *1L CVD-*MoS_2 *FETs with superior performance and reliability*. We found that although their baking at 300°C reduces the hysteresis, it also introduces a strong negative shift of V_{th}. At the same time, subsequent encapsulation with high-quality Al_2O_3 strongly improves the device performance and leads to I_{on}/I_{off} *ratios up to* 10^{10}, *the world record for a 1L semiconductor*, at the cost of a slight hysteresis increase.

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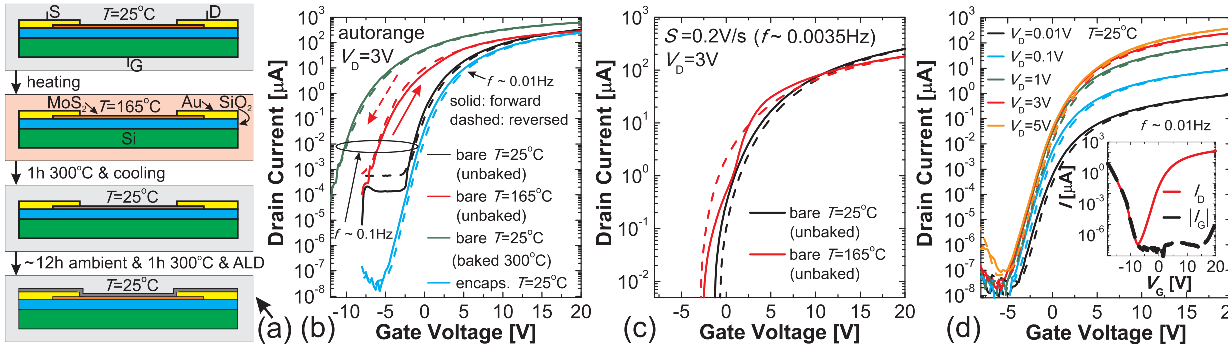

Fig. 1: (a) Schematic layout of our MoS_2 FETs ($L = 1\text{–}4\,\mu$m and $W = 10\,\mu$m) and the main stages of our long-term study. (b) The I_D-V_G characteristics measured for the same device under different conditions. (c) At $T = 165$°C we observe non-volatile memory switching of the hysteresis [10], which is more clearly visible for slow sweeps. (d) A typical I_D-V_G characteristics measured after Al_2O_3 encapsulation. The best on/off current ratio ($\sim 10^{10}$) is achieved for $V_D = 3$ V, while being limited by the pad-to-gate leakage which becomes considerable for V_G below -8 V (inset).

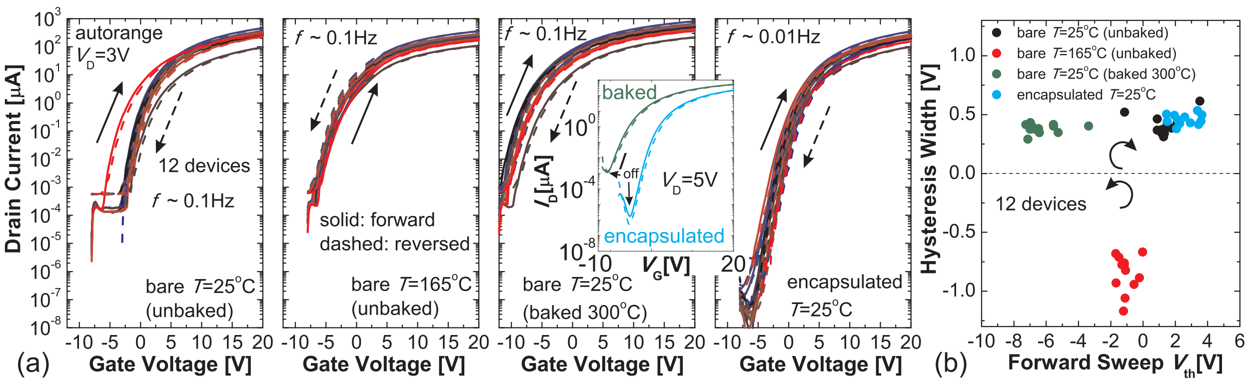

Fig. 2: (a) The I_D-V_G characteristics measured for the same 12 devices before 300°C baking ($T = 25$°C and 165°C), after baking ($T = 25$°C) and after Al_2O_3 encapsulation ($T = 25$°C). After encapsulation V_{th} is more positive and thus I_{off} is smaller, owing to smaller pad-to-gate leakage for more positive V_G (inset). (b) The corresponding hysteresis widths versus forward sweep V_{th}. At $T = 165$°C the hysteresis around V_{th} is switched towards counterclockwise.

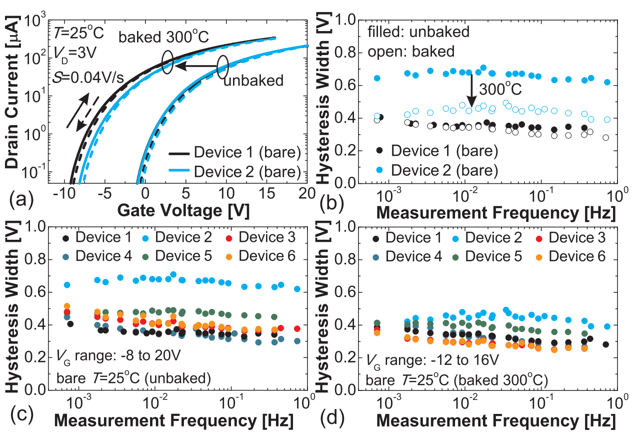

Fig. 3: (a) The slow sweep I_D-V_G characteristics of two bare devices before and after 300°C baking and the corresponding $\Delta V_H(f)$ dependences (b). For Device 2 with the largest ΔV_H the hysteresis is considerably reduced after baking. The $\Delta V_H(f)$ dependences measured for six bare devices before (c) and after (d) 300°C baking. Baking leads to a considerable decrease of the variability.

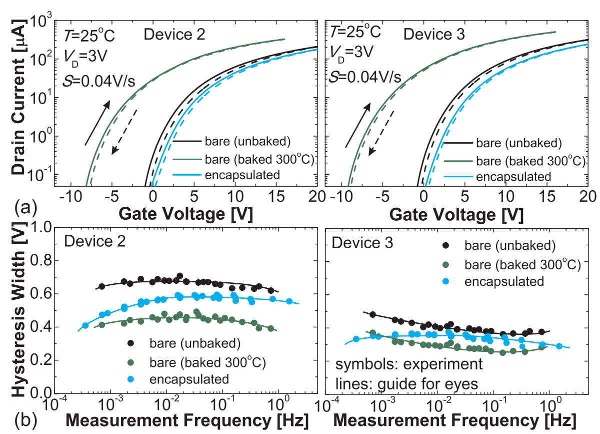

Fig. 4: (a) The slow sweep I_D-V_G characteristics of two devices before baking, after baking and after Al_2O_3 encapsulation exhibit similar trends, with originally larger hysteresis for the Device 2. (b) The corresponding $\Delta V_H(f)$ dependences. While baking reduces the hysteresis, a subsequently applied encapsulation leads to its partial increase and affects the $\Delta V_H(f)$ dependence.