Understanding and Modeling Transient Threshold Voltage Instabilities in SiC MOSFETs

Katja Puschkarsky, Tibor Grassner, Thomas Aichinger, Wolfgang Gustin and Hans Reisinger

Abstract—Modeling of the threshold voltage instabilities in SiC power MOSFETs is difficult due to the fast recovery of $\Delta V_{th}$ after positive and negative gate bias stress. This work investigates the capture- and emission-time constants of positive and negative charge trapped in the gate oxide and at the interface as a function of gate bias and temperature. We present a measurement technique which enables time-resolved measurements of the real $V_{th}$ during application-relevant bipolar AC high temperature gate stress (HTGS). We use capture and emission time (CET) maps to model the temperature and voltage dependence of the $\Delta V_{th}$ after positive as well as negative gate stress. In addition, we provide a complete modeling approach for the $\Delta V_{th}$ after long-term AC stress considering the full stress-history. Furthermore, we present a very accurate model for the short-term hysteresis during a bipolar AC period and we show that the threshold voltage hysteresis has no harmful effect on switching operation in real applications.

Index Terms—BTI, CET, HTGS, Hysteresis, SiC

I. INTRODUCTION

Due to the higher breakdown field, high voltage power MOSFETs made of SiC allow much smaller geometries compared to Si MOSFET with the same on-resistance $R_{on}$ and voltage class [1–3]. As a consequence, lower losses in switch mode converters enable higher operating frequencies and/or higher efficiencies [4]. On the other hand, short-term threshold ($V_{th}$) hysteresis under AC-gate bias as well as long term $\Delta V_{th}$ in SiC-MOSFETs are significantly higher than the ones observed in Si-MOSFETs [5–7]. The threshold voltage hysteresis is especially pronounced – with amplitudes in $\Delta V_{th}$ up to 4V – in commercially available SiC-MOSFETs from various manufacturers [8–10]. It is clear that such a threshold hysteresis of 4V occurring during switching, which roughly corresponds to 1/3 of the total gate-overdrive, has a substantial influence – but is so far neglected – on SPICE models and thus has to be considered properly. A precondition for a proper consideration of the hysteresis $\Delta V_{th}$ is that the dynamics of $\Delta V_{th}$, how it evolves and recovers dynamically under any given gate stress history, are to be determined and known.

There have been several experimental studies on the SiC threshold hysteresis [6, 11–13]. Though these experiments have demonstrated some of the fundamental properties of the threshold hysteresis, they were not designed to provide quantitative data on the sub-millisecond dynamic behavior of $\Delta V_{th}$. For example, they were not able to measure the evolution of $\Delta V_{th}$ under a negative gate bias and how fast this $\Delta V_{th}$ recovers when the gate is switched to a positive bias, as a function of the magnitudes of these biases and as a function of temperature.

Therefore the primary goal of this paper is to demonstrate an experiment and an extraction method providing all the data and parameters for a model required to extend a SPICE simulation in order to consider this non-constant threshold voltage.

Our model is based on capture and emission time (CET) maps and considers stress and recovery times down to 100ns. Thus it is able to determine the threshold voltage hysteresis under real gate signals, for example under bipolar AC-stress [+15/-5V at 50kHz], as occurring in switching converters. The model is also able to explain the peculiarities which have been observed for SiC such as the seemingly unphysical temperature dependence of $\Delta V_{th}$ after DC-stress and the dependence of the measurement delay on the voltage acceleration factor of $\Delta V_{th}$ [14].

Since the measuring technique is key to achieve the above goals, we discuss the parameters of our measurement setup in detail in Section II. A short general introduction into the “CET-methodology” will be given in Section III. The results of our measurements, divided in positive and negative DC stress will be discussed in Sections IV and V, respectively. We will furthermore discuss in this section the properties of the CET maps together with consequences, both for positive and negative gate bias stress. Next, the fast threshold hysteresis under AC stress is discussed in Section VI. Section VII and VIII will present the simulation results utilizing the CET maps for short- and long-term AC-stress, together with experimental data, and thus serve as verification of the model.

II. MEASUREMENT SETUP

The samples used in this study were packaged SiC trench MOSFETs with a rated $V_{ds,max}$ of 1200V and a rated $V_{gs,max}$ of +20/-10V. Measuring $\Delta V_{th}$ after gate bias stress is difficult due to fast recovery after stress. These difficulties are similar to the problems found one decade ago during studies of the negative bias temperature instability on Si devices [15], although they are much more pronounced on SiC. The new measuring techniques introduced for NBTI were measure-stress-measure (MSM) techniques with fast 1μs measurement delays [16, 17] and recovery-free OTF-techniques (on-the-fly) [18] which do not interrupt the stress but try to determine $\Delta V_{th}$ at stress-level. The main differences between SiC-Vth-instabilities and NBTI are:

- Trapping of charges of both polarities at the same time for SiC. Analysis of an observed positive $dV_{th}/dt$, for example, has to distinguish if this $dV_{th}/dt$ is due to trapping of positive charge or emission of negative charge.
- For SiC the relevance of fast effects is much higher than for any Si-MOSFET (power or logic) [14].

In consequence, the unwanted effect of the measurement delay is more important for the SiC case. In particular, the hysteresis under bipolar gate stress amounts up to 4V while it is only several mV for a Si-MOSFET with comparable gate oxide thickness [19].

To account for the above facts we have developed the setup shown in Fig. 1, which intends to meet the following goals:

- The setup must be able to apply any application-relevant gate-stress-sequence e.g. switches between standby conditions and bipolar AC stress with any frequency and duty-factor.
Most important: interruption of stress at any well-defined time, e.g. after 200ns in the high-period (see Fig. 1) and then switch to measure \( V_{th} \) with a measurement delay as short as possible.

It should be noted that the amount of \( \Delta V_{th} \) which recovers during a 1μs measurement delay is more or less insignificant for CMOS logic or Si-power-MOSFET’s, as we will demonstrate, is not at all insignificant for SiC. In the real application, for example after the 10μs-on-period, this \( \Delta V_{th} \) which is recovered during the measurement is still active during the application [14]. The amount can be estimated from CET maps, but the estimation is based only on extrapolations and not on experimental data. This is why our setup, in addition to the MSM-unit also contains an OTF-unit which allows a recovery-free determination of \( \Delta V_{th} \) via the measurement of the on resistance \( R_m \).

With the setup in Fig. 1 we achieve a measurement delay of 1μs. This limit of the measurement delay is due to the value of the drain-current at \( V_{gs} = V_{th} \) of \( \approx 1 \text{mA} \), and the values of the capacitances \( C_{GS} \) and \( C_{GD} \), which have to be recharged when switching from stress-mode to measure-mode. The resolution in the stress-timing as well as the width of the shortest rectangular stress pulses is 100ns. The resulting accuracy in the stress timing (also for the AC signals) is about ±20ns. These accuracy limits are mainly determined by the gate capacitance of \( \approx 2\text{nF} \), the length of the test leads of several cm, together with a missing impedance matching. Thus, our accuracy and lower limit in determining the short time constants of \( V_a \)-transients under positive or negative gate stress due to capturing or emitting charge is about ±20ns.

A setup with commercial instruments, e.g. a pulse- or arbitrary wave-form-generator together with commercial SMU’s, would be able to fulfill the above measurement goals. Unfortunately, commercial instruments in general do not provide any “bare-metal programming” which would be necessary just to provide, for example, the required tight synchronization of wave-form-generator and SMU(s). Moreover, the setup in Fig. 1 is quite inexpensive, and a couple of setups can be fit into a single rack and be controlled by a single computer.

### III. CAPTURE AND EMISSION TIME MAP

We have shown in [14] that as for both Si and SiC, the threshold voltage shifts due to BT1 can be well understood as the collective response of an ensemble of independent defects with the two defect states being charged and uncharged. The CET maps contain the required information about the kinetics of charge capture and emission [20]. Charge exchange and the correlated activation energies can be described in consistence with previous work on Si as the sum of two bivariate Gaussian distributions [20]: one distribution for the defects having short capture and emission times (called recoverable component) and one for the charged defects having emission times mostly permanent in typical experimental time windows from capture and emission times 1μs to 100ks. We denote the recoverable and more permanent component in the following with subscript \( r \) and \( p \), respectively.

The main parameters of this analytic density distribution

\[
g(E_c, E_e) = \frac{A}{2\pi \sigma_c \sigma_{\Delta e}} \times \exp \left( -\frac{(E_c - \mu_c)^2}{2\sigma_c^2} - \frac{(E_e - (r \cdot \sigma_e^2 + \sigma_{\Delta e}^2))^2}{2\sigma_{\Delta e}^2} \right)
\]

The threshold voltage shift, for a given stress- and recovery-time is obtained as the integral of the activation energy map over all defects (recoverable and permanent) being charged up to the stress time and not yet being discharged at the recovery time. For Si, the temperature activation of the capture and emission times of a single trap are commonly modeled according to the Arrhenius equation [22]:

\[
E_{a(c,e)} = k_B T \cdot \ln \left( \frac{T_2}{T_1} \right)
\]

The decrease of the capture and emission time constants with temperature can then be described as:

\[
\tau_2 = \tau_0 \cdot \left( \frac{T_2}{T_1} \right)^{\frac{1}{T_1}}
\]

with \( T_2 \) the transformed capture/emission time constant at temperature \( T_2 \), \( \tau_1 \) the capture/emission time constant at temperature \( T_1 \), and \( \tau_0 \) the time constant for infinite temperature.

The activation energy map is therefore a temperature-independent map and the capture and emission time maps at any constant temperature can be calculated from the activation energy map using (2) with the two characteristic temperature-independent constants, \( \tau_{0,r} \) for the recoverable and \( \tau_{0,p} \) for the more permanent defects.
To obtain the temperature and voltage dependent activation energy map, MSM measurements at different temperatures and voltages have been performed. Each MSM measurement consists of a set of stress times ranging from 100ns, 1μs, 10μs,... to 200ks and recovery times after each stress period of up to 100ks. Fitting the measurement data with the integral of the activation energy map over all charged defects we obtain the model parameters for the analytic activation energy map $\Delta V_{th}$, $\mu_{ne}, \mu_{de}, \sigma_{e}, \sigma_{de}, T$, and $\tau_p$ for the temperature dependence for the recovery as well as the permanent component.

To analyze the physical nature of the defects responsible for the positive as well as the negative $\Delta V_{th}$, spectroscopy on individual defects like for NBTI in Si devices would be mandatory [23]. Presently such measurements are not yet available, thus we refrain from speculations on the physical origin of these effects. Independent of the physical nature, commonly accepted facts are:

- Under positive gate bias, there is capture or trapping of negative charge in the oxide or interface leading to a positive $\Delta V_{th}$. This effect is accelerated with increasing gate voltage and referred to as positive bias temperature instability (PBTI).
- Under negative gate bias, there is capture or trapping of positive charge in the oxide or interface leading to a negative $\Delta V_{th}$. This effect is accelerated with decreasing gate voltage and referred to as negative bias temperature instability (NBTI).
- Recovery after both positive and negative gate bias stress occurs when the stress is removed. This recovery is accelerated when the voltage is switched into the direction opposite to the stress voltage.

In the following, we will present CET maps modeling the $\Delta V_{th}$ after positive and negative gate bias stress, independently and we will call these PBTI and NBTI CET map, respectively.

IV. POSITIVE DC GATE STRESS MEASUREMENTS

In Fig. 2, we compare the $\Delta V_{th}$ of SiC-MOSFETs after positive gate bias stress with the $\Delta V_{th}$ of Si-MOSFETs with the same gate oxide thickness $t_{ox}$ and same oxide field $E_{ox}$. SiC-MOSFETs show generally a lower $\Delta V_{th}$ due to a lower trap density compared to SiC. SiC-MOSFETs show a higher, but fast recovering $\Delta V_{th}$ with a peculiarity that is only visible at short measurement delays: The measured $\Delta V_{th}$ at lower temperatures is higher than at high temperatures. Due to the thermal activation, emission time constants of traps around 1μs at $T=25°C$ decrease with increasing temperature and become shorter than the measurement delay at $T=175°C$. The fast onset of $\Delta V_{th}$ after short stress times (see Fig. 2a)) is due to the many defects with short capture time constants. Since the traps with short capture time constants ($\tau_c \approx 1\text{ms}$) also have short emission time constants ($\tau_e \ll 1\text{ms}$), the $\Delta V_{th}$ vanishes as quickly as it appears within milliseconds (see Fig. 2, right).

We obtain the activation energy map from fits to the measurement data with all recovery measurements of stress times from 100ns up to 200ks at $T=25°C$ and $T=175°C$ and determine $\tau_{em} = \tau_{em,0} = 10^{-15}$s. The solid lines in Fig. 2 correspond to calculations with the activation energy map shown in Fig. 3a). The corresponding PBTI CET maps for each temperature are shown in Fig. 4. The measurement windows of the DC measurements are indicated in Fig. 3a) with the blue ($T=25°C$) and red ($T=175°C$) rectangles.

We observe for SiC that many traps have very short capture and emission time constants, also below 1μs. The correlation between the capture and emission activation energies for the charged trap density of the recoverable defects described in (1) is $r=1$, whereas the correlation of the more permanent defects (with capture times bigger than e.g. 10s at $T=175°C$) is $r=0$.

The charged trap occupation map for a stress time of 200ks and a measurement delay of 1μs is shown in Fig. 3 b). After 200ks stress, trap centers within area 1-3) at $T=25°C$ and within area 1-6) at $T=175°C$ are charged. With a measurement delay of 1μs, defects within area 1) at $T=25°C$ and within area 1, 2, 4 and 5) at $T=175°C$ are already recovered within the measurement delay. Comparing the defect densities in Fig. 3a) of area 2) and area 6) we observe that the defect density within area 2) is higher than within area 6). Therefore the measured $\Delta V_{th}$ at $T=25°C$ is higher than at $T=175°C$ for short recovery times. Defects within area 6) have longer emission times, whereas defects within area 2) quickly recover. This behavior can be seen in Fig. 2 on the right, where the recovery at lower temperatures occurs faster than at higher temperatures.
course thermally activated, thus the remaining component is increasing towards short time constants (see Fig. 24, 25). For SiC, in contrast, the density of the recoverable component is observed. A higher temperature acceleration according to (2). Recovery is also thermally activated (note that all emission time constants in Fig. 3 and Fig. 4 are shorter than their corresponding capture time constants) so the remaining \( \Delta V_{\text{th}} \) after a measurement delay <1ms is less at high temperature than at low temperature. We have shown that this seemingly paradoxical dependence of \( \Delta V_{\text{th}} \) on the recovery time and temperature can be well understood with the PBTI CET maps. To demonstrate the validity of the PBTI CET map models and their temperature dependence, we compare \( \Delta V_{\text{th}} \) after the same stress time and voltage after high and low temperature stress with the \( \Delta V_{\text{th}} \) after high temperature stress with recovery at room temperature (green circles in Fig. 5 the red and blue circles correspond to the data as shown in Fig. 2 on the right). To measure the recovery at \( T=25°C \) after \( T=175°C \) stress, the sample is cooled down with bias applied after the high temperature stress [26], such that during the one hour cool-down the \( \Delta V_{\text{th}} \) is not recovering.

To summarize: Charge capture due to gate stress is of course thermally activated, thus \( \Delta V_{\text{th}} \) increases with temperature and we obtain \( \tau_{\text{th}} = \tau_{\text{th,p}} = 10^{-15}s \). The temperature dependence is fully described by the Arrhenius temperature acceleration according to (2). Recovery is also thermally activated (note that all emission time constants in Fig. 3 and Fig. 4 are shorter than their corresponding capture time constants), so the remaining \( \Delta V_{\text{th}} \) after a measurement delay <1ms is less at high temperature than at low temperature. We have shown that this seemingly paradoxical dependence of \( \Delta V_{\text{th}} \) on the recovery time and temperature can be well understood with the PBTI CET maps. To demonstrate the validity of the PBTI CET map models and their temperature dependence, we compare \( \Delta V_{\text{th}} \) after the same stress time and voltage after high and low temperature stress with the \( \Delta V_{\text{th}} \) after high temperature stress with recovery at room temperature (green circles in Fig. 5 the red and blue circles correspond to the data as shown in Fig. 2 on the right). To measure the recovery at \( T=25°C \) after \( T=175°C \) stress, the sample is cooled down with bias applied after the high temperature stress [26], such that during the one hour cool-down the \( \Delta V_{\text{th}} \) is not recovering.

To provide a complete modeling approach for \( \Delta V_{\text{th}} \) DC as well as the long-term AC stress considering the full stress-history, the activation energy map has to be extended to include also the stress voltage dependence [27]. We therefore compare \( \Delta V_{\text{th}} \) at three different voltages and observe a power-law like dependence for long stress times (see Fig. 6 on the left) for a measurement delay of 1μs (circles). \( \Delta V_{\text{th}} \) increases linearly with stress voltage whereas the power-law exponent for all voltages remains constant. The dependence of \( \Delta V_{\text{th}} \) on the recovery time (see Fig. 6 on the right) for all three voltages already indicates that the distribution of the capture and emission time constants does not change significantly with the stress voltage, but the number of active traps increases.

A similar observation was made in [20] for Si, where the strong bias dependence of the individual traps did not directly translate into the distribution of time constants. The reason for this is that with different gate bias also the energetically available traps in the oxide changes [28].

To model this voltage dependence, we extended the model for the activation energy maps: The amplitudes of each component \( A_v \) are modeled to linearly increase with stress voltage \( V_{\text{stress}} \) as \( A_v = A_0 + m V_{\text{stress}} \) with the constants \( m \) and \( A_0 \). Furthermore, previous studies on individual defects
on Si have shown [23] that the mean value \( \mu_c \) of each distribution is expected to linearly decrease with increasing stress voltage (capture times decrease with increasing stress voltage, emission times remain unaffected). We thus model the linear decrease of \( \mu_c \) with increasing stress voltage by \( \mu_c = \mu_{c,0} - k V_{\text{stress}} \). With \( \mu_{c,0} \) the mean value of the activation energy constants for the charge capture at 0V and \( k \) the voltage acceleration constant.

Since the emission times remain unaffected by the stress voltage, we have to increase \( \Delta \mu_e \) accordingly: \( \Delta \mu_e = \Delta \mu_{e,0} + k V_{\text{stress}} \). The results calculated with the voltage dependent activation energy map for each voltage are shown as lines in Fig. 6 and show a very good agreement with the measurement data (circles). The obtained voltage model parameters are \( m_e = 0.42 V^{-1}, m_p = 0.08 V^{-1}, k_e = 0.032 eV/V \) and \( k_p = 0.003 eV/V \). We observe a stronger voltage dependence of the amplitude and mean values for the recoverable component than for the more permanent component, which has also been observed for Si [29].

Lifetime estimation according to the JEDEC [30] procedure allows a measurement delay of 48 hours which is clearly inappropriate for SiC, because of the strong recovery dependence and the negligence of the fast recovering components. With the use of PBTI CET maps, all parameters needed for lifetime predictions are provided and the measurement delay is considered within the model. An important aspect to consider is the fact that SiC MOSFETs are typically operated with e.g. bipolar AC voltages or negative DC gate voltage. Since threshold voltage shifts due to negative stress voltages dominate the \( \Delta V_{\text{th}} \) under bipolar AC gate signals, it is of particular importance to analyze and model the threshold voltage after negative gate bias stress.

V. NEGATIVE DC GATE STRESS MEASUREMENTS

The previously observed sub-threshold hysteresis seen in the difference in the sub-threshold regime of IV-curves up-sweep and down-sweep measurements explained in [10] is also caused by the negative gate stress. Due to the longer measurement delay (compared to our 1\( \mu \)s), the negative \( \Delta V_{\text{th}} \) has already recovered when measuring \( V_{\text{th}} \).

Our advanced measurement technique provides additional information on the time-dynamics determined by the capture and emission time constants also after negative DC stress. We observe a large and very fast negative \( \Delta V_{\text{th}} \) under negative gate bias stress (see Fig. 7). The negative \( \Delta V_{\text{th}} \) already saturates after 100s at T=175°C and we observe a decrease of the saturation stress time with increasing temperature. In addition, the recovery after negative stress is also fast and the complete negative \( \Delta V_{\text{th}} \) has recovered within less than 100s. We apply the same concept as for the PBTI CET maps to the negative gate bias MSM measurements as seen in Fig. 7 with full recovery after each stress step and calculate the NBTI CET map for \( V_{\text{g}}=5V \). The NBTI CET maps for each temperature are shown in Fig. 8 (T=25°C on the left, T=175°C on the right). Obviously, the density of traps with small capture and emission time constants is very high for negative DC stress. In contrast to the PBTI CET maps, the distribution of the traps does not contain a permanent component and the emission time constants are narrowly distributed.

The temperature dependence is slight, but due to the logarithmic color scale it becomes apparent that the distribution of the capture and emission time constants at T=25°C is broader than at T=175°C. Furthermore, the capture time constants are wider distributed than the emission time constants. Here, the temperature difference is mainly visible in a longer stress time to saturation \( t_{\text{sat}} \) (T=25°C \( t_{\text{sat}} \approx 10000 \)s, T=175°C \( t_{\text{sat}} \approx 100 \)s). We observe a crossing of the \( \Delta V_{\text{th}} \) recovery for the short stress times (e.g. 1\( \mu \)s in Fig. 7), due to slower recovery at T=25°C than T=175°C. These temperature dependencies can be also explained with Arrhenius temperature acceleration activation energies for charge capture and charge emission are below 100meV.

In earlier publications [14, 19], we have also shown measurements with \( V_{\text{g}}=10V \), where the negative \( \Delta V_{\text{th}} \) is doubled compared \( V_{\text{g}}=5V \) and saturation occurs already after 10\( \mu \)s. Comparing the results, we observe that the density of traps also shows a strong voltage dependence. Modeling this negative stress voltage dependence is work in progress.

In addition to the stress voltage dependence of the capture time constants, there is also a dependence of the emission time constants on the recovery voltage. In particular, it is necessary to study the time-constants of the recovery with recovery voltage for negative as well as positive stress to provide a model for the bipolar AC stress with variable voltage levels.

\[ \text{Fig. 7: Threshold voltage shift after negative stress and its recovery at (} V_{\text{g}}=-5V/ V_{\text{th}} \text{) at } T=25°C \text{ and } T=175°C \text{. Shown is on the left the saturation of } V_{\text{th}} \text{ after stress at } V_{\text{g}}=-5V \text{ with increasing stress time (symbols correspond to the measurement data with a measurement delay of 1}\mu\text{s). The recovery time to return to the initial } V_{\text{th}} \text{ at } V_{\text{g}}= V_{\text{th}} \text{ (right) is shown for } t_e=1\mu\text{s (triangles)} \text{ and } t_e=10\text{ks (circles)} \text{ and is shorter than 100ks for both temperatures. The solid lines are simulations obtained by the NBTI CET maps shown in Fig. 8.} \]

\[ \text{Fig. 8: NBTI capture and emission time map (} V_{\text{g}}=5V/ V_{\text{th}} \text{) at a) } T=25°C \text{ and b) } T=175°C \text{ obtained by fits according to eq. (1) to MSM measurements as shown in Fig. 7. with recovery traces for stress-times from 100ns up to 100ks. The charged trap density } g \text{ is shown in dependence of the capture and emission activation energies and is normalized to 1 using } \log_{10}(1+k) \text{ max}(g) / \log_{10}(1+k) \text{ with } k=100 \text{ to emphasize all details [20]. Max}(g)=23.7V/eV^2, \text{ which corresponds for } T=175°C \text{ to } \max(g)=1.5V/\text{decade}^2. \text{ Activation energies for charge capture and charge emission are below 100meV.}\]
VI. AC MEASUREMENT RESULTS

In the next step, we study the threshold voltage hysteresis introduced by an application-like bipolar AC gate signal with a frequency of 50kHz for different V_{high} and V_{low} combinations (see Fig. 12 a-d). 50kHz is a common frequency for applications of SiC MOSFETs. The goal of these measurements is to measure the hysteresis and compare the results to our CET map simulation approach. We will demonstrate in Chapter VII that combining the PBTI CET map (Fig. 3) and the NBTI CET map (Fig. 8), we are able to model the V_{th} hysteresis, which can be used as add-on in circuit simulators.

To measure the behavior of V_{th} in real-time during the AC stress, we interrupt the AC stress at different positions in time during the AC signal (see Fig. 11b).

The full V_{th} recovery (1μs up to 10ms) back to the initial V_{th} can be seen in Fig. 11c) for each interruption of the AC gate signal. The measurement – keeping V_{g} at V_{th} for 10ms – disrupts the trap occupation state caused by the bipolar AC signal. To fully restore the pre-measurement trap occupation state before each interruption of the AC gate signal 100ns of AC stress is applied (see Fig. 11a). This is long enough to fully restore the trap-occupation state and short enough that only the traps with short capture and emission times are activated. Applying another AC stress of 100ms does therefore not increase the long-term V_{th}, because no slowly recovering components are activated.

The most relevant part of these measurements is the hysteresis at the shortest possible measurement delay of 1μs, so in Fig. 11d), the first measurement points of a V_{th} recovery trace are shown with respect to their timing position during the AC signal. In Fig. 12a) and b), the measured V_{th} at T=175°C during a 50kHz AC signal is shown for two different V_{high} (5V and 20V) with ten V_{low} combinations ranging from 0 to -10V. Short-term hysteresis of the threshold voltage of up to 4V is observed (see Fig. 12b) for V_{low}~10V and V_{high}=20V. The fast decrease in V_{th} during negative gate stress is caused by the previously described capture of holes with capture times below 1μs dependent on the negative gate voltage [14].

For Si MOSFETs the short-term threshold hysteresis during AC stress amounts only to a few mV, due to a very small portion of traps with short capture and emission time constants. The capture times of SiC for hole capture are a lot faster than for electron capture, which is visible in the fast saturation during the V_{low} signal (compare to electron capture in Fig. 2). Furthermore, the saturation under V_{low} bias is accelerated with decreasing V_{low} and almost independent of V_{high}. On the other hand the increase in V_{th} during the V_{high} signal is both due to the acceleration of the negative ΔV_{th} recovery with increasing V_{gate} and also due to the capture of electrons during positive gate bias stress (see Fig. 9).

We performed measurements for the different V_{high} and V_{low} combinations also at T=25°C with the same qualitative observations as for the measurements at T=175°C (see Fig. 12c) and d). The initial V_{th} at T=25°C is higher due to the intrinsic temperature dependence of the threshold voltage.

![Fig. 9: Recovery from negative stress (V_{gate}=-10V, t_s=10ms) at T=25°C and T=175°C. Shown is the required time at V_{th} to recover V_{th} back to a value of 3.5V. The required time decreases exponentially with increasing recovery voltage (dashed lines), the charge emission at operation voltage occurs within 100ns after switching to a positive V_{g}.](image)

However, the NBTI and the PBTI CET maps are obtained with V_{dec} = V_{th} and are thus not directly applicable. For the calculation of the occupation probability map when switching from negative to positive gate voltage, the accelerated recovery of the negative ΔV_{th} with increased recovery voltage has to be considered.

Conversely, when switching from positive to negative gate voltage, the accelerated recovery of the positive ΔV_{th} with increased recovery voltage has to be considered. In Fig. 9, we show the recovery time of V_{th}, after negative stress back to the initial V_{th} as a function of the recovery voltage. Most of the negative ΔV_{th} disappears within ~100ns after switching V_{gate} back to positive bias (see Fig. 9). The recovery time depends exponentially on the gate voltage during recovery. In these first 100ns the negative ΔV_{th} actually helps to switch the MOSFET faster into the ON-state than without this ΔV_{th}.

In Fig. 10 (equivalent to Fig. 9), we show the dependence of the recovery voltage on the time it takes V_{th} to recover back to its initial value after positive stress for two exemplary stress times for T=25°C and T=175°C. Applying e.g. -5V after positive stress accelerates the recovery back to the initial V_{th} by more than 8 orders of magnitude in time compared to applying 5V during recovery (dependent on the temperature and positive bias stress time).

These properties have to be considered when performing simulations with the CET maps by correcting the occupation probability map by the corresponding de- or accelerated recovery times.

![Fig. 10: Recovery from positive stress (V_{gate}=25V, t_{meas}=10μs (rectangles) and t_{meas}=1s (circles)) at T=25°C and T=175°C. Shown is the required time at V_{th} to recover V_{th} back to its initial value. The required time decreases drastically with decreasing recovery voltage (dashed lines).](image)
An analysis of all minimum and maximum values of $V_{th}$ during the bipolar AC stress of the different $V_{high}$ and $V_{low}$ combinations can be found in [19]. For the $V_{high}$ phase, the most interesting parameter is the time it takes to reach the maximum value $V_{th}$ during AC stress. With increasing $V_{high}$ the time until saturation decreases. Comparing Fig. 12a) and Fig. 12c), we observe a longer time needed to recover after the negative voltage phase for $T=25^\circ C$, which is due to the broader distribution of the emission time constants at lower temperatures (see Fig. 8). Based on this result, the impact of the hysteresis on circuit operation is studied and modeled in Chapter VII.

VII. SIMULATING SHORT AND LONG TERM AC STRESS

We have shown in Chapters IV and V that $\Delta V_{th}$ under positive and negative gate bias stress contains large fast recovering components. Furthermore, we have demonstrated that we can model the DC $\Delta V_{th}$ using PBTI and NBTI CET maps. The concept of CET maps is especially beneficial for the simulation of short- as well as long-term AC signals. To obtain the $V_{th}$ response to a rectangular AC signal, the occupancy of the CET map has to be evaluated. For a rectangular signal a derivation of the occupancy level of the defects after AC stress can be found in [31]. First, we will explain and discuss the short-term bipolar AC simulation results and compare them to the measurements shown in Fig. 12. In the second part we will present the results from long-term AC measurements and simulations.

For a comparison of the hysteresis simulation results we chose $V_{low}=-5V$ and $V_{high}=25V$ and show the measured and simulated $\Delta V_{th}$ at $T=25^\circ C$ and $T=175^\circ C$ in Fig. 13. The measured hysteresis inherits two temperature dependencies: As already seen in Fig. 1, the negative $\Delta V_{th}$ after 10$\mu$s stress is higher for $T=175^\circ C$ than for $T=25^\circ C$, whereas as seen in Fig. 2, the $\Delta V_{th}$ after 10$\mu$s positive stress is higher for the lower temperature. Combining both effects, the absolute hysteresis is larger for $T=175^\circ C$ than for $T=25^\circ C$. Due to the bipolar AC stress, the simulation results are obtained by the superposition of the negative and positive $\Delta V_{th}$ calculated using the corresponding PBTI and NBTI CET maps.

The negative $\Delta V_{th}$ during the $V_{low}$ signal and its recovery during the $V_{high}$ signal phase can be simulated with the NBTI CET map shown in Fig. 8 a) for $T=25^\circ C$ and b) for $T=175^\circ C$. In addition, the accelerated recovery of the negative $\Delta V_{th}$ with increased recovery voltage has to be considered when switching from negative to positive gate voltage (see Fig. 9).

The positive $\Delta V_{th}$ during the $V_{high}$ signal and its recovery during the $V_{low}$ gate signal can be modeled with the PBTI CET map shown in Fig. 4. As seen in Fig. 10, the recovery of the positive $\Delta V_{th}$ is highly accelerated with decreased recovery voltage of -5V (compared to $V_{th}$ in Fig. 2), so the contribution of the positive $\Delta V_{th}$ to the $V_{th}$ hysteresis during the $V_{low}$ signal phase can be neglected. The simulated hysteresis, shown in Fig. 13, with the superposition of the contribution of both the positive and negative $\Delta V_{th}$ shows an excellent agreement with
the measurement results. With the knowledge of all temperature and voltage dependencies of both the NBTI and PBTI CET maps, we provide a very good and accurate approach for the consideration of the hysteresis in circuit simulators.

Another important application of the CET maps is the calculation of the $\Delta V_{th}$ after long-term AC stress. In Fig. 14 we compare the measurements of $\Delta V_{th}$ after DC stress at two different temperatures ($25^\circ\text{C}$ and $175^\circ\text{C}$) to the $\Delta V_{th}$ after AC stress with $V_{\text{high}}/V_{\text{low}}$ 25V/5V as well as the 25V/0V at $T=175^\circ\text{C}$ at a frequency of 50kHz.

The $\Delta V_{th}$ after AC stress is measured directly at the end of the high voltage period with a measurement delay of 1μs. We observe that $\Delta V_{th}$ after AC conditions 25V/5V as well as AC 25V/0V have the same power-law exponent as the DC stress (see Fig. 14 on the right). Simulation results are obtained by the PBTI CET maps shown in Fig. 4. The AC simulations can be directly obtained by the multiplication of the PBTI CET map at $T=175^\circ\text{C}$ with the defect occupancy map for the corresponding AC stress pattern. For $V_{\text{low}}=0$V, additionally the recovery acceleration with decreasing recovery voltage has to be considered (see Fig. 10). The acceleration of the relaxation during the AC stress $V_{\text{low}}$ period leads to a lower degradation after AC 25/0V AC stress than at 25/5V. We achieve a very good agreement of all PBTI CET map simulations (shown as lines in Fig. 14) and the measurement data of the AC stress, which is mainly limited by sample to sample variation.

Fig. 14: Simulation (lines) from PBTI CET map (shown in Fig. 4) and measurements of $\Delta V_{th}$ after 25V DC $T=25^\circ\text{C}$ and DC $T=175^\circ\text{C}$, 25V/AC and 25V/0V AC gate stress at $T=175^\circ\text{C}$ (linear scale on the left, log scale on the right). Measurement delay is 1μs. The AC measurements were performed at a frequency of 50kHz and a duty cycle of 50% equivalent to alternating 1μs. The solid lines are simulations obtained from the PBTI CET map. To simulate the 25V/0V AC signal the stress time $t_\text{st}$ = 10μs and the equivalent recovery time $t_\text{rec} = 3 \cdot t_\text{rec}_{V_{\text{high}}}$.

To understand the impact of each component of the PBTI CET map, we show in Fig. 15 the evolution of the recoverable and more permanent component of $\Delta V_{th}$ within the 25/5V AC stress (same data as red circles in Fig. 14, $T=175^\circ\text{C}$, f=50kHz). The solid black line shows the contribution of the more permanent defects of the PBTI CET map (see Fig. 4), whereas the black dashed line corresponds to the contribution of the recoverable defects. Already after 1ms AC stress, the contribution of the recoverable defects does not increase any more – these defects contribute to the short-term hysteresis also shown in the inset in Fig. 15. The dashed red lines correspond to the simulated $\Delta V_{th}$ at the end of the low voltage period. Furthermore, the highlighted red area marks the constant charging and discharging of the defects, which is the short-term hysteresis, within the long-term AC stress. In contrast, the contribution of the more permanent defects, as expected, increases with AC stress time. The hysteresis does not increase for the long-term AC stress which has been verified with hysteresis measurements before and after the AC stress. To conclude, we have demonstrated that the concept of analytic CET maps can be used to predict the temperature and voltage dependence of DC SiC positive gate bias stress with a very high accuracy. Moreover the analytic CET map is also a valuable method to simulate different short as well as long-term AC gate stress signals.

VIII. IMPACT ON CIRCUIT OPERATION AND VERIFICATION

For Si, the $V_{th}$ hysteresis during a bipolar AC signal amounts to only a few mV and is uncritical. For SiC, the short-term threshold voltage hysteresis mainly due to negative gate bias has been already observed the measurement of IV-curves in a shift of the subthreshold voltage [4]. Fortunately, this effect is not permanent and recovers quickly within a fraction of the positive gate bias pulse. Also, the threshold voltage hysteresis itself does not increase after end of life.

In real applications in contrast to the measurement the portion of $\Delta V_{th}$ which is recovered within the measurement delay is still active during the application [14]. The amount can be estimated from CET maps, but the estimation is based only on extrapolations and not on experimental data. Therefore, we also perform recovery-free on-the-fly measurements to study the impact of $\Delta V_{th}$ on $R_{\text{on}}$ during application conditions.
In Fig. 16 we present the measured $R_{on}$ during the $V_{\text{high}}$ period (transistor is “on”) of the AC stress for different $V_{\text{low}}$ voltages. For the comparison of $R_{on}$ with $\Delta V_{\text{th}}$, we use a temperature of $T=25^\circ \text{C}$, because the impact of $\Delta V_{\text{th}}$ on $R_{on}$ at high temperatures decreases due to the temperature dependence of $R_{on}$ and the decreasing transconductance. Furthermore, we chose $V_{\text{high}}=10\text{V}$ because at higher gate voltages (i.e. 15V) $\Delta V_{\text{th}}$ recovers too fast to cause a clearly measurable change in $R_{on}$ (see Fig. 9). Fig. 16 shows that the dependence of $R_{on}$ during AC stress is only correlated to the observed $\Delta V_{\text{th}}$ during AC stress and shows the same dependencies as $\Delta V_{\text{th}}$ in Fig. 12. As a matter of fact, $R_{on}$ is actually lower after negative gate stress which helps to minimize static losses. The measured $\Delta V_{\text{th}}$ during AC stress at $T=25^\circ \text{C}$ and $V_{\text{high}}=10\text{V}$ is used to calculate the change in $R_{on}$ using the static $I_d-V_g$ curve in the linear regime ($R_{on}$ dependent on the gate voltage) as reference. The observed $\Delta V_{\text{th}}$ can be directly mapped to $R_{on}$ (see circles in Fig. 16) with a perfect agreement. The $R_{on}$ increases back to its initial value with recovering $V_{\text{th}}$. An even lower $R_{on}$ in Fig. 16 is expected for $t \leq 1\mu\text{s}$ (not shown in Fig. 16 due to finite settling time of measuring amplifier). Note that $\Delta V_{\text{th}}$ is the only reason for $\Delta R_{on}$ and can completely explain the changes in magnitude. Possible changes in the mobility apparently do not play a role. This has three highly positive conclusions: First, we can perfectly explain and model the change in $R_{on}$ due to the hysteresis has no harmful effect when the MOSFET works in a switch-mode converter, because $R_{on}$ is actually lowered during the negative period of the AC stress and therefore helps to switch the SiC-MOSFET faster, thus minimizing dynamic losses.

IX. CONCLUSIONS

Utilizing a fast measurement technique, that is, short stress pulses (100ns) and continuously measured recovery from $\mu$s to 100ks, we are able to determine the time constants for capture and emission of positive and negative charges as a function of the applied bias. We developed a simulation approach for modeling of $\Delta V_{\text{th}}$ under positive as well as negative gate bias stress using capture and emission time maps. We have shown that both the positive and negative gate bias stress contain large quickly recovering components, which remain undetected during JEDEC-like tests as being defined for silicon devices [30]. Due to the temperature dependence, also of the fast recovery after positive gate bias stress, we observed a higher $\Delta V_{\text{th}}$ for low temperatures than for higher temperatures. Therefore, we propose to cool down the sample with bias applied prior to measuring the recovery.

An alternative to the standard JEDEC test is to use a preconditioning approach [12], which eliminates the contribution of the fast recovering part of the negative as well as the positive $\Delta V_{\text{th}}$. With this approach the lifetime parameter dependence on the measurement delay is drastically reduced, but information about recovering components in the sub millisecond regime is lost. To completely investigate the impact of the fast recovering components, we propose utilizing gate bias stress occurring in the application (negative DC and AC only) and a shortest possible measurement delay (e.g. 1$\mu$s).

We have also presented a method using a bipolar AC gate bias stress, which is application-relevant and can simulate any AC/DC stress sequence or history, exactly like in the application. Our measurements show that applying a bipolar AC gate bias stress causes large and very fast fully recoverable threshold hysteresis as seen before in [4] with magnitudes up to 4V.

Combining the NBTI and PBTI CET maps obtained by the DC stress measurements, we can perfectly explain and model this behavior. During the negative gate phase $\Delta V_{\text{th}}$ is due to capture of positive charges in the oxide and at the interface. During the positive gate phase the positive charges are neutralized and negative charges are captured. Our model additionally includes the recovery voltage dependence of the positive and negative charge emission. With this modeling approach we are able to model the threshold voltage hysteresis during normal operation and provide it as an add-on to a standard SPICE model for circuit simulations.

Furthermore, we have demonstrated that the AC long-term measurements can be simulated with good accuracy by the analytic CET maps enabling lifetime modeling after an arbitrary stress signal. Results and predictions of the analytic CET maps are considering the measurement delay and thus eliminating the influence of the measurement delay on the $\Delta V_{\text{th}}$ prediction.

We have also shown that the change in $R_{on}$ is only due to the $\Delta V_{\text{th}}$ change during AC stress which is fully recoverable just like the $\Delta V_{\text{th}}$. It is also demonstrated that the change in $R_{on}$ due to the hysteresis has no harmful effect when the MOSFET works in a switch-mode converter, because $R_{on}$ is actually lowered during the negative period of the AC stress and therefore helps to switch the SiC-MOSFET faster while minimizing static losses and temperature increase of the device.

X. REFERENCES


