Understanding and Modeling Transient Threshold Voltage Instabilities in SiC MOSFETs

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***Abstract*—Modeling of the threshold voltage instabilities in SiC power MOSFETs is difficult due to the fast recovery of ΔV_{th} after positive and negative gate bias stress. This work investigates the capture- and emission-time constants of positive and negative charge trapped in the gate oxide and at the interface as a function of gate bias and temperature. We present a measurement technique which enables time-resolved measurements of the real V_{th} during application-relevant bipolar AC high temperature gate stress (HTGS). We use capture and emission time (CET) maps to model the temperature and voltage dependence of the ΔV_{th} after positive as well as negative gate stress. In addition, we provide a complete modeling approach for the ΔV_{th} after long-term AC stress considering the full stress-history. Furthermore, we present a very accurate model for the short-term hysteresis during a bipolar AC period and we show that the threshold voltage hysteresis has no harmful effect on switching operation in real applications.**

***Index Terms*—BTI, CET, HTGS, Hysteresis, SiC**

I. Introduction

Due to the higher breakdown field, high voltage power MOSFETs made of SiC allow much smaller geometries compared to Si MOSFET with the same on-resistance R_{on} and voltage class [1–3]. As a consequence, lower losses in switch mode converters enable higher operating frequencies and/or higher efficiencies [4]. On the other hand, short-term threshold (V_{th}) hysteresis under AC-gate bias as well as long term ΔV_{th} in SiC-MOSFETs are significantly higher than the ones observed in Si-MOSFETs [5–7]. The threshold voltage hysteresis is especially pronounced – with amplitudes in ΔV_{th} up to 4V – in commercially available SiC--MOSFETs from various manufacturers [8–10]. It is clear that such a threshold hysteresis of 4V occurring during switching, which roughly corresponds to 1/3 of the total gate-overdrive, has a substantial influence – but is so far neglected – on SPICE models and thus has to be considered properly. A precondition for a proper consideration of the hysteresis ΔV_{th} is that the dynamics of ΔV_{th}, how it evolves and recovers dynamically under any given gate stress history, are to be determined and known.

There have been several experimental studies on the SiC threshold hysteresis [6, 11–13]. Though these experiments have demonstrated some of the fundamental properties of the threshold hysteresis, they were not designed to provide quantitative data on the sub-millisecond dynamic behavior of ΔV_{th}. For example, they were not able to measure the evolution of ΔV_{th} under a negative gate bias and how fast this ΔV_{th} recovers when the gate is switched to a positive bias, as a function of the magnitudes of these biases and as a function of temperature.

Therefore the primary goal of this paper is to demonstrate an experiment and an extraction method providing all the data and parameters for a model required to extend a SPICE simulation in order to consider this non-constant threshold voltage.

Our model is based on capture and emission time (CET) maps and considers stress and recovery times down to 100ns.Thus it is able the determine the threshold voltage hysteresis under real gate signals, for example under bipolar AC-stress (+15/-5V at 50kHz), as occurring in switching converters. The model is also able to explain the peculiarities which have been observed for SiC such as the seemingly unphysical temperature dependence of ΔV_{th} after DC-stress and the dependence of the measurement delay on the voltage acceleration factor of ΔV_{th} [14].

Since the measuring technique is key to achieve the above goals, we discuss the parameters of our measurement setup in detail in Section II. A short general introduction into the "CET-methodology" will be given in Section III. The results of our measurements, divided in positive and negative DC stress will be discussed in Sections IV and V, respectively. We will furthermore discuss in this section the properties of the CET maps together with consequences, both for positive and negative gate bias stress. Next, the fast threshold hysteresis under AC stress is discussed in Section VI. Section VII and VIII will present the simulation results utilizing the CET maps for short- and long-term AC-stress, together with experimental data, and thus serve as verification of the model.

II. Measurement Setup

The samples used in this study were packaged SiC trench MOSFETs with a rated $V_{ds,max}$ of 1200V and a rated $V_{gs,max}$ of +20/-10V. Measuring ΔV_{th} after gate bias stress is difficult due to fast recovery after stress. These difficulties are similar to the problems found one decade ago during studies of the negative bias temperature instability on Si devices [15], although they are much more pronounced on SiC. The new measuring techniques introduced for NBTI were measure-stress-measure (MSM) techniques with fast 1µs measurement delays [16, 17] and recovery-free OTF-techniques (on-the-fly) [18] which do not interrupt the stress but try to determine ΔV_{th} at stress-level. The main differences between SiC-Vth-instabilities and NBTI are:

- Trapping of charges of both polarities at the same time for SiC. Analysis of an observed positive dV_{th}/dt, for example, has to distinguish if this dV_{th}/dt is due to trapping of positive charge or emission of negative charge.
- For SiC the relevance of fast effects is much higher than for any Si-MOSFET (power or logic) [14].

In consequence, the unwanted effect of the measurement delay is more important for the SiC case. In particular, the hysteresis under bipolar gate stress amounts up to 4V while it is only several mV for a Si-MOSFET with comparable gate oxide thickness [19].

To account for the above facts we have developed the setup shown in Fig. 1, which intends to meet the following goals:

- The setup must be able to apply any application-relevant gate-stress-sequence e.g. switches between standby conditions and bipolar AC stress with any frequency and duty-factor.

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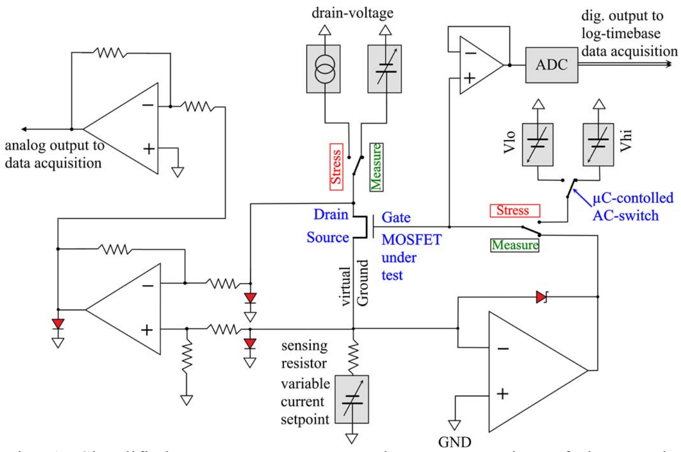

Fig. 1: Simplified measurement setup: The setup consists of three main components: **1)** A stress-signal generator, consisting of DACs generating V_{high} and V_{low} and analog switches driven by the PWM-unit of a µC **2)** an analog measuring unit, consisting of analog switches and an operational amplifier in a feedback loop in order to control V_{gate} in a way to make I_{drain} constant **3)** an "OTF"-measuring unit, consisting of a constant current (≈<1A) fed into drain and a differential amplifier for measuring V_{DS} (corresponding to R_{ON}) during the V_{gate}-on-phase. Most important for fast settling times is that all amplifier inputs/outputs have voltage limiting circuits (represented by diodes in red) to prevent amplifier saturation. All switches are fast solid state analog switches with appropriate on resistance.

- Most important: interruption of stress at any well-defined time, e.g. after 200ns in the high-period (see Fig. 1) and then switch to measure V_{th} with a measurement delay as short as possible.

It should be noted that the amount of ΔV_{th} which recovers during a 1µs measurement delay is more or less insignificant for CMOS logic or Si-power-MOSFETs, as we will demonstrate, is not at all insignificant for SiC. In the real application, for example after the 10µs-on-period, this ΔV_{th} which is recovered during the measurement is still active during the application [14]. The amount can be estimated from CET maps, but the estimation is based only on extrapolations and not on experimental data. This is why our setup, in addition to the MSM-unit also contains an OTF-unit which allows a recovery-free determination of ΔV_{th} via the measurement of the on resistance R_{on}.

With the setup in Fig. 1 we achieve a measurement delay of 1µs. This limit of the measurement delay is due to the value of the drain-current at V_g=V_{th} of ≈1mA, and the values of the capacitances C_{GS} and C_{GD}, which have to be recharged when switching from stress-mode to measure-mode. The resolution in the stress-timing as well as the width of the shortest rectangular stress pulses is 100ns. The resulting accuracy in the stress timing (also for the AC signals) is about ± 20ns. These accuracy limits are mainly determined by the gate capacitance of ≈2nF, the length of the test leads of several cm, together with a missing impedance matching. Thus, our accuracy and lower limit in determining the short time constants of V_{th}-transients under positive or negative gate stress due to capturing or emitting charge is about ±20ns.

A setup with commercial instruments, e.g. a pulse- or arbitrary wave-form-generator together with commercial SMU's, would be able to fulfil the above measurement goals. Unfortunately, commercial instruments in general do not provide any "bare-metal programming" which would be necessary just to provide, for example, the required tight synchronization of wave-form-generator and SMU(s). Moreover, the setup in Fig. 1 is quite inexpensive, and a couple of setups can be fit into a single rack and be controlled by a single computer.

III. CAPTURE AND EMISSION TIME MAP

We have shown in [14] that as for both Si and SiC, the threshold voltage shifts due to BTI can be well understood as the collective response of an ensemble of independent defects with the two defect states being charged and uncharged. The CET maps contain the required information about the kinetics of charge capture and emission [20]. Charge exchange and the correlated activation energies can be described in consistence with previous work on Si as the sum of two bivariate Gaussian distributions [20]: one distribution for the defects having short capture and emission times (called recoverable component) and one for the charged defects having emission times mostly permanent in typical experimental time windows from capture and emission times 1µs to 100ks. We denote the recoverable and more permanent component in the following with subscript r and p, respectively.

The main parameters of this analytic density distribution $g(E_c, E_e)$ are the mean values μ_c and $\mu_{\Delta e}$ of the capture and emission activation energies $E_{a,c}$ and $E_{a,e}$ with their standard deviations σ_c and $\sigma_{\Delta e}$. σ_c and $\sigma_{\Delta e}$ correspond to the width of the distributions in both directions ($E_{a,c}$, $E_{a,e}$ see Fig. 3). Furthermore, the emission activation energies $E_{a,e}$ increase with larger capture activation energies $E_{a,c}$: $E_{a,e} = E_{a,c} + \Delta E_{a,e}$. An implicit correlation between the standard deviations $\sigma_e^2 = r \cdot \sigma_c^2 + \sigma_{\Delta e}^2$ as explained in [21] is used, where r denotes the correlation between the capture and emission activation energies. If $r = 0$, the angle of the orientation of the distribution is 0 (no correlation) and if $r = 1$ the angle is 45° (correlation, compare Fig. 3). Thus the charged trap density $g(E_c, E_e)$ for each component with amplitude A is given by

$$g(E_c, E_e) = \frac{A}{2\pi\sigma_c\sigma_{\Delta e}} \cdot exp\left(-\frac{(E_c-\mu_c)^2}{2\sigma_c^2} - \frac{\left(E_e-(rE_c+\mu_{\Delta e})\right)^2}{2\sigma_{\Delta e}^2}\right) \quad (1).$$

The threshold voltage shift, for a given stress- and recovery-time is obtained as the integral of the activation energy map over all defects (recoverable and permanent) being charged up to the stress time and not yet being discharged at the recovery time. For Si, the temperature activation of the capture and emission times of a single trap are commonly modeled according to the Arrhenius equation [22]:

$$E_{a(c,e)} = k_B T \cdot \ln\left(\frac{\tau}{\tau_0}\right) \quad (2).$$

The decrease of the capture and emission time constants with temperature can then be described as:

$$\tau_2 = \tau_o \cdot \left(\frac{\tau_1}{\tau_0}\right)^{\frac{T1}{T2}} \quad (3)$$

with τ_2 the transformed capture/emission time constant at temperature T_2, τ_1 the capture/emission time constant at temperature T_1, and τ_0 the time constant for infinite temperature.

The activation energy map is therefore a temperature-independent map and the capture and emission time maps at any constant temperature can be calculated from the activation energy map using (2) with the two characteristic temperature-independent constants, $\tau_{0,r}$ for the recoverable and $\tau_{0,p}$ for the more permanent defects.

To obtain the temperature and voltage dependent activation energy map, MSM measurements at different temperatures and voltages have been performed. Each MSM measurement consists of a set of stress times ranging from 100ns, 1µs, 10µs,… to 200ks and recovery times after each stress period of up to 100ks. Fitting the measurement data with the integral of the activation energy map over all charged defects we obtain the model parameters for the analytic activation energy map A, μ_c, $\mu_{\Delta e}$, σ_c, $\sigma_{\Delta e}$, r and τ_o for the temperature dependence for the recoverable as well as the permanent component.

To analyze the physical nature of the defects responsible for the positive as well as the negative ΔV_{th}, spectroscopy on individual defects like for NBTI in Si devices would be mandatory [23]. Presently such measurements are not yet available, thus we refrain from speculations on the physical origin of these effects. Independent of the physical nature, commonly accepted facts are:

- Under positive gate bias, there is capture or trapping of negative charge in the oxide or interface leading to a positive ΔV_{th}. This effect is accelerated with increasing gate voltage and referred to as positive bias temperature instability (PBTI).
- Under negative gate bias, there is capture or trapping of positive charge in the oxide or interface leading to a negative ΔV_{th}. This effect is accelerated with decreasing gate voltage and referred to as negative bias temperature instability (NBTI).
- Recovery after both positive and negative gate bias stress occurs when the stress is removed. This recovery is accelerated when the voltage is switched into the direction opposite to the stress voltage.

In the following, we will present CET maps modeling the ΔV_{th} after positive and negative gate bias stress, independently and we will call these PBTI and NBTI CET map, respectively.

IV. Positive DC Gate Stress Measurements

In Fig. 2, we compare the ΔV_{th} of SiC-MOSFETs after positive gate bias stress with the ΔV_{th} of Si-MOSFETs with the same gate oxide thickness t_{ox} and same oxide field E_{ox}. Si-MOSFETs show generally a lower ΔV_{th} due to a lower trap density compared to SiC. SiC-MOSFETs show a higher, but fast recovering ΔV_{th} with a peculiarity that is only visible at short measurement delays: The measured ΔV_{th} at lower temperatures is higher than at high temperatures. Due to the thermal activation, emission time constants of traps around 1µs at T=25°C decrease with increasing temperature and become shorter than the measurement delay at T=175°C. The fast onset of ΔV_{th} after short stress times (see Fig. 2a)) is due to the many defects with short capture time constants. Since the traps with short capture time constants (τ_c<1ms) have also short emission time constants ($\tau_e \ll$ 1ms), the ΔV_{th} vanishes as quickly as it appears within milliseconds (see Fig. 2, right).

We obtain the activation energy map from fits to the measurement data with all recovery measurements of stress times from 100ns up to 200ks at T=25°C and T=175°C and determine $\tau_{0,r} = \tau_{0,p} = 10^{-15}$s. The solid lines in Fig. 2 correspond to calculations with the activation energy map shown in Fig. 3a). The corresponding PBTI CET maps for each temperature are shown in Fig. 4. The measurement windows of the DC measurements are indicated in Fig. 3a) with the blue (T=25°C) and red (T=175°C) rectangles.

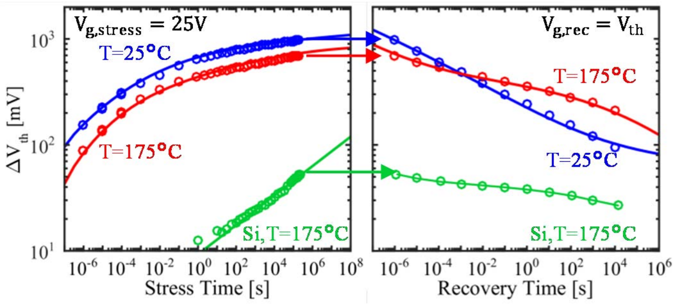

Fig. 2: **Left:** Comparison of SiC and Si-MOSFETs with same t_{ox} and same E_{ox} during positive gate bias stress with 1µs measurement delay. SiC shows higher but fast recovering ΔV_{th} with a reversed temperature dependence compared to Si: ΔV_{th} at lower temperatures (T=25°C) is larger than at higher temperatures (T=175°C). **Right:** Recovery after 200ks stress with the same Fig. stress voltage. Recovery at lower temperatures is faster than at higher temperatures. A crossing of the measured ΔV_{th} is observed at 5ms. The solid blue and red lines in both figures (left and right) show the simulations for each temperature obtained by the analytic activation energy map shown in Fig. 3.

We observe for SiC that many traps have very short capture and emission time constants, also below 1µs. The correlation between the capture and emission activation energies for the charged trap density of the recoverable defects described in (1) is r=1, whereas the correlation of the more permanent defects (with capture times bigger than e.g. 10s at T=175°C) is r=0.

The charged trap occupation map for a stress time of 200ks and a measurement delay of 1µs is shown in Fig. 3 b). After 200ks stress, trap centers within area 1-3) at T=25°C and within area 1-6) at T=175°C are charged. With a measurement delay of 1µs, defects within area 1) at T=25°C and within area 1,2, 4 and 5) at T=175°C are already recovered within the measurement delay. Comparing the defect densities in Fig. 3a) of area 2) and area 6) we observe that the defect density within area 2 is higher than within area 6). Therefore the measured ΔV_{th} at T=25°C is higher than at T=175°C for short recovery times. Defects within area 6) have longer emission times, whereas defects within area 2) quickly recover. This behavior can be seen in Fig. 2 on the right, where the recovery at lower temperatures occurs faster than at higher temperatures.

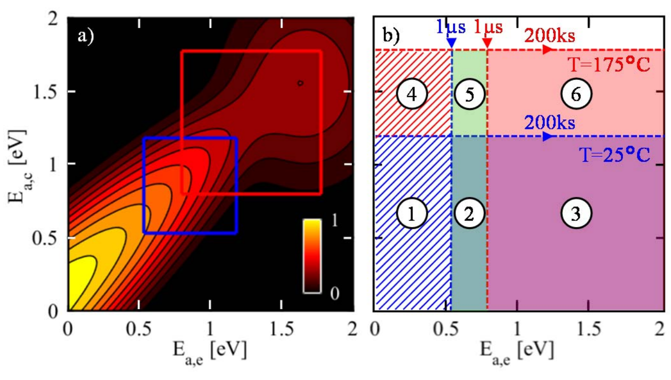

Fig. 3 **a):**Analytic activation energy map obtained with stress and recovery data like the ones shown in Fig. 2 with recovery traces for stress-times from 1µs up to 200ks. The charged trap density g is shown in dependence of the capture and emission activation energies and is normalized to 1 using $\log_{10}(1 + \kappa \cdot \max(g))/\log_{10}(1 + \kappa)$ with $\kappa = 100$ with $\max(g) = 7V/eV^2$ to emphasize all details [20]. The measurement range from 1µs to 200ks is marked in blue for T=25°C and in red for T=175°C. **b)** Charge trap occupation map shown for the DC stress at T=25°C and T=175°C. The blue and red filled rectangle mark the traps that are occupied for a stress time of 200ks and a measurement delay of 1µs. The blue and red patterned areas indicate the region of the activation energy map that is out of the measurement range at T=25°C and T=175°C, respectively. The green region marks the traps that have activation energies which are within the measurement range at T=25°C and are captured when stressing at T=175°C and measuring V_{th} at T=25°C.

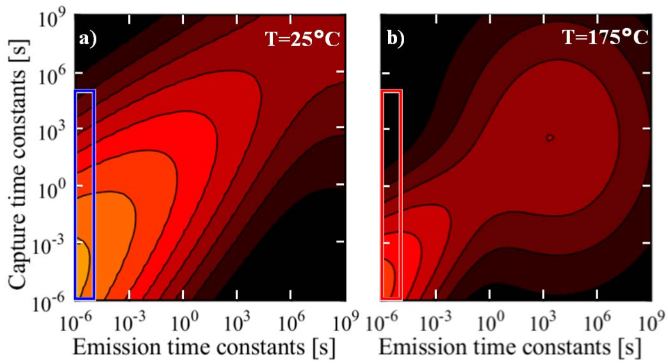

Fig. 4: PBTI Capture and emission time maps (derived from Fig. 3) shown as a function of the capture and emission time constants at a) T=25°C and b) T=175°C with the same normalization and color code as Fig. 3. Fitting the data we obtain the two characteristic temperature-independent constants $\tau_{0,r} = \tau_{0,p} = 10^{-15}$s. The blue and red rectangles mark the defects, that are recovering within the decade of 1µs to 10µs recovery time after 100ks DC stress at T=25°C and T=175°C, respectively, indicated in Fig. 5.

After 5ms recovery time, a crossing of the measured ΔV_{th} is observed. A higher ΔV_{th} at lower temperatures has not been observed for Si, because the defect density in the PBTI CET map increases from short to long capture time constants τ_c [24, 25]. For SiC, in contrast, the density of the recoverable component is increasing towards short time constants (see Fig. 3).

To summarize: Charge capture due to gate stress is of course thermally activated, thus ΔV_{th} increases with temperature and we obtain $\tau_{0,r} = \tau_{0,p} = 10^{-15}$s. The temperature dependence is fully described by the Arrhenius temperature acceleration according to (2). Recovery is also thermally activated (note that all emission time constants in Fig. 3 and Fig. 4 are shorter than their corresponding capture time constants), so the remaining ΔV_{th} after a measurement delay <1ms is less at high temperature than at low temperature. We have shown that this seemingly paradoxical dependence of ΔV_{th} on the recovery time and temperature can be well understood with the PBTI CET maps. To demonstrate the validity of the PBTI CET map models and their temperature dependence, we compare ΔV_{th} after the same stress time and voltage after high and low temperature stress with the ΔV_{th} after high temperature stress with recovery at room temperature (green circles in Fig. 5 the red and blue circles correspond to the data as shown in Fig. 2 on the right). To measure the recovery at T=25°C after T=175°C stress, the sample is cooled down with bias applied after the high temperature stress [26], such that during the one hour cool-down the ΔV_{th} is not recovering.

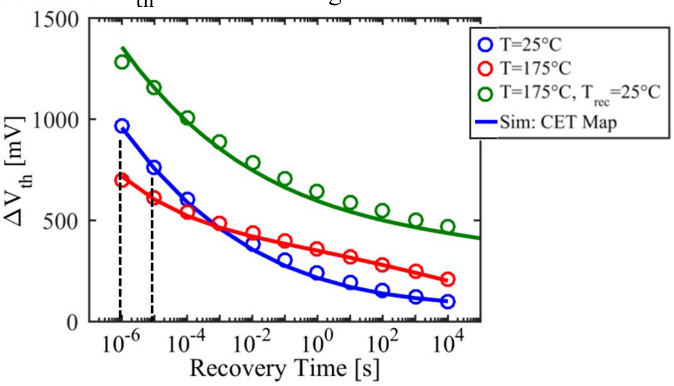

Fig. 5: ΔV_{th} recovery traces after t_s = 200ks at $T_s = T_r$=25°C (blue) and $T_s = T_r$=175°C (red) in comparison with T_s=175°C and T_r=25°C (green). Symbols are experimental data. The solid lines are simulations obtained by the same analytic activation energy map shown in Fig. 3.

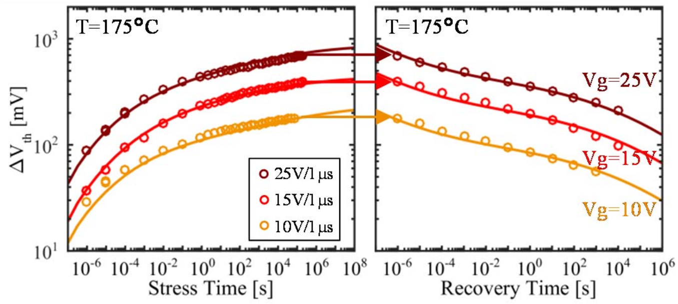

Fig. 6: **Left:** Comparison of ΔV_{th} as a function of stress time at three different voltages with measurement delay 1µs T=175°C. The labels in the legend denote stress voltage and measurement delay. **Right:** Comparison of the recovery after 200ks stress time. The solid lines show the calculations for each voltage obtained by the voltage dependent analytic activation energy map shown for V=25V in Fig. 3.

The simulated ΔV_{th} for this measurement is obtained by the same activation energy map as shown in Fig. 3 taking into account for the occupation map that the recovery is measured at a different temperature than the stress temperature. Measurements and simulations show very good agreement, which demonstrates that the temperature dependence of the PBTI CET maps is correctly modeled and that the difference between the recovery at T=175°C and T=25°C can be fully attributed to the temperature acceleration of the recovery. As an example, the traps recovering within one decade (1µs to 10µs, see dashed lines in Fig. 5) are indicated in Fig. 4 a) and b) for T=25°C and T=175°C, respectively. Therefore, the recovery measurements at high temperature are misleading and information about the short time constants is lost. After 200ks DC stress at T=25°C, barely any charged traps of the more permanent component contribute to ΔV_{th} (see Fig. 3). In fact, the threshold voltage shift after high temperature stress (see green circles) is higher than for room temperature stress (as is also the case for Si). To avoid loss of information and provide a comparability of different stress temperatures, ΔV_{th} after high temperature stress should also be measured at room temperature or even cryogenic temperatures with a measurement delay as short as possible [26]. For lifetime extrapolation, capture and emission time maps should be used in order to properly consider the recovery.

To provide a complete modeling approach for ΔV_{th} DC as well as the long-term AC stress considering the full stress-history, the activation energy map has to be extended to include also the stress voltage dependence [27]. We therefore compare ΔV_{th} at three different voltages and observe a power-law like dependence for long stress times (see Fig. 6 on the left) for a measurement delay of 1µs (circles).

ΔV_{th} increases linearly with stress voltage whereas the power-law exponent for all voltages remains constant. The dependence of ΔV_{th} on the recovery time (see Fig. 6 on the right) for all three voltages already indicates that the distribution of the capture and emission time constants does not change significantly with the stress voltage, but the number of active traps increases.

A similar observation was made in [20] for Si, where the strong bias dependence of the individual traps did not directly translate into the distribution of time constants. The reason for this is that with different gate bias also the energetically available traps in the oxide changes [28].

To model this voltage dependence, we extended the model for the activation energy maps: The amplitudes of each component (A_r and A_p) are modeled to linearly increase with stress voltage V_{stress} as $A = mV_{stress} + A_0$ with the constants m and A_0. Furthermore, previous studies on individual defects on Si have shown [23] that the mean value μ_c of each distribution is expected to linearly decrease with increasing stress voltage (capture times decrease with increasing stress voltage, emission times remain unaffected). We thus model the linear decrease of μ_c with increasing stress voltage by $\mu_c = \mu_{c,0} - kV_{stress}$. With $\mu_{c,0}$ the mean value of the activation energy constants for the charge capture at 0V and k the voltage acceleration constant.

Since the emission times remain unaffected by the stress voltage, we have to increase $\Delta\mu_e$ accordingly: $\Delta\mu_e = \Delta\mu_{e,0} + kV_{stress}$. The results calculated with the voltage dependent activation energy map for each voltage are shown as lines in Fig. 6 and show a very good agreement with the measurement data (circles). The obtained voltage model parameters are $m_r = 0.42V^{-1}$, $m_p = 0.08V^{-1}$, $k_r = 0.032\mathrm{eV/V}$ and $k_p = 0.003\mathrm{eV/V}$. We observe a stronger voltage dependence of the amplitude and mean values for the recoverable component than for the more permanent component, which has also been observed for Si [29].

Lifetime estimation according to the JEDEC [30] procedure allows a measurement delay of 48 hours which is clearly inappropriate for SiC, because of the strong recovery dependence and the negligence of the fast recovering components. With the use of PBTI CET maps, all parameters needed for lifetime predictions are provided and the measurement delay is considered within the model An important aspect to consider is the fact that SiC MOSFETs are typically operated with e.g. bipolar AC voltages or negative DC gate voltage. Since threshold voltage shifts due to negative stress voltages dominate the ΔV_{th} under bipolar AC gate signals, it is of particular importance to analyze and model the threshold voltage after negative gate bias stress.

V. NEGATIVE DC GATE STRESS MEASUREMENTS

The previously observed sub-threshold hysteresis seen in the difference in the sub-threshold regime of IV-curves up-sweep and down-sweep measurements explained in [10] is also caused by the negative gate stress. Due to the longer measurement delay (compared to our 1µs), the negative ΔV_{th} has already recovered when measuring V_{th}.

Our advanced measurement technique provides additional information on the time-dynamics determined by the capture and emission time constants also after negative DC stress. We observe a large and very fast negative ΔV_{th} under negative gate bias stress (see Fig. 7). The negative ΔV_{th} already saturates after 100s at T=175°C and we observe a decrease of the saturation stress time with increasing temperature. In addition, the recovery after negative stress is also fast and the complete negative ΔV_{th} has recovered within less than 100s. We apply the same concept as for the PBTI CET maps to the negative gate bias MSM measurements as seen in Fig. 7 with full recovery after each stress step and calculate the NBTI CET map for V_g=-5V. The NBTI CET maps for each temperature are shown in Fig. 8 (T=25°C on the left, T=175°C on the right). Obviously, the density of traps with small capture and emission time constants is very high for negative DC stress. In contrast to the PBTI CET maps, the distribution of the traps does not contain a permanent component and the emission time constants are narrowly distributed.

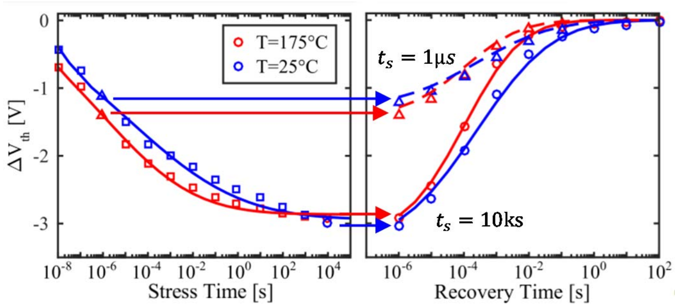

Fig. 7: Threshold voltage shift after negative stress and its recovery at (V_g=-5V/ V_{th}) at T=25°C and T=175°C. Shown is on the left the saturation of V_{th} after stress at V_g=-5V with increasing stress time (symbols correspond to the measurement data with a measurement delay of 1µs). The recovery time to return to the initial V_{th} at V_g= V_{th} (right) is shown for t_s = 1µs (triangles) and t_s = 10ks (circles) and is shorter than 100s for both temperatures. The solid lines are simulations obtained by the NBTI CET maps shown in Fig. 8.

The temperature dependence is slight, but due to the logarithmic color scale it becomes apparent that the distribution of the capture and emission time constants at T=25°C is broader than at T=175°C. Furthermore, the capture time constants are wider distributed than the emission time constants. Here, the temperature difference is mainly visible in a longer stress time to saturation t_{sat} (T=25°C $t_{\mathrm{sat}} \approx 10000s$, T=175°C $t_{\mathrm{sat}} \approx 100s$). We observe a crossing of the ΔV_{th} recovery for the short stress times (e.g. 1µs in Fig. 7), due to slower recovery at T=25°C than T=175°C. These temperature dependencies can be also explained with Arrhenius temperature acceleration activation energies for charge capture and charge emission are below 100meV.

In earlier publications [14, 19], we have also shown measurements with V_g=-10V, where the negative ΔV_{th} is doubled compared V_g=-5V and saturation occurs already after 10µs. Comparing the results, we observe that the density of traps also shows a strong voltage dependence. Modeling this negative stress voltage dependence is work in progress.

In addition to the stress voltage dependence of the capture time constants, there is also a dependence of the emission time constants on the recovery voltage. In particular, it is necessary to study the time-constants of the recovery with recovery voltage for negative as well as positive stress to provide a model for the bipolar AC stress with variable voltage levels.

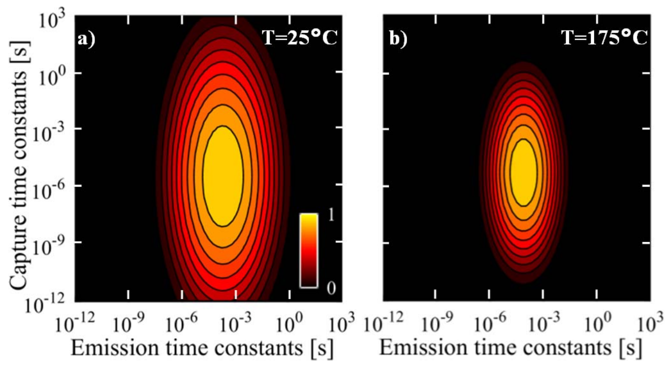

Fig. 8: NBTI capture and emission time map (V_g=-5V/ V_{th}) at a) T=25°C and b) T=175°C obtained by fits according to equ. (1) to MSM measurements as shown in Fig. 7. with recovery traces for stress-times from 100ns up to 100ks. The charged trap density g is shown in dependence of the capture and emission activation energies and is normalized to 1 using $\log_{10}(1+\kappa\cdot \max(g))/\log_{10}(1+\kappa)$ with $\kappa = 100$ to emphasize all details [20]. Max(g)= $23.7V/eV^2$, which corresponds for T=175°C to $\max(g) = 1.5V/\mathrm{decade}^2$. Activation energies for charge capture and charge emission are below 100meV.

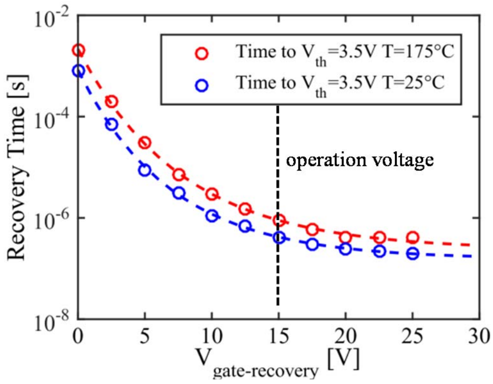

Fig. 9: Recovery from negative stress (V_g=-10V, t_s=10ms) at T=25°C and T=175°C. Shown is the required time at V_{gs} to recover V_{th} back to a value of 3.5V. The required time decreases exponentially with increasing recovery voltage (dashed lines), the charge emission at operation voltage occurs within 100ns after switching to a positive V_g.

However, the NBTI and the PBTI CET maps are obtained with $V_{rec} = V_{th}$ and are thus not directly applicable. For the calculation of the occupation probability map when switching from negative to positive gate voltage, the accelerated recovery of the negative ΔV_{th} with increased recovery voltage has to be considered.

Conversely, when switching from positive to negative gate voltage, the accelerated recovery of the positive ΔV_{th} with increased recovery voltage has to be considered. In Fig. 9, we show the recovery time of V_{th} after negative stress back to the initial V_{th} as a function of the recovery voltage. Most of the negative ΔV_{th} disappears within ~100ns after switching V_{gate} back to positive bias (see Fig. 9). The recovery time depends exponentially on the gate voltage during recovery. In these first 100ns the negative ΔV_{th} actually helps to switch the MOSFET faster into the ON-state than without this ΔV_{th}.

In Fig. 10 (equivalent to Fig. 9), we show the dependence of the recovery voltage on the time it takes V_{th} to recover back to its initial value after positive stress for two exemplary stress times for T=25°C and T=175°C. Applying e.g. -5V after positive stress accelerates the recovery back to the initial V_{th} by more than 8 orders of magnitude in time compared to applying 5V during recovery (dependent on the temperature and positive bias stress time).

These properties have to be considered when performing simulations with the CET maps by correcting the occupation probability map by the corresponding de- or accelerated recovery times.

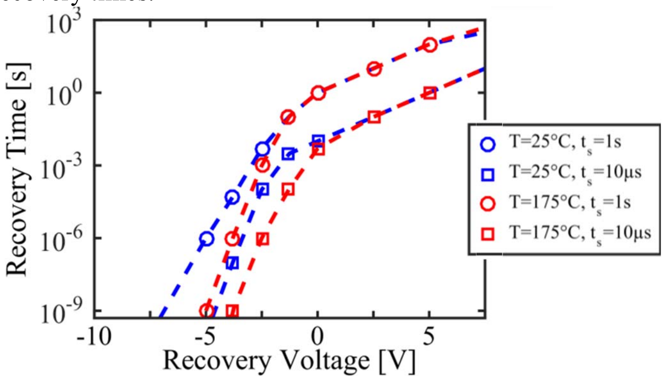

Fig. 10: Recovery from positive stress (V_g=25V, t_{stress}=10µs (rectangles) and t_{stress}=1s (circles)) at T=25°C and T=175°C. Shown is the required time at $V_{g,rec}$ to recover V_{th} back to its initial value. The required time decreases drastically with decreasing recovery voltage (dashed lines).

VI. AC Measurement Results

In the next step, we study the threshold voltage hysteresis introduced by an application-like bipolar AC gate signal with a frequency of 50kHz for different V_{high} and V_{low} combinations (see Fig. 12 a-d). 50kHz is a common frequency for applications of SiC MOSFETs. The goal of these measurements is to measure the hysteresis and compare the results to our CET map simulation approach. We will demonstrate in Chapter VII that combining the PBTI CET map (Fig. 3) and the NBTI CET map (Fig. 8), we are able to model the V_{th} hysteresis, which can be used as add-on in circuit simulators.

To measure the behavior of V_{th} in real-time during the AC stress, we interrupt the AC stress at different positions in time during the AC signal (see Fig. 11b).

The full V_{th} recovery (1µs up to 10ms) back to the initial V_{th} can be seen in Fig. 11c) for each interruption of the AC gate signal. The measurement – keeping V_g at V_{th} for 10ms – disrupts the trap occupation state caused by the bipolar AC signal. To fully restore the pre-measurement trap occupation state before each interruption of the AC gate signal 100ms of AC stress is applied (see Fig. 11a). This is long enough to fully restore the trap-occupation state and short enough that only the traps with short capture and emission times are activated. Applying another AC stress of 100ms does therefore not increase the long-term V_{th}, because no slowly recovering components are activated.

The most relevant part of these measurements is the hysteresis at the shortest possible measurement delay of 1µs, so in Fig. 11d), the first measurement points of a V_{th} recovery trace are shown with respect to their timing position during the AC signal. In Fig. 12a) and b), the measured V_{th} at T=175°C during a 50kHz AC signal is shown for two different V_{high} (5V and 20V) with ten V_{low} combinations ranging from 0 to -10V. Short-term hysteresis of the threshold voltage of up to 4V is observed (see Fig. 12b) for V_{low}=-10V and V_{high}=20V. The fast decrease in V_{th} during negative gate stress is caused by the previously described capture of holes with capture times below 1µs dependent on the negative gate voltage [14].

For Si MOSFETs the short-term threshold hysteresis during AC stress amounts only to a few mV, due to a very small portion of traps with short capture and emission time constants. The capture times of SiC for hole capture are a lot faster than for electron capture, which is visible in the fast saturation during the V_{low} signal (compare to electron capture in Fig. 2). Furthermore, the saturation under V_{low} bias is accelerated with decreasing V_{low} and almost independent of V_{high}. On the other hand the increase in V_{th} during the V_{high} signal is both due to the acceleration of the negative ΔV_{th} recovery with increasing V_{gate} and also due to the capture of electrons during positive gate bias stress (see Fig. 9).

We performed measurements for the different V_{high} and V_{low} combinations also at T=25°C with the same qualitative observations as for the measurements at T=175°C (see Fig. 12c) and d). The initial V_{th} at T=25°C is higher due to the intrinsic temperature dependence of the threshold voltage.

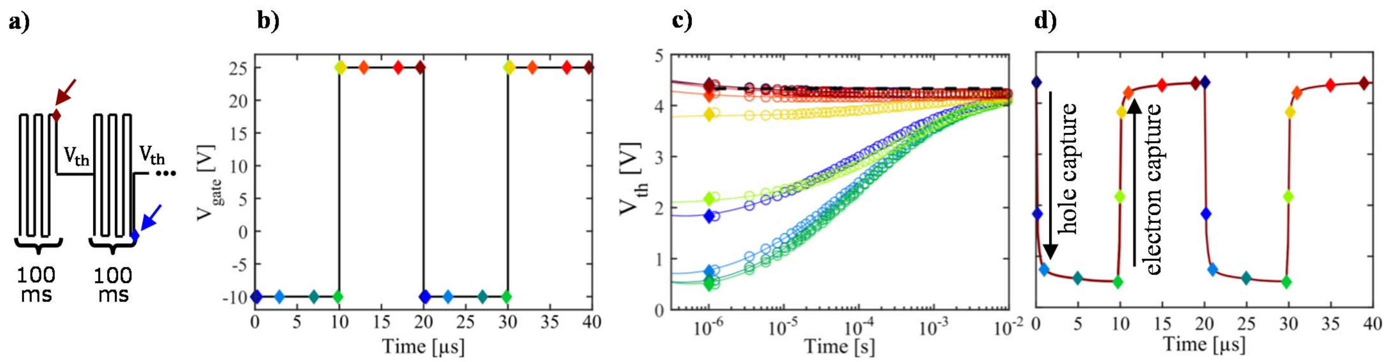

Fig. 11: Explanation of the measurement technique, example with real data (T=175°C, V_{high}=25V, V_{low}=-10V, f=50kHz): **a)** The AC stress is interrupted at different points in time of the rectangular signal. Directly after end of stress, the threshold voltage is measured from 1µs to 10ms recovery time. Between each measurement point another AC stress of 100ms is applied in order to restore the pre-measurement trap occupation state. **b)** An example 50kHz bipolar AC signal is shown with different points of interruption as described for a). In **c)** The V_{th} measurement after each interruption of the AC signal is shown on a logarithmic time scale. **d)** The first measurement point (after 1µs measurement delay) is shown with the corresponding timing position during the AC signal. Line serves as guide to the eye. The threshold voltage hysteresis is mostly due to capture and emission (neutralization) of positive charges.

An analysis of all minimum and maximum values of V_{th} during the bipolar AC stress of the different V_{high} and V_{low} combinations can be found in [19]. For the V_{high} phase, the most interesting parameter is the time it takes to reach the maximum value V_{th} during AC stress. With increasing V_{high} the time until saturation decreases. Comparing Fig. 12a) and Fig. 12c), we observe a longer time needed to recover after the negative voltage phase for T=25°C, which is due to the broader distribution of the emission time constants at lower temperatures (see Fig. 8). Based on this result, the impact of the hysteresis on circuit operation is studied and modeled in Chapter VII.

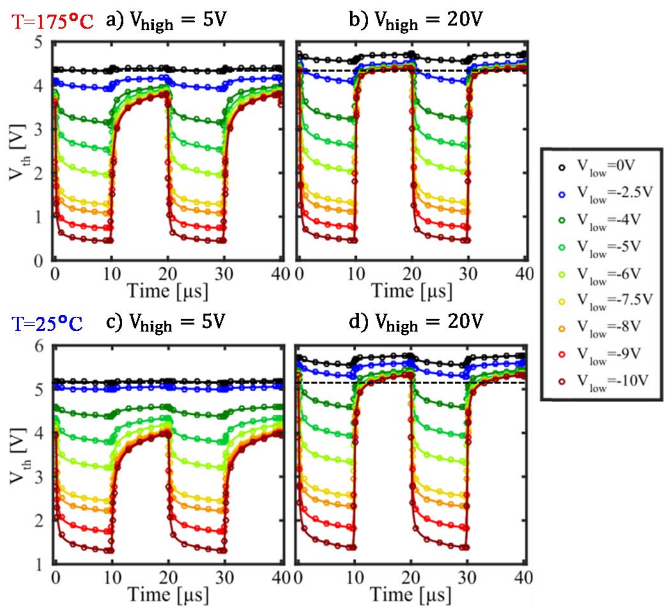

Fig. 12: Threshold voltage hysteresis at a bipolar AC signal with frequency of 50kHz. The measured V_{th} dependence on the AC signal with varied V_{low} is shown for T=175°C with a) V_{high}=5V and b) V_{high}=20V as well as for T=25°C in c) and d). The initial V_{th} is marked as dashed line. Lines serve as guide to the eye.

VII. Simulating Short and Long Term AC Stress

We have shown in Chapters IV and V that ΔV_{th} under positive and negative gate bias stress contains large fast recovering components. Furthermore, we have demonstrated that we can model the DC ΔV_{th} using PBTI and NBTI CET maps. The concept of CET maps is especially beneficial for the simulation of short- as well as long-term AC signals. To obtain the V_{th} response to a rectangular AC signal, the occupancy of the CET map has to be evaluated. For a rectangular signal a derivation of the occupancy level of the defects after AC stress can be found in [31]. First, we will explain and discuss the short-term bipolar AC simulation results and compare them to the measurements shown in Fig. 12. In the second part we will present the results from long-term AC measurements and simulations.

For a comparison of the hysteresis simulation results we chose V_{low}=-5V and V_{high}=25V and show the measured and simulated ΔV_{th} at T=25°C and T=175°C in Fig. 13. The measured hysteresis inherits two temperature dependencies: As already seen in Fig. 1, the negative ΔV_{th} after 10µs stress is higher for T=175°C than for T=25°C, whereas as seen in Fig. 2, the ΔV_{th} after 10µs positive stress is higher for the lower temperature. Combining both effects, the absolute hysteresis is larger for T=175°C than for T=25°C. Due to the bipolar AC stress, the simulation results are obtained by the superposition of the negative and positive ΔV_{th} calculated using the corresponding PBTI and NBTI CET maps.

The negative ΔV_{th} during the V_{low} signal and its recovery during the V_{high} signal phase can be simulated with the NBTI CET map shown in Fig. 8 a) for T=25°C and b) for T=175°C. In addition, the accelerated recovery of the negative ΔV_{th} with increased recovery voltage has to be considered when switching from negative to positive gate voltage (see Fig. 9).

The positive ΔV_{th} during the V_{high} signal and its recovery during the V_{low} gate signal can be modeled with the PBTI CET map shown in Fig. 4. As seen in Fig. 10, the recovery of the positive ΔV_{th} is highly accelerated with decreased recovery voltage of -5V (compared to V_{th} in Fig. 2), so the contribution of the positive ΔV_{th} to the V_{th} hysteresis during the V_{low} signal phase can be neglected. The simulated hysteresis, shown in Fig. 13, with the superposition of the contribution of both the positive and negative ΔV_{th} shows an excellent agreement with

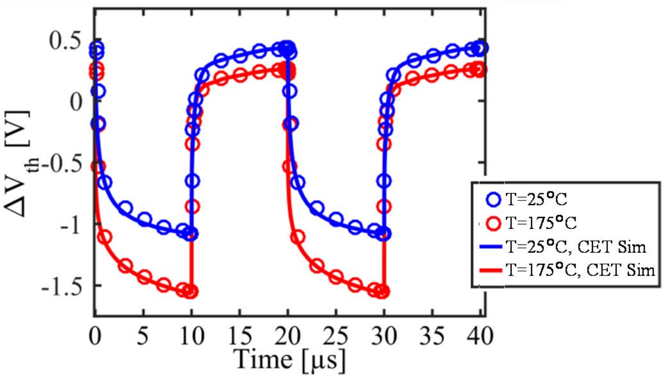

Fig. 13: ΔV_{th} hysteresis at a bipolar AC signal with V_{low}=-5V, V_{high}=25V T=25°C (blue) and T=175°C (red) with f=50kHz. Symbols are experimental data recorded with a measurement delay of 1µs. The solid lines show the calculated results for each temperature obtained by the combination of the NBTI and PBTI CET maps shown in Fig. 3 and Fig. 8.

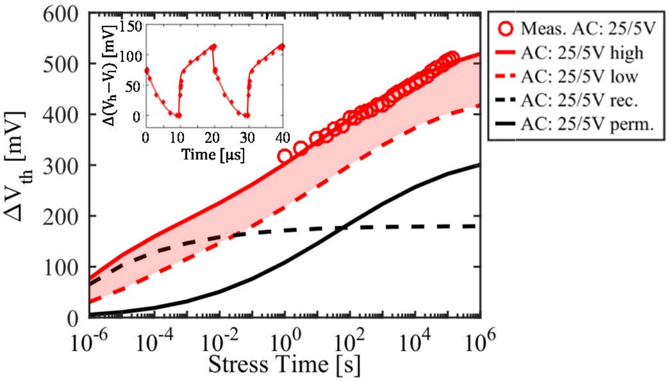

Fig. 15: Simulation and measurements of ΔV_{th} after 25/5V AC gate stress at T=175°C and a measurement delay of 1µs. The AC measurements were performed at a frequency of 50kHz and a duty cycle of 50% (red circles). The lines correspond to the simulation obtained from the CET map shown in Fig. 3. The solid red line corresponds to the simulated ΔV_{th} of the CET map in Fig. 3 with interruption of the AC stress after the high pulse whereas the dashed red line corresponds to the simulation after the end of the low pulse. The black lines correspond to the contribution of the recoverable (dashed black line) and the permanent component (solid black line). In the inset the threshold voltage hysteresis within the high and low pulse is shown.

the measurement results. With the knowledge of all temperature and voltage dependencies of both the NBTI and PBTI CET maps, we provide a very good and accurate approach for the consideration of the hysteresis in circuit simulators.

Another important application of the CET maps is the calculation of the ΔV_{th} after long-term AC stress. In Fig. 14 we compare the measurements of ΔV_{th} after DC stress at two different temperatures (25°C and 175°C) to the ΔV_{th} after AC stress with V_{high}/ V_{low} 25V/5V as well as the 25V/0V at T=175°C at a frequency of 50kHz.

The ΔV_{th} after AC stress is measured directly at the end of the high voltage period with a measurement delay of 1µs. We observe that ΔV_{th} after AC conditions 25V/5V as well as AC 25V/0V have the same power-law exponent as the DC stress (see Fig. 14 on the right). Simulation results are obtained by the PBTI CET maps shown in Fig. 4. The AC simulations can be directly obtained by the multiplication of the PBTI CET map at T=175°C with the defect occupancy map for the corresponding AC stress pattern. For V_{low}=0V, additionally the recovery acceleration with decreasing recovery voltage has to be considered (see Fig. 10).The acceleration of the relaxation during the AC stress V_{low} period leads to a lower degradation after AC 25/0V AC stress than at 25/5V. We achieve a very good agreement of all PBTI CET map simulations (shown as lines in Fig. 14) and the measurement data of the AC stress, which is mainly limited by sample to sample variation.

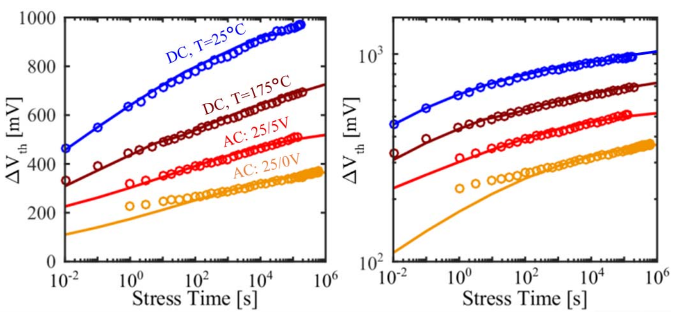

Fig. 14: Simulation (lines) from PBTI CET map (shown in Fig. 4) and measurements of ΔV_{th} after 25V DC T=25°C and DC T=175°C, 25/5V AC and 25/0V AC gate stress at T=175°C (linear scale on the left, log scale on the right). Measurement delay is 1µs. The AC measurements were performed at a frequency of 50kHz and a duty cycle of 50% equivalent to alternating $t_s = 10\mu s$ and $t_{rec} = 10\mu s$. The solid lines are simulations obtained from the PBTI CET map. To simulate the 25V/0V AC signal the stress time $t_s = 10\mu s$ and the equivalent recovery time $t_{rec,0V} = 3 \cdot t_{rec,V_{th}}$. Simulation and measurements show a very good agreement.

To understand the impact of each component of the PBTI CET map, we show in Fig. 15 the evolution of the recoverable and more permanent component of ΔV_{th} within the 25/5V AC stress (same data as red circles in Fig. 14, T=175°C, f=50kHz). The black solid line shows the contribution of the more permanent defects of the PBTI CET map (see Fig. 4), whereas the black dashed line corresponds to the contribution of the recoverable defects. Already after 1ms AC stress, the contribution of the recoverable defects does not increase any more – these defects contribute to the short-term hysteresis also shown in the inset in Fig. 15. The dashed red lines correspond to the simulated ΔV_{th} at the end of the low voltage period. Furthermore, the highlighted red area marks the constant charging and discharging of the defects, which is the short-term hysteresis, within the long-term AC stress. In contrast, the contribution of the more permanent defects, as expected, increases with AC stress time. The hysteresis does not increase for the long-term AC stress which has been verified with hysteresis measurements before and after the AC stress. To conclude, we have demonstrated that the concept of analytic CET maps can be used to predict the temperature and voltage dependence of DC SiC positive gate bias stress with a very high accuracy. Moreover the analytic CET map is also a valuable method to simulate different short as well as long-term AC gate stress signals.

VIII. IMPACT ON CIRCUIT OPERATION AND VERIFICATION

For Si, the V_{th} hysteresis during a bipolar AC signal amounts to only a few mV and is uncritical. For SiC, the short-term threshold voltage hysteresis mainly due to negative gate bias has been already observed the measurement of IV-curves in a shift of the subthreshold voltage [4]. Fortunately, this effect is not permanent and recovers quickly within a fraction of the positive gate bias pulse. Also, the threshold voltage hysteresis itself does not increase after end of life.

In real applications in contrast to the measurement the portion of ΔV_{th} which is recovered within the measurement delay is still active during the application [14]. The amount can be estimated from CET maps, but the estimation is based only on extrapolations and not on experimental data. Therefore, we also perform recovery-free on-the-fly measurements to study the impact of ΔV_{th} on R_{on} during application conditions.

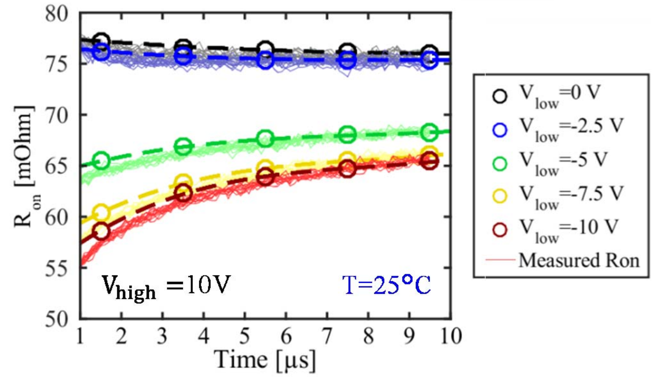

Fig. 16: R_{on} during the V_{high} period of the AC stress for different values of V_{low} with V_{high}=10V with Id=100mA at T=25°C. Thin lines: Directly measured R_{on} for 50 successive periods. Circles: R_{on} calculated from measured static I_d-V_g curves and the ΔV_{th} from Fig. 12. The dashed lines are a guide to the eye connecting the circles. The change in R_{on} is therefore fully recoverable during AC stress.

In Fig. 16 we present the measured R_{on} during the V_{high} period (transistor is "on") of the AC stress for different V_{low} voltages. For the comparison of R_{on} with ΔV_{th} we use a temperature of T=25°C, because the impact of ΔV_{th} on R_{on} at high temperatures decreases due to the temperature dependence of R_{on} and the decreasing transconductance. Furthermore, we chose V_{high}=10V because at higher gate voltages (i.e. 15V) ΔV_{th} recovers too fast to cause a clearly measurable change in R_{on} (see Fig. 9). Fig. 16 shows that the dependence of R_{on} during AC stress is only correlated to the observed ΔV_{th} during AC stress and shows the same dependencies as ΔV_{th} in Fig. 12. As a matter of fact, R_{on} is actually lower after negative gate stress which helps to minimize static losses. The measured ΔV_{th} during AC stress at T=25°C and V_{high}=10V is used to calculate the change in R_{on} using the static I_d-V_g curve in the linear regime (R_{on} dependent on the gate voltage) as reference. The observed ΔV_{th} can be directly mapped to R_{on} (see circles in Fig. 16) with a perfect agreement. The R_{on} increases back to its initial value with recovering V_{th}. An even lower R_{on} in Fig. 16 is expected for t ≤ 1µs (not shown in Fig. 16 due to finite settling time of measuring amplifier). Note that ΔV_{th} is the only reason for ΔR_{on} and can completely explain the changes in magnitude. Possible changes in the mobility apparently do not play a role. This has three highly positive conclusions: First, we can perfectly explain and model the change in R_{on} during AC stress. Second the change in R_{on} is also fully recoverable as V_{th} and third, R_{on} is lowered during the negative (V_{low}) period of the AC stress and therefore helps to switch the SiC-MOSFET faster, thus minimizing dynamic losses.

IX. Conclusions

Utilizing a fast measurement technique, that is, short stress pulses (100ns) and continuously measured recovery from µs to 100ks, we are able to determine the time constants for capture and emission of positive and negative charges as a function of the applied bias. We developed a simulation approach for modeling of ΔV_{th} under positive as well as negative gate bias stress using capture and emission time maps. We have shown that both the positive and negative gate bias stress contain large quickly recovering components, which remain undetected during JEDEC-like tests as being defined for silicon devices [30]. Due to the temperature dependence, also of the fast recovery after positive gate bias stress, we observed a higher ΔV_{th} for low temperatures than for higher temperatures. Therefore, we propose to cool down the sample with bias applied prior to measuring the recovery.

An alternative to the standard JEDEC test is to use a preconditioning approach [12], which eliminates the contribution of the fast recovering part of the negative as well as the positive ΔV_{th}. With this approach the lifetime parameter dependence on the measurement delay is drastically reduced, but information about recovering components in the sub millisecond regime is lost. To completely investigate the impact of the fast recovering components, we propose utilizing gate bias stress occurring in the application (negative DC and AC only) and a shortest possible measurement delay (e.g. 1µs).

We have also presented a method using a bipolar AC gate bias stress, which is application-relevant and can simulate any AC/DC stress sequence or history, exactly like in the application. Our measurements show that applying a bipolar AC gate bias stress causes large and very fast fully recoverable threshold hysteresis as seen before in [4] with magnitudes up to 4V.

Combining the NBTI and PBTI CET maps obtained by the DC stress measurements, we can perfectly explain and model this behavior. During the negative gate phase ΔV_{th} is due to capture of positive charges in the oxide and at the interface. During the positive gate phase the positive charges are neutralized and negative charges are captured. Our model additionally includes the recovery voltage dependence of the positive and negative charge emission. With this modeling approach we are able to model the threshold voltage hysteresis during normal operation and provide it as an add-on to a standard SPICE model for circuit simulations.

Furthermore, we have demonstrated that the AC long-term measurements can be simulated with good accuracy by the analytic CET maps enabling lifetime modeling after an arbitrary stress signal. Results and predictions of the analytic CET maps are considering the measurement delay and thus eliminating the influence of the measurement delay on the ΔV_{th} prediction.

We have also shown that the change in R_{on} is only due to the ΔV_{th} change during AC stress which is fully recoverable just like the ΔV_{th}. It is also demonstrated that the change in R_{on} due to the hysteresis has no harmful effect when the MOSFET works in a switch-mode converter, because R_{on} is actually lowered during the negative period of the AC stress and therefore helps to switch the SiC-MOSFET faster while minimizing static losses and temperature increase of the device.

X. References

[1] T. Kimoto, "Material science and device physics in SiC technology for high-voltage power devices," *Japanese Journal of Applied Physics*, vol. 54, no. 4, p. 40103, 2015.

[2] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Applied Physics Reviews*, vol. 2, no. 2, p. 21307, 2015.

[3] R. Rupp, "CoolSiC™ and major trends in SiC power device development," in *Solid-State Device Research Conference (ESSDERC), 2017 47th European*, 2017, pp. 118–121.

[4] CREE, "CPWR-AN08 Application Considerations for SiC MOSFETs," http://studylib.net/doc/18170945/cree-cpwr-an08-application-considerations-for-sic-mosfets.

[5] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 316–323, 2015.

[6] T. Okunishi *et al.,* "Reliability study on positive bias temperature instability in SiC MOSFETs by fast drain current measurement," *Japanese Journal of Applied Physics*, vol. 56, no. 4S, 04CR01, 2017.

[7] G. Rescher, G. Pobegen, and T. Grasser, "Threshold voltage instabilities of present SiC-power MOSFETs under positive bias temperature stress," in *Materials Science Forum*, 2016, pp. 481–484.

[8] R. Green, A. Lelis, and D. Habersat, "Threshold-voltage bias-temperature instability in commercially-available SiC MOSFETs," *Japanese Journal of Applied Physics*, vol. 55, no. 4S, 04EA03, 2016.

[9] D. B. Habersat, R. Green, and A. J. Lelis, "Evaluations of threshold voltage stability on COTS SiC DMOSFETs using fast measurements," in *Reliability Physics Symposium (IRPS), 2016 IEEE International*, 2016, CD‐4.

[10] G. Rescher, G. Pobegen, T. Aichinger, and T. Grasser, "On the subthreshold drain current sweep hysteresis of 4H-SiC nMOSFETs," in *Electron Devices Meeting (IEDM), 2016 IEEE International*, 2016, pp. 10–18.

[11] D. B. Habersat, R. Green, and A. J. Lelis, "Temperature-dependent threshold stability of COTS SiC MOSFETs during gate switching," in *Reliability Physics Symposium (IRPS), 2017 IEEE International*, 2017, WB‐4.

[12] G. Rescher, T. Aichinger, G. Pobegen, "Comprehensive Evaluation of Bias Temperature Instabilities on 4H-SiC MOSFETs Using Device Preconditioning: (to be published)," *ICSCRM*, 2017.

[13] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability*, vol. 80, pp. 68–78, 2018.

[14] Puschkarsky K., Reisinger H., Aichinger, T., Gustin W., Grasser T., "Understanding BTI in SiC MOSFETs and its impact on circuit operation," *Transactions on Device Microelectronics Reliability*, 2018.

[15] J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: A review," (en), *Microelectronics Reliability*, vol. 46, no. 2–4, pp. 270–286, 2006.

[16] T. Grasser *et al.,* "Recent advances in understanding the bias temperature instability," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, p. 4.

[17] H. Reisinger *et al.,* "Analysis of NBTI degradation-and recovery-behavior based on ultra fast VT-measurements," in *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International*, 2006, pp. 448–453.

[18] M. Denais *et al.,* "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 109–112.

[19] Puschkarsky K., Reisinger H., Aichinger, T., Gustin W., Grasser T., "Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation," in *Integrated Reliability Workshop Final Report, 2017 IEEE International*, Lake Tahoe, 2017.

[20] T. Grasser *et al.,* "Analytic modeling of the bias temperature instability using capture/emission time maps," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, 27‐4.

[21] Y. Illarionov *et al.,* "Hot-Carrier Degradation and Bias-Temperature Instability in Single-Layer Graphene Field-Effect Transistors: Similarities and Differences," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3876–3881, 2015.

[22] G. Pobegen, T. Aichinger, M. Nelhiebel, and T. Grasser, "Understanding temperature acceleration for NBTI," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, 27‐3.

[23] T. Grasser *et al.,* "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," in *Integrated Reliability Physics Symposium (IRPS), 2010 IEEE International*, 2010, pp. 16–25.

[24] C. Schlünder, W. Heinrigs, W. Gustin, and H. Reisinger, "On the impact of the NBTI recovery phenomenon on lifetime prediction of modern p-MOSFETs," in *Integrated Reliability Workshop Final Report, 2006 IEEE International*, 2006, pp. 1–4.

[25] G. Pobegen and T. Grasser, "On the distribution of NBTI time constants on a long, temperature-accelerated time scale," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2148–2155, 2013.

[26] T. Aichinger, M. Nelhiebel, and T. Grasser, "On the temperature dependence of NBTI recovery," *Microelectronics Reliability*, vol. 48, no. 8, pp. 1178–1184, 2008.

[27] H. Reisinger, T. Grasser, W. Gustin, and C. Schlünder, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC-and AC-stress," in *Reliability Physics Symposium (IRPS), 2010 IEEE International*, 2010, pp. 7–15.

[28] G. Rzepa *et al.,* "Complete extraction of defect bands responsible for instabilities in n and pFinFETs," in *VLSI Technology, 2016 IEEE Symposium on*, 2016, pp. 1–2.

[29] T. Grasser *et al.,* "Analytic modeling of the bias temperature instability using capture/emission time maps," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, 27‐4.

[30] *JEDEC Standard: Temperature, bias, and operating life*: JESD22-A108D.

[31] H. Reisinger *et al.,* "Understanding and modeling AC BTI," in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, 2011, 6A‐1.