Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation

Katja Puschkarsky[1,3], Hans Reisinger[1], Thomas Aichinger[2], Wolfgang Gustin[1] and Tibor Grasser[3]

1) Infineon Technologies AG, D-85579 Munich, Germany
2) Infineon Austria AG, AT-9550 Villach, Austria
3) Vienna University of Technology, AT-1030 Vienna, Austria

***Abstract*— Threshold voltage hysteresis in SiC power MOSFETs is rarely studied. This work investigates the capture- and emission-time constants of positive and negative charge trapped in the gate oxide and interface as a function of gate bias. We present a measurement technique which enables measurement of the real V_{th} during application-relevant bipolar AC gate stress. We show that threshold voltage hysteresis has no harmful effect on switching operation.**

I. Introduction

Due to the higher breakdown field in SiC compared to Si, high voltage power MOSFETs made of SiC have shorter drift zones than those made of Si with the same on-resistance R_{on} and voltage class, and thus have 100 times lower gate-source and gate-drain capacitances [1, 2]. Thus the losses caused by gate driving are reduced. On the other hand, short-term as well as long term ΔV_{th} in SiC-MOSFETs under positive and negative gate bias stress are significantly higher but recovering faster than the ones observed in Si-MOSFETs [3–5]. This is observed in commercially available SiC-MOSFETs from various manufacturers. There are major differences to the well-known threshold drifts in Si-MOSFETs, especially the well-investigated NBTI-effect in pMOSFETs. ΔV_{th} in SiC-MOSFETs is fast recovering and goes in both directions from typically +1V to -3V, due to capture of both negative and positive charges in the gate oxide and interface [6]. In this paper, we will compare parameters extracted from positive and negative DC-stress tests as a function of measurement delay. Our measurement technique provides direct readouts of V_{th} with 1µs resolution. This high resolution enables us for the first time to determine capture and emission time constants of positive and negative charge as a function of the applied gate bias and temperature. We measure how the threshold voltage varies at a typical 50kHz bipolar AC gate signal. The main purpose of this paper is to show the necessity to improve the JEDEC tests for SiC and to discuss the impact of the threshold hysteresis on the switching behavior.

II. Measurement Setup

The samples used in this study were packaged SiC trench MOSFETs with a maximum V_{ds} of 1200V and a maximum V_{gs} of +20/-10V. ΔV_{th} after DC gate bias stress as well as during bipolar AC-stress were measured using our ultra-fast measurement technique [7] with a measurement delay, that is the time between interruption of stress and the settling time of the Vth-readout, of 1µs. The resolution in the stress-timing as well as the width of the shortest rectangular stress pulses we can apply is 100ns. The resulting accuracy in the stress timing (also for the AC signals) is about ± 20ns. These limits are mainly determined by the high gate capacitance of ≈2nF, the length of the test leads of several cm, together with an imperfect impedance matching. Thus our accuracy in determining the time constants of V_{th}-transients under positive or negative gate stress due to capturing or emitting charge also is about ±20ns. As seen, for example in Fig. 6 c), there is only a moderate and pretty smooth change in V_{th} (for V_g=V_{th}) between recovery-times of 100ns to 10µs. An improved measurement delay e.g. of 100ns would only moderately change our results. Before each stress measurement, the initial V_{th} is recorded and the measurement sequence applied is a Measure-Stress-Measure (MSM) sequence. All measurements are performed with a well-defined stress history e.g. 50kHz AC stress for a given number of periods and ending at exactly 20% of a period and without voltage ramps to measure IV curves (see Fig. 6). Therefore comparability is secured and the measurements are perfectly reproducible. Our ultra-fast measurement technique enables measurement of the real V_{th} during application-relevant bipolar AC stress signals. In order to reveal the impact of the short-term threshold excursions on the switching behavior, time resolved R_{on} measurements during AC stress were performed. Stress and measurement temperatures ranged from 25°C to 175°C.

III. DC Measurement Results

We compare the ΔV_{th} of SiC-MOSFETs after positive gate bias stress with the ΔV_{th} of Si-MOSFETs with the same gate oxide thickness t_{ox} and same E_{ox}(see Fig. 1). Si-MOSFETs show generally a lower ΔV_{th} due to a lower defect density compared to SiC. SiC-MOSFETs show a higher, but fast recovering ΔV_{th} with a peculiarity that is only visible at short measurement delays: The ΔV_{th} at lower temperatures is higher than at high temperatures. We will demonstrate in section III that it is easy to explain this phenomenon using so-called capture and emission time (CET) maps. For Si, it is already well established that threshold voltage shifts due to BTI can be understood as the collective response of an ensemble of independent defects, in addition the CET maps contain information about the kinetics of charge capture and emission [8]. A higher ΔV_{th} at lower temperatures has not been observed for Si, because the defect density in the CET map

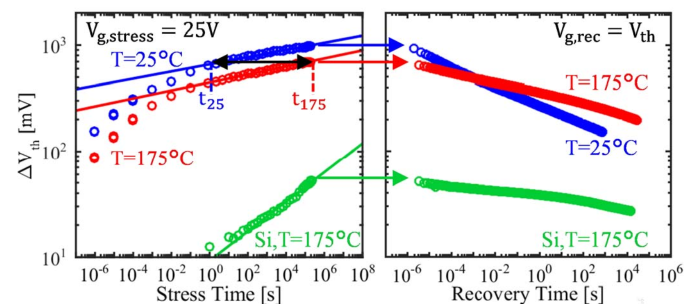

Fig. 1: **Left:** Comparison of SiC and Si-MOSFETs with same t_{ox} and same E_{ox} during positive gate bias stress with 1µs measurement delay. SiC shows higher but fast recovering ΔV_{th} with a reversed temperature dependence compared to Si: ΔV_{th} at lower temperatures (T=25°C) is larger than at higher temperatures (T=175°C). **Right:** Recovery after 200ks stress with the same stress voltage. Recovery at lower temperatures is faster than at higher temperatures. A crossing of the measured ΔV_{th} is observed at 5ms.

978-1-5386-2332-9/17/$31.00 ©2017 IEEE

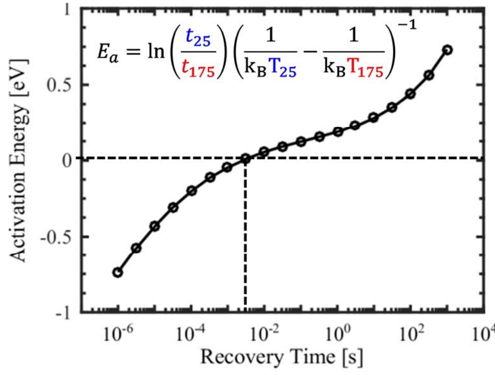

Fig. 2: Extracted apparent activation energy for the capture time constants as a function of the recovery times calculated with t_{25} and t_{175} (see Fig. 1). Due to the different recovery slopes, the extracted apparent activation energy depends strongly on the measurement delay

increases from short to long capture time constants τ_c [9, 10]. We observe for SiC that many trap centers have very short capture and emission time constants, also below 1µs. The fast increase of ΔV_{th} after short stress times (see Fig. 1a) manifests this observation. Since the trap centers with short capture time constants (τ_c<1ms) have also short emission time constants (τ_e<1ms), the increase of V_{th} vanishes quickly as it appears within milliseconds (see Fig. 1, right). For Si, the temperature activation of a single trap is modeled according to the Arrhenius equation as a decrease of the capture and emission time constants [11]:

$$t_2 = \tau_o \cdot \left(\frac{t_1}{\tau_0}\right)^{\frac{T_1}{T_2}} \qquad (1)$$

with t_1 the capture/emission time constant at temperature T_1, t_2 the transformed capture/emission time constant at temperature T_2 and τ_0 the time transformation constant. Due to this dependency, capture time constants of trap centers around 1µs at T=25°C decrease with increasing temperature and become shorter than the measurement delay. Therefore the measured ΔV_{th} at T=25°C is higher than at T=175°C for short recovery times. The amount of ΔV_{th} caused by defects with very short capture and emission time constants is directly visible in the difference between T=25°C and T=175°C. As seen in Fig. 1 on the right, the recovery at lower temperatures occurs faster than at higher temperatures. After 5ms recovery time, a crossing of the measured ΔV_{th} is observed. Measurements with standard measurement equipment and a measurement delay greater 10ms cannot resolve this temperature dependence and miss the change of ΔV_{th} caused by fast charging and de-charging trap centers. The different measurement delays lead to a large unphysical dependence of the extracted activation energy of the capture time constants on the measurement delay (see Fig. 2). In particular for measurement delays shorter than 5ms, negative activation energy is extracted. This dependency has to be considered for lifetime extrapolation [10]. Nonetheless, also for SiC there are many trap centers with capture and emission constants >100ks. For long stress times, the effective activation energy is positive, so the worst case for positive gate bias stress is still at high temperatures.

The comparison of ΔV_{th} at two different voltages shows a powerlaw dependence with stress time (see Fig. 3 on the left) for two different measurement delays (1µs circles, 100ms triangles). Already after 100ms, half of the ΔV_{th} has vanished (see Fig. 3 on the right). As observed for Si, with increasing

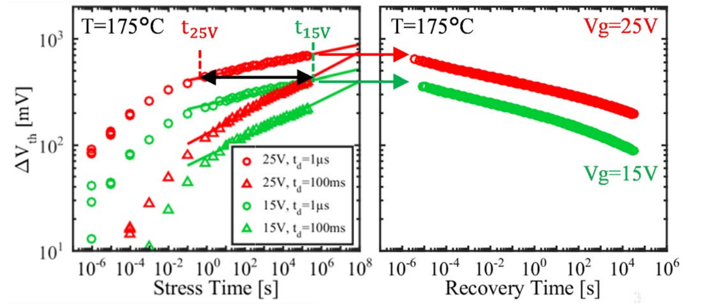

Fig. 3: **Left:** Comparison of the ΔV_{th} with stress time at two different voltages with two different measurement delays (1µs and 100ms at T=175°C). The data is fitted with a powerlaw with same exponent for both voltages. **Right:** Comparison of the recovery after 200ks stress time. Within a few ms a huge amount of the ΔV_{th} recovers following a power law.

stress voltage ΔV_{th} increases, but the recovery after BTI for Si devices is approximately linear with the logarithm of recovery time which is due to the broader distribution of the emission time constants. For SiC the recovery is linear on a log-log scale (see Fig. 3, on the right), due to many trap centers with short emission times. We conclude that with a higher stress voltage more trap centers are activated, but the distribution of the capture and emission time constants remains unchanged when increasing the stress voltage. A similar observation was made in [8] for Si, where the strong bias dependence of the individual traps did not directly translate into the distribution of time constants. The reason for this is that with different gate bias also the active energy region in the oxide changes. The voltage acceleration factor (see Fig. 4) is commonly used to calculate the decrease of stress time compared to use conditions. The voltage acceleration factor of in Fig. 4 is the longest stress time of the 15V measurement (t_{15V}, green dashed line in Fig. 3, left) divided by the stress time needed to reach the same ΔV_{th} at 25V (t_{25V}, red dashed line in Fig. 3, left). Due to the fast recovery after stress, the measurement delay also has a dramatic effect on the voltage acceleration factor. Dependent on the measurement delay, the voltage acceleration factor differs by orders of magnitudes.

The parameters required for lifetime predictions e.g. stress time dependence, measured apparent activation energies and voltage acceleration factor depend strongly on the measurement delay. Lifetime estimation according to the JEDEC [12] procedure allows a measurement delay of 48 hours which is clearly inappropriate for SiC. Furthermore, SiC-MOSFETs in switch mode converters are operated in AC mode or negative DC mode, but positive long-term DC stress is never applied.

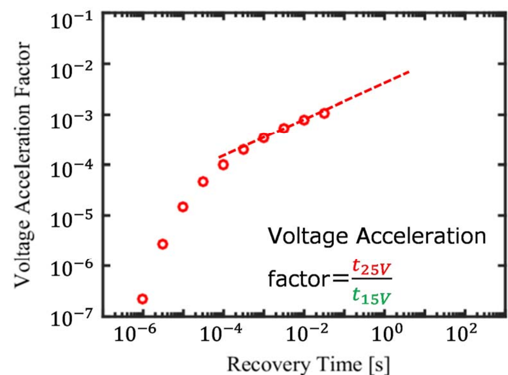

Fig. 4: The voltage acceleration factor taken at t_{stress}=100ks as a function of recovery time. The non-linear recovery leads to different voltage acceleration factors depending on the measurement delay, which hampers the extraction of lifetime models for SiC.

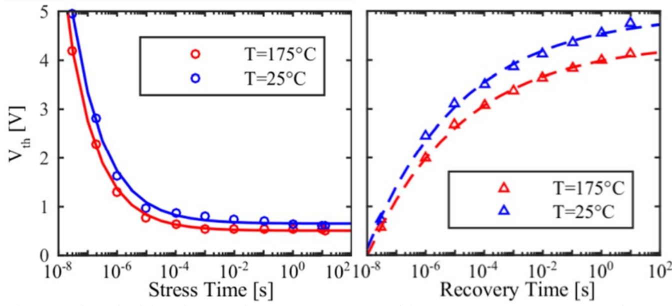

Fig. 5: Threshold voltage after neg. stress and its recovery at (V_g=-10V/0V) at T=25°C and T=175°C. Shown is on the left the saturation of V_{th} after stress at V_g=-10V with increasing the stress time (circles,). The recovery to return to initial V_{th} at V_g=0V (triangles, right) takes longer than 10s of recovery.

To understand the impact of negative stress voltages during bipolar AC stress, we first analyze the threshold voltage after negative gate bias stress and its recovery (Fig. 5). We observe a large and very fast negative ΔV_{th} under negative stress. Already after stress times of 10µs the negative ΔV_{th} saturates. Obviously, the density of trap centers with capture time constants below 10µs is very high. The emission time constants at Vg=0V are broadly distributed and reach values up to 10s (Fig. 5, on the right). With increasing recovery voltage, the recovery is accelerated and the emission time constants decrease below 1ms (see also Fig. 10). Only a small temperature dependence is observed for the negative gate stress. Due to the shorter capture and emission time constants at T=175°C than at T=25°C, the temperature difference is not captured by a measurement delay of 1 µs. The previously observed sub-threshold hysteresis seen in the difference between IV-curve up-sweeps measurements and down-sweeps explained in [13] is caused by the negative gate stress. Due to the longer measurement delay (compared to our 1µs), already the negative ΔV_{th} has recovered when measuring V_{th}. Nevertheless this effect is only observed in the sub-threshold regime [13]. Our advanced measurement technique provides additional information on the time-dynamics and the capture and emission time constants after positive and negative DC stress.

IV. AC Measurement Results

In the next step, we study the threshold voltage hysteresis introduced by an application-like bipolar AC gate signal with a frequency of 50kHz for different V_{high} and V_{low} combinations (see Fig. 7 a-d)). 50kHz is a typically recommended frequency for applications of SiC MOSFETs. Furthermore, to measure the behavior of V_{th} in real-time during the AC stress, we interrupt the AC stress at different positions during the AC signal (see Fig. 6 b)). For these experiments, the settling time of the V_{th}-readout is 1µs and the recorded recovery of V_{th} (up to 10ms) is shown in Fig. 6 c) for each interruption of the AC gate signal. The measurement destroys the trap occupation state. To fully restore the pre-measurement trap occupation state, before each interruption of the AC gate signal, another 100ms of AC stress are applied (see Fig. 6 a)). The used stress times are very short, so as discussed before, only the traps with short capture and emission times are activated. Applying another AC stress of 100ms therefore does not increase the long-term V_{th} as seen in Fig. 3 on the left). In Fig. 6 d), the first measurement points of V_{th} with a measurement delay of 1µs are shown with respect to their timing position during the AC signal.

In Fig. 7 a) and b), the measured V_{th} at T=175°C during a 50kHz AC signal is shown for two different V_{high} and V_{low} combinations of the AC signal. Short-term hysteresis of the threshold voltage of up to 4V is observed (see Fig. 7 b) for V_{low}=-10V and V_{high}=20V). For Si MOSFETs the short-term threshold hysteresis during AC stress amounts only to a few mV, due to a very small portion of traps with short capture and emission time constants. For SiC-MOSFETs, the fast decrease in V_{th} during negative gate stress is caused by the previously described capture of holes with capture times below 1µs. The increase in V_{th} during the V_{high} signal is both due to the acceleration of recovery with increasing V_{gate} and also due capture of electrons during positive gate bias stress (see Fig. 3). The capture times for hole capture are a lot faster than for electron capture, which is visible in the fast saturation during the V_{low} signal (compare to electron capture in Fig. 1). The saturation within 10µs is to a first approximation independent on the V_{low} voltage. We performed measurements for the different V_{high} and V_{low} combinations at T=25°C with the same qualitative observations as for the measurements at T=175°C (see Fig. 7 c) and d)). The initial V_{th} at T=25°C is higher due to the intrinsic temperature dependence of the threshold voltage. An analysis of all minimum values of V_{th} during the AC stress of the different V_{high} and V_{low} combinations can be found in Fig. 8 and a comparison of all maximum values of V_{th} during the AC stress in Fig. 9. The minimum value of V_{th} during the AC stress itself is exponentially dependent on V_{low} (see Fig. 8) with a small dependence on V_{high} for both temperatures with an offset mainly due to the higher initial V_{th} at T=25°C. The maximum value of V_{th} (see Fig. 9)

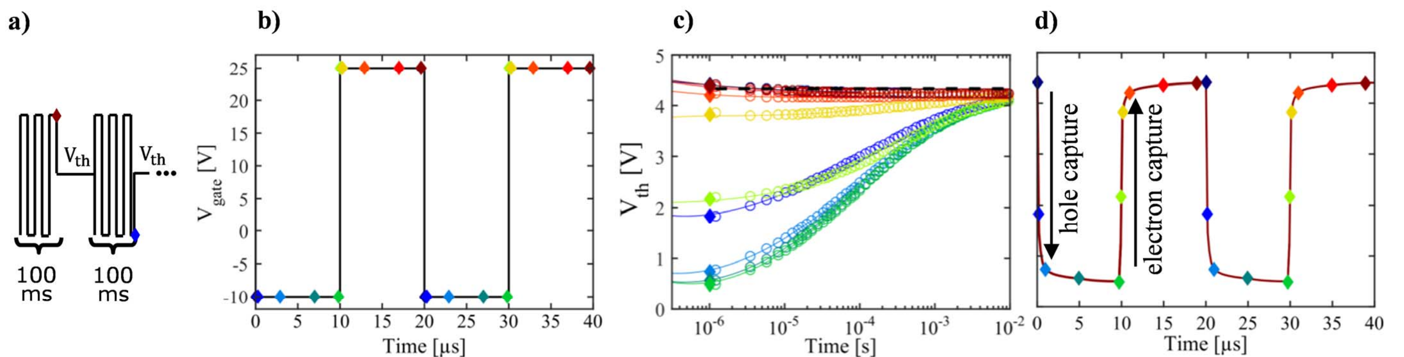

Fig. 6: Explanation of the measurement technique, example with real data (T=175°C, V_{high}=25V, V_{low}=-10V, f=50kHz): **a)** The AC stress is interrupted at different positions in time of the rectangular signal. Directly after end of stress, the threshold voltage is measured from 1µs to 100ms recovery time. Between each measurement point another AC stress of 100ms is applied in order to restore the pre-measurement trap occupation state **b)** An example 50kHz bipolar AC signal is shown with different points of interruption as described for a). In **c)** The V_{th} measurement after each interruption of the AC signal is shown on a logarithmic time scale. **d)** The first measurement point (after 1µs measurement delay) is shown with the corresponding timing position during the AC signal. The threshold voltage hysteresis is mostly due to capture and emission (neutralization) of positive charges (hole capture and electron capture).

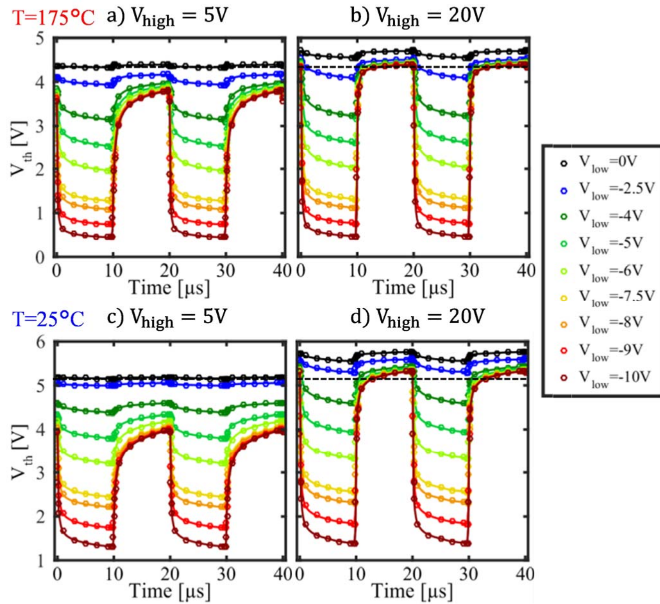

Fig. 7: Threshold voltage hysteresis at a bipolar AC signal with frequency of 50kHz. The measured V_{th} dependence on the AC signal with varied V_{low} is shown for T=175°C with a) V_{high}=5V and b) V_{high}=20V as well as for T=25°C in c) and d). The initial V_{th} is marked as dashed line.

V_{low} and is linearly dependent on V_{high}. For the V_{high} phase, the most interesting parameter is the time it takes to reach the maximum value V_{th} during AC stress. Comparing Fig. 7 a) and Fig. 7 c), we observe a slower increase of the V_{th} after the negative voltage phase for T=25°C. With increasing V_{high} the time until saturation decreases and the difference due to temperature is only visible in the absolute V_{th}. Based on this result, the impact on circuit operation is studied and estimated.

V. IMPACT ON CIRCUIT OPERATION

For Si, the V_{th} hysteresis during a bipolar AC signal amounts to only a few mV and is uncritical. For SiC, the short-term threshold voltage hysteresis has been already observed during the measurement of IV-Curves in a shift of the subthreshold voltage [4]. Fortunately, this effect is not permanent and recovers quickly. Also, the threshold voltage hysteresis itself does not increase after end of life. To estimate the effect of the threshold voltage hysteresis on the circuit operation performance in the sub-µs regime, we take a closer look at the time-constants of the recovery of V_{th} after negative stress back to the initial V_{th}. Most of the negative

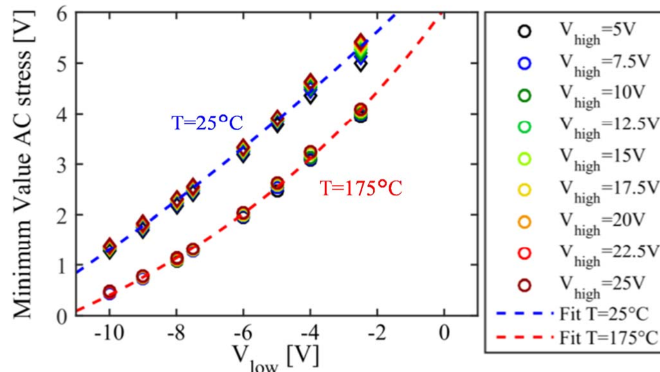

Fig. 8: Minimum V_{th} value during AC stress (see Fig. 7) dependent on V_{low} at T=25°C and T=175°C. It increases with increasing V_{low} (dashed fit) and is roughly independent on V_{high}. Minimum value at T=25°C is increased compared to T=175°C mainly due to the temperature dependence of 0h-V_{th}.

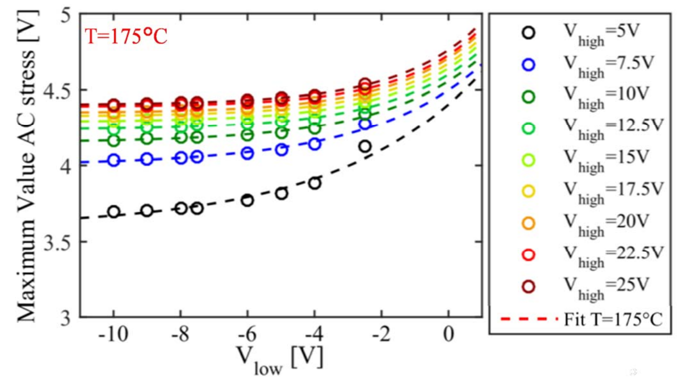

Fig. 9: Maximum V_{th} value during AC stress (compare Fig. 7) increases exponentially with increasing V_{low} at T=175°C (dashed fit). However the more dominant dependence is the linear dependence on V_{high}.

ΔV_{th} disappears within ~100ns after switching V_{gate} back to positive bias (see Fig. 10). The recovery time exponentially depends on the gate voltage during recovery. In these first 100ns the negative ΔV_{th} actually helps to switch the MOSFET faster into the ON-state than without this ΔV_{th}. As a matter of fact, R_{on} is actually lower after negative gate stress which helps to minimize static losses. In Fig. 11 we present the measured R_{on} during the V_{high} period (transistor is "on") of the AC stress for different V_{low} voltages. For the comparison of R_{on} with ΔV_{th}, we use a temperature of T=25°C, because there R_{on} increases and transconductance decreases by a factor of 3 (175°C compared to 25°C), which decreases the impact of ΔV_{th} on R_{on}. Furthermore, we chose V_{high}=10V, because at higher gate voltages (i.e. 15V). ΔV_{th} recovers too fast to be measurable as change in R_{on} (see Fig. 10). Fig. 11 shows that the dependence of R_{on} during AC stress is directly and only correlated to the observed ΔV_{th} during AC stress and shows the same dependencies as ΔV_{th} in Fig. 7. Furthermore, the measured ΔV_{th} during AC stress at T=25°C and V_{high}=10V is used to calculate the change in R_{on} using a IV measurement (R_{on} dependent on the gate voltage) as reference. The observed ΔV_{th} can be directly mapped to R_{on} (see circles in Fig. 11) with a perfect agreement. The R_{on} increases again with recovering V_{th}. An even lower R_{on} in Fig. 11 is expected for $t \leq 1\mu s$. Note that ΔV_{th} is the only reason for ΔR_{on} and can fully explain the changes in magnitude. Possible changes in the mobility apparently do not play a role. This has three highly positive conclusions: First, we can fully explain and model the change in R_{on} during AC stress. Second the change in R_{on} is also fully recoverable as V_{th} and third, R_{on} is lowered during the negative (V_{low}) period of the AC stress and therefore helps to switch the SiC-MOSFET faster, while minimizing static losses.

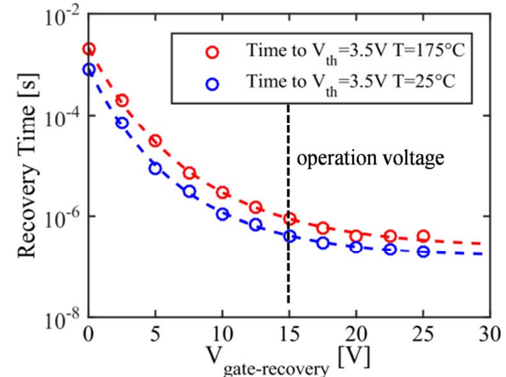

Fig. 10: Recovery from negative stress (Vg=-10V, t_{stress}=10ms) at T=25°C and T=175°C. Shown is the required time at V_{gate} to recover V_{th} back to a value of 3.5V. The required time decreases exponentially with increasing recovery voltage (dashed lines), the charge emission at operation voltage occurs within 100ns after switching to a positive V_g.

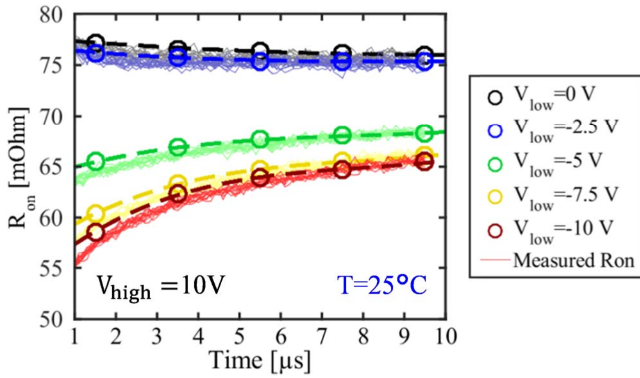

Fig. 11: R_{on} during the V_{high} period of the AC stress as a function of V_{low} with V_{high}=10V with Id=100mA at T=25°C (lines, measurement of 50 AC periods). The change in R_{on} can be directly calculated from the observed ΔV_{th} (circles). The change in R_{on} is therefore during AC stress fully recoverable.

VI. Conclusion

The ΔV_{th} under **positive gate bias stress** contains large fast recovering components which remain undetected during JEDEC-like tests. We observe a strong influence of the measurement delay on the parameters required for lifetime prediction e.g. stress time dependence, measured apparent activation energies and voltage acceleration factors. A JEDEC test with measurement delay of hours will not be sufficient for lifetime predictions under application conditions and has to be improved [12]. An alternative to the standard JEDEC test is to use a preconditioning approach [14], which eliminates the contribution of the fast recovering part of the negative as well as the positive ΔV_{th}. With this approach the lifetime parameter dependence on the measuring delay is drastically reduced, but information about all fast recovering components is lost. To investigate the impact of the fast recovering components, we propose utilizing only gate bias stress occurring in the application (negative DC and AC only) and a shortest possible measurement delay (e.g. 1µs).

We presented a measurement technique using a bipolar AC gate bias stress, which is application-relevant and has a well-defined stress history exactly like in the application. Our measurements show that applying a **bipolar AC gate bias stress** causes large and very fast fully recoverable threshold hysteresis as seen before in [4] with magnitudes >4V. We can fully explain this behavior as being due to capture of positive charges in the oxide and at the interface when the gate is negative and neutralization of these positive charges as well as capture of negative charges within the 10µs AC-positive period. We also observe a voltage acceleration of the positive charge emission as well as capture of negative charges in the oxide when the gate is positive. Utilizing a fast measurement technique, we are able to determine the time constants for capture and emission of these positive and negative charges as a function of the applied bias. The neutralization of the positive charges occurs within ~100ns after switching the gate to a positive voltage. It is clear that the threshold hysteresis during normal operation mode makes a standard SPICE model, which assumes a fixed threshold, not usable to explain effects caused by this threshold hysteresis. Therefore, we use CET maps and we are able to calculate V_{th} at any stress history, enabling lifetime modeling of SiC transistors (work in progress). We have also shown that we can fully explain and model the change in R_{on} during AC stress, which is as the V_{th} fully recoverable. It is also demonstrated that R_{on} has no harmful effect when the MOSFET works in a switch-mode converter, because R_{on} is lowered during the negative period of the AC stress and therefore helps to switch the SiC-MOSFET faster while minimizing static losses and temperature increase of the device.

VII. References

[1] T. Kimoto, “Material science and device physics in SiC technology for high-voltage power devices,” *Japanese Journal of Applied Physics*, vol. 54, no. 4, p. 40103, 2015.

[2] G. Liu, B. R. Tuttle, and S. Dhar, “Silicon carbide: A unique platform for metal-oxide-semiconductor physics,” *Applied Physics Reviews*, vol. 2, no. 2, p. 21307, 2015.

[3] A. J. Lelis, R. Green, D. B. Habersat, and M. El, “Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 316–323, 2015.

[4] T. Okunishi *et al.*, “Reliability study on positive bias temperature instability in SiC MOSFETs by fast drain current measurement,” *Japanese Journal of Applied Physics*, vol. 56, no. 4S, 04CR01, 2017.

[5] G. Rescher, G. Pobegen, and T. Grasser, “Threshold voltage instabilities of present SiC-power MOSFETs under positive bias temperature stress,” in *Materials Science Forum*, 2016, pp. 481–484.

[6] T. Grasser *et al.*, “Recent advances in understanding the bias temperature instability,” in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, p. 4.

[7] H. Reisinger *et al.*, “Analysis of NBTI degradation-and recovery-behavior based on ultra fast VT-measurements,” in *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International*, 2006, pp. 448–453.

[8] T. Grasser *et al.*, “Analytic modeling of the bias temperature instability using capture/emission time maps,” in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, 27-4.

[9] G. Pobegen and T. Grasser, “On the distribution of NBTI time constants on a long, temperature-accelerated time scale,” *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2148–2155, 2013.

[10] C. Schlünder, W. Heinrigs, W. Gustin, and H. Reisinger, “On the impact of the NBTI recovery phenomenon on lifetime prediction of modern p-MOSFETs,” in *Integrated Reliability Workshop Final Report, 2006 IEEE International*, 2006, pp. 1–4.

[11] G. Pobegen, T. Aichinger, M. Nelhiebel, and T. Grasser, “Understanding temperature acceleration for NBTI,” in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, 27-3.

[12] *JEDEC Standard: Temperature, bias, and operating life*. JESD22-A108D.

[13] G. Rescher, G. Pobegen, T. Aichinger, and T. Grasser, “On the subthreshold drain current sweep hysteresis of 4H-SiC nMOSFETs,” in *Electron Devices Meeting (IEDM), 2016 IEEE International*, 2016, pp. 10–18.

[14] Gerald Rescher, T. Aichinger, Gregor Pobegen, “Comprehensive Evaluation of Bias Temperature Instabilities on 4H-SiC MOSFETs Using Device Preconditioning: (to be published),” *ICSCRM*, 2017.