NANO LETTERS

pubs.acs.org/NanoLett

Anomalous Piezoresistance Effect in Ultrastrained Silicon Nanowires

A. Lugstein,*,† M. Steinmair,† A. Steiger,‡ H. Kosina,§ and E. Bertagnolli†

†Institute for Solid State Electronics, Vienna University of Technology, Floragasse 7, A-1040 Vienna, Austria, ‡Institute for Solid State Physics, Vienna University of Technology, Wiedner Hauptstr. 8/052, A-1040 Vienna, Austria, and §Institute for Microelectronics, Vienna University of Technology, Gusshausstrasse 27-29, A-1040 Vienna, Austria

ABSTRACT In this paper we demonstrate that under ultrahigh strain conditions p-type single crystal silicon nanowires possess an anomalous piezoresistance effect. The measurements were performed on vapor−liquid−solid (VLS) grown Si nanowires, monolithically integrated in a microelectro-mechanical loading module. The special setup enables the application of pure uniaxial tensile strain along the ⟨111⟩ growth direction of individual, 100 nm thick Si nanowires while simultaneously measuring the resistance of the nanowires. For low strain levels (nanowire elongation less than 0.8%), our measurements revealed the expected positive piezoresistance effect, whereas for ultrahigh strain levels a transition to anomalous negative piezoresistance was observed. For the maximum tensile strain of 3.5%, the resistance of the Si nanowires decreased by a factor of 10. Even at these high strain amplitudes, no fatigue failures are observed for several hundred loading cycles. The ability to fabricate single-crystal nanowires that are widely free of structural defects will it make possible to apply high strain without fracturing to other materials as well, therefore in any application where crystallinity and strain are important, the idea of making nanowires should be of a high value.

KEYWORDS Nanowire, strained silicon, piezoresitivity, mobility

The various effects of strain on silicon and germanium have been studied since the 1950s.[1] It was recognized early, that if the band structure is changed due to strain, many material properties are altered including, and most significant to silicon technology, band gap, effective mass, carrier mobility as well as diffusivity of dopants, and oxidation rate.[2] In particular the piezoresistance effect, changing electrical resistance of a material due to applied mechanical stress, was quickly adopted to realize micro-electro-mechanical sensors systems.[3] This strain effect on the transduction physics of silicon-based piezoresistive sensors is closely related to the carrier mobility enhancement in strained Si-CMOS.[4−9] Strained Si on silicon−germanium substrates was explored in an effort to boost carrier mobility since the early 1990s.[10−13] In only a few short years, both, localized tensile as well as compressive strain was being deliberately introduced in a variety of ways to enhance carrier mobility in high performance devices.[14−16] Today, almost every semiconductor manufacturer has announced their version of strained CMOS.[17]

The effects of high strain levels on the electronic and optical properties of nanowires have been, however, largely overlooked up to now, although the electrical and optical properties of nanowires have been extensively studied. In situ tuning of high strain levels has proved to be challenging as the nanostructures have to be interfaced with electrodes which guarantee reliable contacts even when subjected to such mechanical forces, where surface imperfections may initiate fractures.[18] Very recently Gordon et al. have shown that the "effective" Young's modulus increased slightly as nanowire diameter decreased, but fracture strength increased by 2−3 orders of magnitude.[19] Within their investigations VLS grown Si nanowires grown with a colloidal catalyst were the most mechanically sound with high modulus and high fracture stress (>1 GPa). A reduction in diameter as large as 426% (the ratio of initial diameter over breakpoint diameter as a percentage) and 125% elongation ratio were obtained at ambient temperature for a nanowire with an original diameter of 26 nm.[20]

However, most of the approaches, such as the commonly used four-point bending method,[21] are applicable to study the piezoresistive behavior of nanowires only at low strain levels.[22−27] On the basis of a microelectro-mechanical loading system, we developed a special technique enabling maximum strain levels up to 3.5% on monolithically integrated VLS grown crystalline Si nanowires. Thereby we can induce uniform tensile strain in these individual Si rods while measuring simultaneously the resistance of the nanowire. The use of nanowires enables us to avoid the defects and variations that make it difficult to study standard ultrastrained silicon that has so many dislocations and defects that strain measurements are not accurate.

Figure 1a shows the schematic view and Figure 1b shows the scanning electron microscopy (SEM) image of the microelectro-mechanical testing module with the suspended Si nanowire (see inset in Figure 1b).

*To whom correspondence should be addressed. E-mail: alois.lugstein@tuwien.ac.at.

Received for review: 06/21/2010
Published on Web: 07/13/2010

DOI: 10.1021/nl102179c | *Nano Lett.* **2010,** *10,* 3204–3208

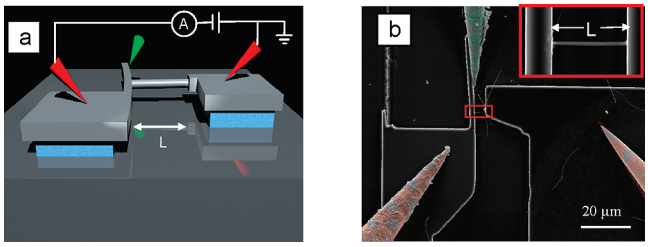

FIGURE 1. (a) Schematic illustration and (b) SEM image of the microelectro-mechanical loading system for tensile testing of a suspended Si nanowire and measuring the resistance change simultaneously. The inset of Figure 1b shows a monolithically integrated 5.81 μm long single crystal Si nanowire with a diameter of about 100 nm. The Si nanowire under test is anchored with one end to a suspended cantilever and with the other end to the opposed insulated Si pad. The green-inked tip is used to apply stress to the freestanding cantilever which further applies strain to the suspended Si nanowire. The red-inked needle probes complete the electrical circuit used to measure the resistance changes during straining.

A freestanding Si-cantilever with $\{111\}$ faceted sidewalls was processed out of a highly boron doped $\langle 110\rangle$ top layer of a silicon on insulator (SOI) wafer by photo lithography, reactive ion etching, and partial removal of the buried oxide by wet etching. Successively, gold colloids with a diameter of 80 nm in aqueous solution were placed selectively on the $\{111\}$ oriented sidewall of the freestanding cantilever by dielectrophoresis. The Si nanowires were synthesized by VLS growth in a hot wall chemical vapor deposition reactor using SiH_4 as precursor.[28] Thereby synthesis parameters were chosen to grow epitaxially, $\langle 111\rangle$-oriented Si nanowires perpendicular to the $\{111\}$ surface of the cantilever to force them to impinge onto the opposite sidewall forming a self-welded contact.[29] The distance between the cantilever and the opposite Si pad was varied for the diverse devices on the chip to enable investigations of nanowires of different lengths L (see Figure 1). Finally, we ended up with suspended Si nanowires, $L = 2.5-7$ μm long, and all of them about 100 nm in diameter, anchored with one end to the suspended cantilever due to epitaxial growth, and attached with the other end to the opposed Si pad.

The transmission electron microscopy (TEM) image in Figure 2 shows the interface region of such epitaxial grown Si nanowires on a Si$\{111\}$ surface.

The dashed line in the high-resolution TEM image represents the substrate/Si nanowire interface. No grain boundaries, abrupt interfaces, or misfit dislocations were observed in this region and the interface appears to be coherent, unstrained, and epitaxial silicon to silicon. It was already demonstrated previously that such grown epitaxial nanowires exhibit extraordinarily robust electrical and mechanical connections.[30,31] The intimate contact between the epitaxial Si nanowires and the micro scale Si electrodes enable to apply exceptional high strain levels and to measure the longitudinal resistance change simultaneously.

By exerting a perpendicular force on the freestanding cantilever by means of a micromanipulator, as indicated in Figure 1, an essentially uniaxial tensile force is inherently

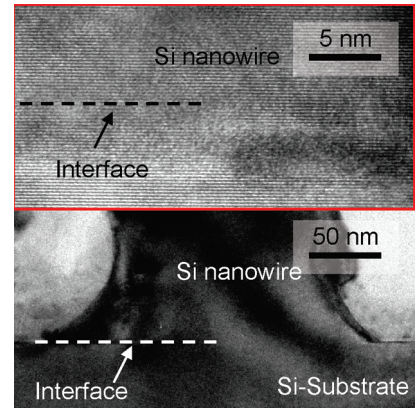

FIGURE 2. Cross-sectional low-magnification, bright-field TEM image of a Si$\langle 111\rangle$ nanowire grown epitaxially on a Si$\{111\}$ surface and the respective high-resolution TEM image of the substrate−nanowire interface region.

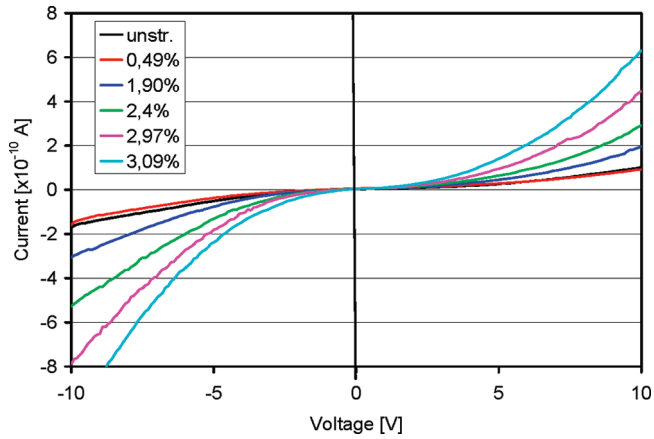

FIGURE 3. I/V characteristics of a suspended Si nanowire, 4.04 μm in length and 100 nm in diameter at various strain levels, as indicated in the legend. The measurements are performed by applying a voltage sweep from −10 to +10 V and by simultaneously reading the current flow.

applied along the $\langle 111\rangle$ growth direction of the suspended Si nanowire (see video in the Supporting Information). This special setup enables high strain levels (up to 3.5% elongation of the nanowire) with no shear component of the stress. The length and elongation of the Si nanowire under stress was determined in situ by SEM imaging, measuring the distance between the two ends of the nanowire. The epitaxial growth of the Si nanowires perpendicular to the cantilever (i.e., to the direction of the electron beam) enables a precise measurement of the nanowire elongation with approximately 10 nm precision without any "hidden" displacement along the electron beam direction.

To characterize the overall electrical response of such a suspended Si nanowire device we applied a voltage sweep from −10 to 10 V and monitored the current flow in the wires at different strain levels. Figure 3 illustrates the typical I/V characteristic of a suspended 4.04 μm long Si nanowire for various strain levels. Such two-terminal I/V measurement setup data comprise the resistance of the nanowire, the

DOI: 10.1021/nl102179c | *Nano Lett.* **2010,** *10,* 3204–3208

contact resistance between the nanowire and the Si electrodes and the resistance between the electrodes and the probe needles. For the heavily doped electrode regions, the contribution of the resistance between the electrodes and the probes was found to be negligible.

Four-probe measurements of such grown Si nanowires revealed an intrinsic resistivity $\rho_{NW} = 20\ \Omega$cm (see Supporting Information). The conductivity-type of the nanowire was determined by a nanowire-FET with back gate geometry exhibiting a field effect response characteristic of a p-type semiconductor (see Supporting Information). Such p-type behavior is a common observation in field−effect measurements of Si nanowires without intentional doping.[32,33] As the p-type Si nanowires and the heavily p-doped Si electrodes of the microelectro-mechanical loading module are of the same conductivity type, good electrical connection has to be expected.

As expected for low strain levels, we observed a slight decrease of the current with increasing strain. This trend is qualitatively consistent with the longitudinal piezoresistance behavior of bulk Si along the ⟨111⟩ directions.[34] In semiconductors, particularly in indirect band gap semiconductors, mechanical stress affects the electronic band structure, thus modifying the effective electron mass, the mobility, and the resistivity ρ.

As the nanowires will be elongated and become slightly thinner when being pulled, the change in resistance caused by an applied stress is the result of both, dimensional changes, and piezoresistivity. Thus, the relation between the relative resistance change in a piezoresistive element, R/R_0, subjected to uniaxial stress, is given by

$$R/R_0 = (1 + 2\nu)\varepsilon_L + \rho/\rho_0$$

where ν is the Poisson's ratio and ε_L is the strain along the piezoresistor with resistance, R. The resistance and the resistivity in the unstressed material are denoted by R_0 and ρ_0, respectively. As the observed changes in resistance are significantly larger than the dimension changes, we converted relative changes in resistance to the relative change in resistivity $\Delta\rho_0$, subtracting the dimensional parameters but neglecting the dimensional changes of the nanowires.

The nonlinear I/V characteristics in Figure 3 indicate that transport through the nanowire is space charge limited.[35] In this regime, the carrier concentration is low and the current unipolar. Ideally, the current density depends quadratically on the applied voltage

$$J_p = \xi\varepsilon\mu_p V^2/L^3$$

In this specific relation for nanowires,[36] the geometric prefactor ξ depends on the ratio R/L, ε is the dielectric constant of the semiconductor, and μ_p is the hole mobility. This relation shows that a significant change in current due to strain can only be attributed to a significant mobility change. The amount of mobile charge is modulated by the applied voltage, and is rather insensitive to bandgap, barrier heights and carrier lifetimes. The main assumption that the current will remain unipolar also in the presence of strain-induced bandgap narrowing is discussed below.

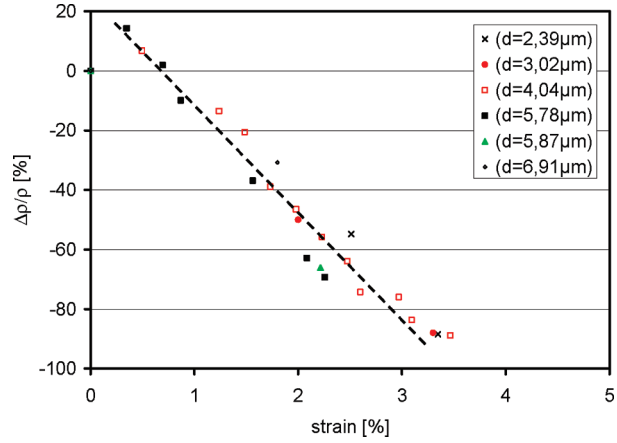

FIGURE 4. Relative changes in resistivity $\Delta\rho/\rho_0$ versus strain of the ⟨111⟩-oriented Si nanowires all with diameters of about 100 nm and different length as indicated in the legend.

Figure 4 shows the relationship between relative change in resistivity and strain for Si nanowires of different length obtained from the measurement of the fractional change of resistivity at different tensile loads. As the trend is qualitatively the same independent of the nanowire length, we propose that the contact resistance remain stable independent of the stress level.

In accordance with the longitudinal piezoresistance behavior of bulk Si along the ⟨111⟩ directions, we observed the expected increase of the resistance for strain levels up to about 0.8%. This trend is also qualitatively consistent with the findings of He and Yang, which have shown that the conductance decreases under tension and increases under compression for VLS grown p-type Si⟨111⟩ nanowires.[34] Though their investigations were restricted to rather low strain values of about 0.06%, they measured an unusually large piezoresistance effect compared with bulk. Such enhancement of piezoresistance effects has also been reported in Si beams defined by electron beam lithography.[37]

Most remarkably for ultrastrained Si nanowires we observed an anomalous and giant decrease of the resistivity with the change in resistivity being proportional to the strain. In the current work, the conductivity of the 100 nm thick Si nanowires could be increased 10-fold for 3.5% elongation.

So far no experimental results of piezoresistivity in such ultrastrained silicon were available. Theoretical calculations based on measured bulk silicon piezoelectric coefficients predict for tensile uniaxial strain an enhancement for both, electron, and hole mobilities.[38] Fischetti et al. calculated a extremely large increase of the hole mobilities (10 times

DOI: 10.1021/nl102179c | Nano Lett. 2010, 10, 3204–3208

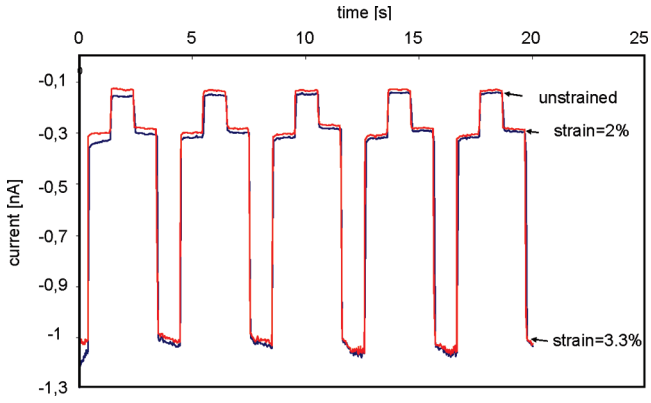

FIGURE 5. Dynamic response of the current through a suspended 2.39 μm long Si nanowire when the structure is subjected to cyclic loading between three levels (relaxed nanowire, 2% strained, 3.3% strained). The red and black line show the respective currents at the two tips where one was grounded and the other one biased to −5 V.

enhancement) for heavily strained (5%) materials.[13] They stated that these results are not too meaningful from a practical perspective as layers subject to such a high strain can only be grown up to very small thicknesses, if at all, before the strain will be relieved by the formation of dislocations and other defects. The ability to fabricate single-crystal nanowires of Si that are free of structural defects makes it possible to apply such high strain without plastic deformation or fracturing of the material. Such nanowires withstand high stress levels before the strain will be relieved by the formation of dislocations and other defects.

To investigate reliability and fatigue resistance of the nanowires in our mechanical loading system, we performed tests under cyclic loading. No fatigue failure was observed for high strain amplitudes (3.3%) up to several hundred cycles (see movie in the Supporting Information). For strain levels above 3.5% the Si nanowires fail via sudden brittle fracture at the self-welded nanowire-Si-electrode contact. In addition to monitoring the mechanical stability under long-time cycle tension, the resistance changes of the nanowire was measured simultaneously under cyclic loading for three constant strain levels. Figure 5 shows a time sequence of the Si nanowire current changes, when the device is successively exposed to tensile cycle loading for 2 strain levels. As expected, the electrical response (I/V versus time) for the Si nanowire shows well-reproducible two levels.

We have further analyzed the effect of strain on the resistivity by means of numerical simulation. The two dominant strain effects considered were a change in mobility and bandgap narrowing. Our simulations clearly show that at room temperature even a considerably reduced bandgap does not give any relevant contribution of the minority carriers to the total current. The same holds if carrier lifetimes are varied by a few orders of magnitude. This means that the current remains unipolar and the reduction in resistivity can only be attributed to a mobility increase and not to the onset of a bipolar conduction mechanism. A significant minority current component would only develop at some sufficiently high temperature of the nanowire. However, the measurement data rule out the assumption that self-heating and the resulting increase of the intrinsic carrier concentration, which would be strain-dependent via the band gap, could explain the observed resistivity reduction. Indeed, qualitatively the same characteristic resistivity reduction can be extracted for both 1 and 10 V applied voltage, which translates into a difference of 2 orders of magnitude in the dissipated heat (see Supporting Information). Since this huge difference does not qualitatively alter the resistivity characteristics, the latter cannot be explained by effects related to self-heating. The simulations performed indicate that the resistivity characteristics mainly reflect the strain-dependent hole mobility, and that the current measured is unipolar and the space charge limited. The effect of strain on the surface depletion layer has been neglected in the simulation. Rowe[39] suggested that the resulting piezo-pinch effect in nanowires is the origin of the giant piezo resistance reported by He and Yang.[34] However, this effect can only explain the resistivity increase at low strain, but not the reduction at high strain. Taking the piezo-pinch effect into account would require an even higher mobility increase to explain the measured resistivity decrease.

Closing, strain engineering involves just smoothly deforming the material and strained Si nanowires would be a semiconductor that has a tunable resistivity while keeping its other unique characteristics. There is a vast geometric and orientational parameter space over which the piezoresistive properties can be tuned, and it is unlikely that the nanowire geometries, orientation, and doping parameters studied here will prove optimal for maximum piezoresistive response. While the anomalous piezoresistive phenomenon obtained in ultrastrained Si nanowires may pave the way toward sensitive, silicon compatible strain gages or high-performance nanoelectronic devices, these effects should apply to many substances beyond Si.

Acknowledgment. This work is partly funded by the Austrian Science Fund (Project No. 20937-N14) and the Austrian Society for Micro- and Nanoelectronics. Technical Support by USTEM TU-Wien is gratefully acknowledged.

Supporting Information Available. Field-effect measurements and calculation of the channel mobility, relative change in resistivity versus strain, additional figures, additional references, and video. This material is available free of charge via the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

(1) Smith, C. S. *Phys. Rev.* **1954**, *94*, 42.
(2) Chidambaram, P. R.; Bowen, C.; Chakravarthi, S.; Machala, C.; Wise, R. *IEEE Trans. Electron Devices* **2006**, *53*, 944.
(3) Craddock, R. Colloquium on Sensing Via Strain. *IEE Conf. Publ.* **1993**, *191*, 5/1−5/4.
(4) Smith, C.; Jones, M. E. *Superlattices Microstruct.* **1998**, *4*, 391.
(5) Chao, C. Y. P.; Chuang, S. L. *Phys. Rev. B* **1992**, *46*, 4110.
(6) Huang, L. J. *Electron Eng.* **2002**, *74*, 34.

DOI: 10.1021/nl102179c | *Nano Lett.* **2010,** *10,* 3204–3208

(7) Fischetti, M. V.; Gamiz, F.; Hansch, W. *J. Appl. Phys.* **2002**, *92*, 7320.
(8) Thompson, S. E.; Armstrong, M.; Auth, C. A. *IEEE Trans. Electron Devices* **2004**, *25*, 191.
(9) Richter, J.; Hansen, O.; Larsen, A. N. *Sens. Actuators, A* **2005**, *123−124*, 388.
(10) Rim, K.; Welser, J.; Hoyt, J. L.; Gibbons, J. F. *IEDM Tech. Dig.* **1995**, 1026.
(11) Nayak, D. K.; Goto, K.; Yutani, A.; Murota, J.; Shiraki, Y. *IEEE Trans. Electron Devices* **1996**, *43*, 1709.
(12) Ghani, T.; Armstrong, M.; Auth, C.; Bost, M.; Charvat, P.; Glass, G.; Hoffmann, T.; Johnson, K.; Kenyon, C.; Klaus, J.; McIntyre, B.; Mistry, K.; Murthy, A.; Sandford, J.; Silberstein, M.; Sivakumar, S.; Smith, P.; Zawadzki, K.; Thompson, S.; Bohr, M. A. *Proc. IEDM* **2003**, 978.
(13) Fischetti, M. V.; Laux, S. E. *J. Appl. Phys.* **1996**, *80*, 2234.
(14) Chidambaram, P. R.; Smith, B. A.; Hall, L. H.; Bu, H.; Chakravarthi, S.; Kim, Y.; Samoilov, A. V.; Kim, A. T.; Jones, P. J.; Irwin, R. B.; Kim, M. J.; Rotondaro, A. L. P.; Machala, C. F.; Grider, D. T. *VLSI Symp. Tech. Dig.* **2004**, 48.
(15) Ghani, T.; Armstrong, M.; Auth, C.; Bost, M.; Charvat, P.; Glass, G.; Hoffmann, T.; Johnson, K.; Kenyon, C.; Klaus, J.; McIntyre, B.; Mistry, K.; Murthy, A.; Sandford, J.; Silberstein, M.; Sivakumar, S.; Smith, P.; Zawadzki, P.; Thompson, S.; Bohr, M. *IEDM Tech. Dig.* **2003**, 1161.
(16) Ota, K.; Sugihara, K.; Sayama, H.; Uchida, Z.; Oda, H.; Eimori, T.; Morimoto, H.; Inoue, Y. *IEDM Tech. Dig.* **2002**, 27.
(17) Lee, M. L. *J. Appl. Phys.* **2005**, *97*, 11101.
(18) Pearson, G. L.; Read, W. T. R.; Feldmann, W. L. *Acta Metall.* **1957**, *5*, 181.
(19) Gordon, M. J.; Baron, T.; Dhalluin, F.; Gentile, P.; Ferret, P. *Nano Lett.* **2009**, *9* (2), 525.
(20) Han, X.; Zheng, K.; Zhang, Y. F.; Zhang, X.; Zhang, Z.; Wang, Z. L. *Adv. Mater.* **2007**, *19*, 2112.
(21) Lund, E.; Finstada, T. G. *Rev. Sci. Instrum.* **2004**, *11*, 75.
(22) Han, X. D.; Zheng, K.; Zhang, Y. F.; Zhang, X. N.; Zhang, Z.; Wang, Z. L. *Adv. Mater.* **2007**, *19*, 2112.
(23) Li, X. X.; Ono, T.; Wang, Y. L.; Esashi, M. *Appl. Phys. Lett.* **2003**, *83*, 3081.
(24) Hoffmann, S.; Utke, I.; Moser, B.; Michler, J.; Christiansen, S. H.; Schmidt, V.; Senz, S.; Werner, P.; Gösele, U.; Ballif, C. *Nano Lett.* **2006**, *6*, 622.
(25) Paulo, A. S.; Arellano, N.; Plaza, J. A.; He, R.; Carraro, C.; Maboudian, R.; Howe, R. T.; Bokor, J.; Yang, P. D. *Nano Lett.* **2007**, *7*, 1100.
(26) Heidelberg, A.; Ngo, L. T.; Wu, B.; Phillips, M. A.; Sharma, S.; Kamins, T. I.; Sader, J. E.; Boland, J. J. *Nano Lett.* **2006**, *6*, 1101.
(27) Lund, E.; Finstad, T. G. *Rev. Sci. Instrum.* **2004**, *75*, 4960.
(28) Lugstein, A.; Hyun, J. Y.; Steinmair, M.; Dielacher, B.; Hauer, G.; Bertagnolli, E. *Nanotechnology* **2008**, *19*, 485606.
(29) Lugstein, A.; Steinmair, M.; Hyun, Y.; Hauer, G.; Pongratz, P.; Bertagnolli, E. *Nano Lett.* **2008**, *8* (8), 2310.
(30) Westwater, J.; Gosain, D. P.; Tomiya, S.; Usui, S.; Ruda, H. *J. Vac. Sci. Technol., B* **1997**, *15*, 554.
(31) Lugstein, A.; Steinmair, M.; Henkel, C.; Bertagnolli, E. *Nano Lett.* **2009**, *9* (5), 1830.
(32) Cui, Y.; Xiangfeng, D.; Jiangtao, H.; Lieber, C. M. *J. Phys. Chem. B* **2000**, *104*, 5213.
(33) Lin, Y. C.; Lu, K. C.; Wu, W. W.; Bai, J.; Chen, L. J.; Tu, K. N.; Huang, Y. *Nano Lett.* **2008**, *8*, 913.
(34) He, R.; Yang, P. *Nat. Nanotechnol.* **2006**, *1*, 42.
(35) Grinberg, A. A.; Luyri, S.; Pinto, M. R.; Schryer, N. L. *IEEE Trans. Electron Devices* **1989**, *36*, 1162.
(36) Talin, A. A.; Leonard, F.; Swartzentruber, B. S.; Wang, X.; Hersee, S. D. *Phys. Rev. Lett.* **2008**, *101*, No. 076892.
(37) Toriyama, T.; Sugiyama, S. *Sens. Actuators, A* **2003**, *108*, 244.
(38) Buca, D.; Holländer, B.; Feste, S.; Lenk, St.; Trinkaus, H.; Mantl, S.; Loo, R.; Caymax, M. *Appl. Phys. Lett.* **2007**, *90*, 032108.
(39) Rowe, A. C. H. *Nat. Nanotechnol.* **2008**, *3*, 311.

DOI: 10.1021/nl102179c | *Nano Lett.* **2010,** *10,* 3204--3208