Calibrated Nanoscale Dopant Profiling and Capacitance of a High-Voltage Lateral MOS Transistor at 20 GHz Using Scanning Microwave Microscopy

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***Abstract*—We quantitatively image the doping concentration and the capacitance of a high-voltage lateral metal-oxide-semiconductor transistor device with a channel length of 0.5 μm at 20-GHz frequency using scanning microwave microscopy (SMM). The transistor is embedded in a deep n-well forming a flat pn-junction with the p-substrate, with the shape of the pn-junction resolved in the SMM images. Calibrated *dC/dV* imaging of the device revealed doping concentration values in the range of 10^{15}–10^{19} atoms/cm^3, including the p-body, n-drift region, n-source-diffusion, as well as all the pn-junctions and the silicon/oxide interfaces at a minimum feature size of 350 nm and SMM electrical resolution of 60 nm. SMM doping concentrations have been compared with technology computer-aided design simulations, resulting in a quantitative agreement between model and experiment. *dC/dV* images have been acquired at different tip dc bias voltages, allowing to determine the p and n dopant polarity. From the reflection scattering S_{11} signal calibrated capacitance measurements have been obtained from the various transistor regions in the range of 300 aF to 1 fF. The results suggest that both *dC/dV* dopant profiling and capacitance measurements can be used for quantitative nanoscale semiconductor device imaging.**

***Index Terms*—Dopant profiling, microwave, nanoscale, scanning microwave microscopy, semiconductors.**

I. Introduction

DOPANT concentration is one of the most important parameters to properly determine and control the design, the functionalities, and the performance of solid-state electronic devices. With the size of modern devices shrinking, dedicated characterization techniques have been developed to meet lateral resolution requirements while guaranteeing the necessary doping sensitivity and doping polarity specificity. Non-destructive probing of the region of interest within the device is also often requested. Scanning Microwave Microscopy (SMM) is a non-destructive technique that allows probing the doping concentration of surface and sub-surface localized features [1]–[9] with nanoscale lateral resolution. Moreover, its broadband 1–20 GHz operating range allows tuning the measuring frequency while giving access to both dielectric [10]–[13] and conductivity [14]–[17] properties including the presence of dopants [15], [18]–[20]. Unlike invasive imaging techniques such as Scanning Spreading Resistance Microscopy (SSRM), SMM-experiments can be performed with virtually no sample modification in an ambient environment using a standard atomic force microscope (AFM) and vector network analyzer (VNA). In SMM, the conductive AFM tip acts as nanoscale imaging and microwave probe, resulting in simultaneous topographic and electrical characterization of the sample under test. There are two main SMM operating modes: reflection S_{11} measurements for complex impedance and *dC/dV* imaging for doping profiling. *dC/dV* effectively measures the derivative of a semiconductor *C-V* curve with respect to the bias voltage at a fixed DC bias, whereas from S_{11} reflection measurements calibrated capacitance and resistance images of the sample under test can be obtained. In both cases the conductive AFM tip and the semiconductor form a metal-oxide-semiconductor (MOS) system. In SMM, the probing depth of a semiconductor sample is determined mainly by the skin depth, which depends on the measuring GHz frequency. Accordingly, by choosing a different working point within the 1-20 GHz frequency window one can vary the skin depth, and therefore the probing depth. On a n-type silicon substrate with doping levels ranging from 4×10^{15} atoms/cm^3 to 1×10^{20} atoms/cm^3, the penetration depth would vary between 1.5 mm and 38 μm at 1 GHz, and between 0.3 mm and 9 μm at 20 GHz [18]. For a p-type silicon substrate typical values at 20 GHz range between 0.7 mm for low doping and 10 μm for high doping concentrations.

SMM has been successfully employed to qualitatively characterize semiconductor structures used in different industrial

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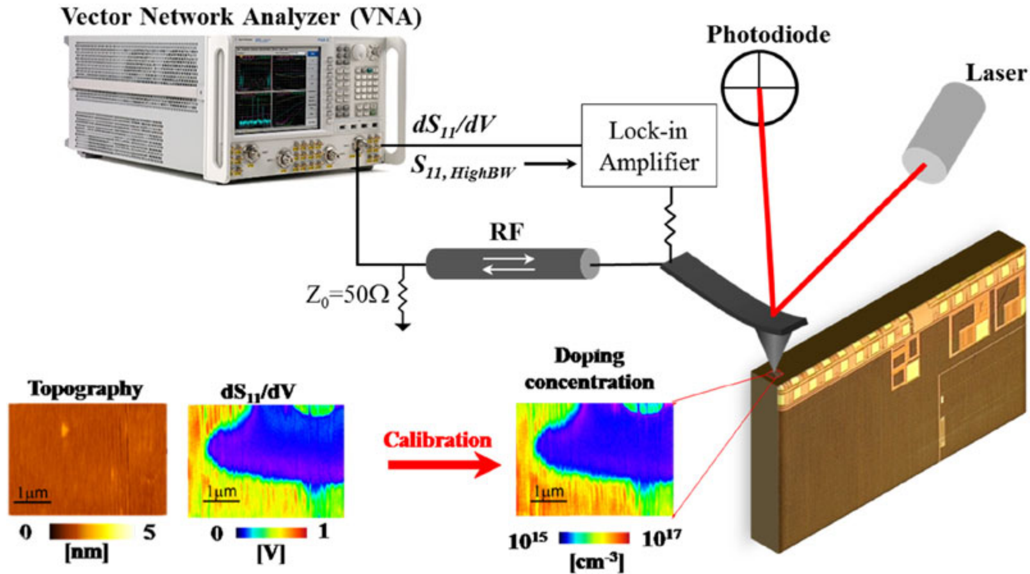

Fig. 1. (a) Scanning Microwave Microscopy (SMM) experimental setup allowing simultaneous acquisition of topography, S_{11} and *dC/dV* of the sample under test. Lower panel: calibration procedure for quantitative doping profiling of a cross-section transistor device. The *dC/dV* image scale is transferred to quantitative dopant values with a dopant calibration sample.

applications [22], [26], [31]–[34]. It was recently shown that the GHz operating frequency can be optimized to obtain a monotonic dependence of the *dC/dV* signal with the doping concentration [35]. Nevertheless, to the best of our knowledge, no work showing quantitative doping concentration as well as capacitance imaging of such semiconductor structures has been yet presented. Here, we demonstrate the capability of SMM to non-invasively and quantitatively probe the doping concentration and capacitance of a high-voltage (HV) lateral MOS transistor (LDMOS) device. The body of this lateral MOS transistor is formed by a diffusion step and therefore the well-known term of an HV LDMOS (lateral diffused) transistor is used. LDMOS devices, where the extension of the gate electrode works as a field-plate, are one of the most interesting structures in the mainstream HV technologies [21]. LDMOS transistors are widely used in telecommunication electronics, dc–dc converters, and mixed-signal circuit design as integrated high-voltage switches and drivers. To quantitatively extract the doping concentration along with the p and n dopant polarity within the device active region, a dopant calibration sample has been used and different DC tip-bias voltages are applied [22]. The SMM results have been compared with Technology Computer-Aided Design (TCAD) simulations, leading to a quantitative agreement between model and experiments.

II. Materials and Methods

A. SMM Setup

A commercial transmission line SMM was used (Keysight Technologies, USA), consisting of a standard 5600 AFM interfaced with a 20 GHz VNA, along with 18 N/m solid platinum AFM tips (RMN, USA). The VNA measures the ratio of the incident and reflected signal at the tip/sample interface, the so called scattering S_{11} parameter. The high tip-sample contact impedance is matched to the sensitive 50 Ω characteristic impedance of the VNA via a half-wavelength coaxial resonator in conjunction with a 50 Ω shunt resistor [23]. The half-wavelength resonator ensures high signal-to-noise ratio with good matching conditions every ∼1 GHz. Since the admittance *Y* scales linearly with the circular frequency ω at a given capacitance C, $Y \sim j\omega C$, it is favorable for the Signal-to-Noise Ratio (SNR) to measure at high frequencies. Accordingly, all the measurements were performed in contact mode at 20 GHz. An intermediate frequency bandwidth (IFBW) of 500 Hz was used, leading to a scan speed of 0.8 line/s (256 points/line).

B. *dC/dV* Imaging for Dopant Profiling

dC/dV imaging was performed connecting a dopant profiling measurement module (DPMM) to the four auxiliary inputs of the VNA. The operating principle is explained in details in [22]. Fig. 1 shows the measurement setup for *dC/dV* experiments. In addition to the GHz signal from the VNA, a kHz signal synthesized by the source of a lock-in amplifier is superimposed using a bias tee and sent to the tip. The sample depletion capacitance changes with the kHz signal, which modulates the reflected GHz signal. This modulation of the reflected signal is detected by the DPMM. A mixer converts the signal into the baseband at zero IF frequency. Subsequently the reflected signal passes through a low-pass filter, and is then sent to the lock-in amplifier operating at the modulation frequency. This final stage rectifies the signal and generates a DC output proportional to the modulation response of the capacitance. In our measurements the incident microwave power was set to -3 dBm (dBm meaning dB per mW input power, thus 0.5 mW), a modulation frequency of 15 kHz, and a modulation drive of 0.5 V were used.

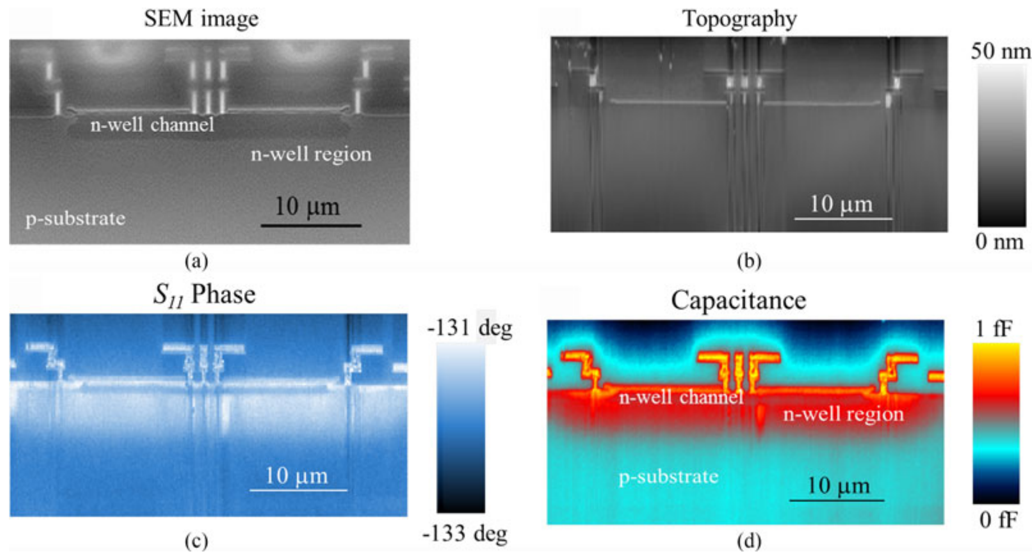

Fig. 2. Cross-section images of a transistor embedded in a deep n-well. The channel length is 10 μm. Scanning Electron Microscopy (SEM) micrograph (a) and SMM (b-d) images. The SEM and the topography images reveal the different areas within the transistor: drift region and drain contact area (left), and source/body area (center). From the S_{11} phase image (c) the calibrated capacitance image (d) is obtained.

C. Dopant Profiling Calibration

For quantitative dopant profiling with *dC/dV*, a well-established calibration workflow, described in details in [22], which effectively converts the *dC/dV* signal into doping concentration values, was used. First, a *dC/dV* amplitude image of a commercially available calibration sample (Infineon Technologies, Germany) [24], is acquired and a dopant calibration curve is generated from it. A flat silicon calibration sample produced by Infineon Munich (shown in Fig. 5(c)), that has both n-type and p-type polarity was used [18], [24]. It consists of a p-Si substrate (10^{15} atoms/cm^3) with 10 different p-type and 10 different n-type implant areas, with doping levels in the range 4×10^{15}–1×10^{20} atoms/cm^3. The n-doped and p-doped regions are next to each other and therefore can be imaged in one SMM scan. In a second step, the *dC/dV* amplitude image of the sample under test is acquired under the same SMM working conditions used in the first step for the calibration sample (i.e. VNA frequency, % drive voltage, DPMM kHz frequency). Using the dopant calibration curve, the *dC/dV* image of the sample is converted into a calibrated dopant concentration image.

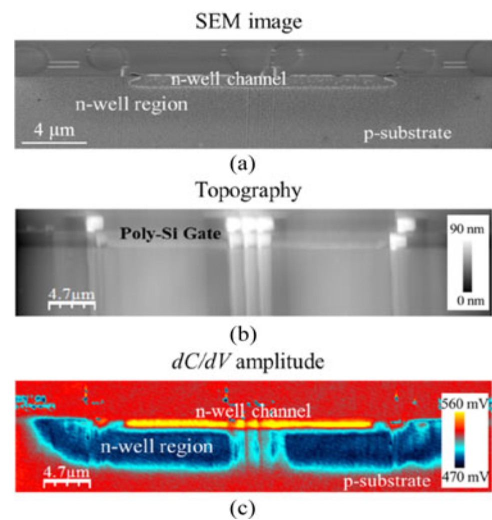

Fig. 3. SEM micrograph (a), SMM topography (b), and *dC/dV* amplitude (c) of the deep n-well region. The channel length is 10 μm. The *dC/dV* contrast depends on the modulation of the depletion zone, and clearly reveals the n-well region as well as the channel. No contrast is obtained in the field oxide and poly-silicon gate regions.

D. Complex Impedance Calibration

The measured S_{11} data were converted into capacitance using the calibration procedure established recently [12]. Thereby, a one-port black-box calibration [25] is employed to convert the measured S_{11} into complex impedance *Z*. For this, three complex error parameters e_{00}, e_{01}, and e_{11} are provided via a simultaneous acquisition of S_{11} and Electrostatic Force Microscopy (EFM) *dC/dz* approach curves. The main advantage of this method is that it works in situ on the sample under test; therefore, no external capacitance calibration sample is required.

E. Cross-Section Transistor Sample

The cross-section transistor sample was designed and fabricated by austriamicrosystems (http://ams.com). A p-type silicon dice with several transistor devices has been cut to obtain a series of cross-section transistors having their active regions accessible with a scanning probe. After cut the sample is exposed to air and a $\sim$1 nm thick native silicon dioxide passivation layer is spontaneously formed. This ensures the presence of the oxide layer and thus of a MOS system when scanning the sample with the SMM conductive probe. In general, SMM works also on non-stoichiometric oxide layers because of the

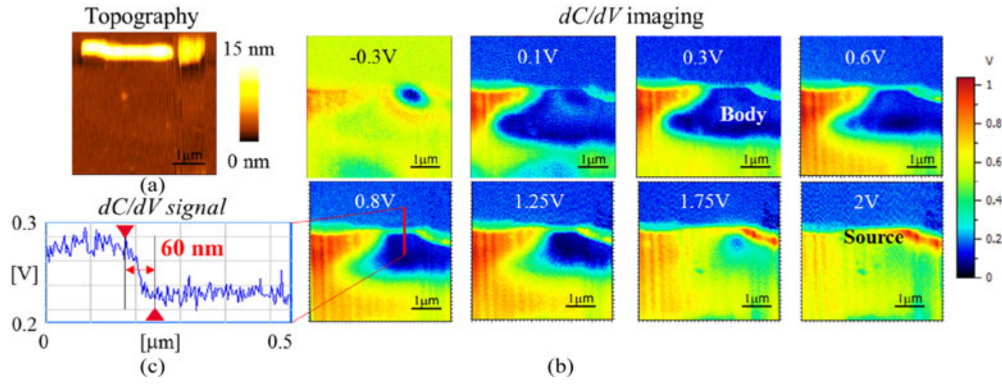

Fig. 4. SMM topography (a) and *dC/dV* phase images with cross-section (b, c) of a transistor cross-section at different DC tip bias voltages. The minimum channel length is 0.5 μm. The topography shows the poly-silicon gate and the field oxide which are higher than the flat active area. The *dC/dV* images show no unspecific topographic cross-talk in the poly-silicon gate and the field oxide (uniform color at the top of each image). Within the flat active region, the *dC/dV* signal shows its sensitivity to the differently p- and n-type doped areas. The electrical lateral resolution is shown in the cross-section (c) of the *dC/dV* image at 0.8 V (red line).

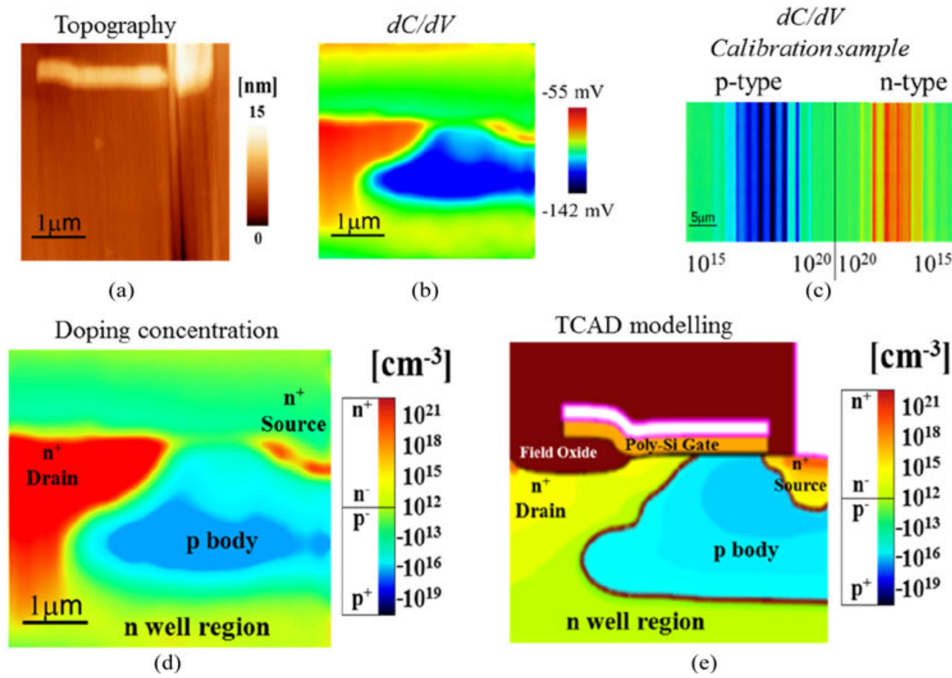

Fig. 5. Calibrated SMM doping concentration of a transistor cross-section. Firstly, SMM topography (a) and *dC/dV* amplitude (b) images are obtained. Then, a dopant calibration sample having n-type and p-type regions is scanned acquiring a calibration *dC/dV* image (c) under the same operating conditions. The raw transistor image is then calibrated resulting in quantitative dopant concentrations (d). The scale bar (n-type in red and p-type in blue, respectively) shows the net-doping concentration – i.e. the difference between donors and acceptors - which defines the electrical conductivity in the considered region. (e) TCAD model of the same area.

GHz-capacitive coupling between tip and sample and the corresponding E-field penetration into the sample [22]. Fig. 1 shows a sketch of the sample, measured in cross-section. The device investigated is an n-channel LDMOS transistor implemented in a CMOS-based HV technology. The minimum feature size is 350 nm. Our study was performed on a 30 μm $\times$ 5 μm active region of a non-butted transistor device embedded in a deep n-well. In particular, a quantitative SMM study has been performed in a 4 μm $\times$ 4 μm area including poly-silicon gate, field oxide, p-body, n+-source, and n+-drain. The part under investigation is a lateral high voltage n-channel transistor with a maximum operating voltage of $V_{DS} = 20$ V. The maximum allowed gate voltage is $V_{GS} = 5$ V. The body well is located in a deep n-well which isolates the body from the substrate. Because of the isolation, the body and source potential can be in between the source supply voltage V_{SS} and the drain supply voltage V_{DD}. The deep n-well potential is defined by the drain potential. To get the appropriate breakdown voltage the drift region below the field oxide has to be balanced with a remaining part of the body well. This results in the typical pn junction curvature shown in this work [see Fig. 4(b) & Fig. 5(e)].

F. TCAD Modelling

For the TCAD setup the SYNOPSYS TCAD software was used. During simulation the option "advanced calibration" was activated. The simulation window was defined in a way to best reflect the drain/drift region and the body/source area of a transistor with a channel length of 0.5 μm. It was assumed that the deep n-well doping profile shows a one-dimensional dopant distribution and that the deep n-well implant boundary is far away from the simulation window. In addition, the depth of the silicon was set to 20 μm to account for the vertical diffusion of the deep n-well.

III. Results and Discussion

A. Calibrated Capacitance of Transistor

The high-voltage (HV) lateral MOS transistor device [SEM image in Fig. 2(a)] has been imaged in cross-section acquiring SMM topography and microwave S_{11} images [see Fig. 2(b) and (c). In the SEM micrograph, both the gate and the deep n-well of the device with a channel length of 10 μm are visible. The SMM topography shows the poly-silicon gate structure that agrees in size and pattern with the SEM data. The microwave images show both gate and n-well regions, confirming the sensitivity of S_{11} to the doping distribution within the material. The S_{11} images have been calibrated [12] into a capacitance image of the transistor [see Fig. 2(d)]. As expected, the highest capacitance value, 1fF, is observed in the metal-like region of the poly-silicon gate. The deep n-well region and its pn junction interface with the p-type substrate are both resolved with roughly 300 aF contrast, with the capacitance being higher in the doped n-well region. Within the active region the capacitance increases with the doping concentration, showing the lowest values in the p-type silicon substrate. Finally, the capacitance image also reveals the n-channel that runs below the field-oxide and poly-silicon gate at 600 aF [see Fig. 2(d)].

B. dC/dV Imaging of the n-Well Region

dC/dV imaging has been performed on the n-channel LDMOS transistor in CMOS HV technology. Fig. 3 shows a SEM micrograph, topography, and *dC/dV* amplitude of the device. The SEM image has been acquired after dipping the device in acid, causing the onset of the small granular structures within the n-well region. The topography and the SEM micrograph show an agreement in the overall dimensions. The *dC/dV* image clearly reveals the differently doped regions within the device's active region, including the deep-n-well, the n-channel, and the flat pn junction formed at the p-substrate/n-well interface. No contrast is obtained in the field oxide and poly-silicon gate top region. This is expected, because the technique is sensitive specifically to voltage induced modulations occurring within the depletion zone underneath the sample surface.

C. DC Tip Bias Manipulation of Charge Carriers

dC/dV imaging resolves the doped regions within the transistor, and further investigations of the doping depletion zone can be done by adding a DC tip bias voltage to the SMM tip. Depending on the sign of the applied bias voltage to the AFM tip, the charge carriers in the semiconductor are attracted or depleted from the surface forming a space charge region. The width of the space charge region in the semiconductor varies with the tip bias affecting the capacitance of the MOS junction. For a given tip bias, the width of the space charge region is also a function of the charge carrier density in the semiconductor, which corresponds to the concentration of impurity donor or acceptor atoms, i.e. the dopant concentration. Measuring the differential capacitance *dC/dV* of the tip-sample interface and its variation with an applied DC tip-sample bias is therefore an important extension for the electrical characterization of semiconductors. As such, the local charge carriers are modulated by the DC voltage bias, and the *dC/dV* signal is used to simultaneously read-out the effects on the depletion zone. Fig. 4 shows *dC/dV* images at different tip-bias voltages on a transistor with a channel length of 0.5 μm, resolved with an electrical lateral resolution of 60 nm [see Fig. 4(c)]. The topography image shows the poly-silicon gate and the field oxide, with a flat active region that includes the charge carriers. Fig. 4 shows that, at appropriate bias, the *dC/dV* images are almost exclusively sensitive either to electrons (n-type areas) or holes (p-type areas). The *dC/dV* images are shown at steps from -0.3 V up to 2 V tip bias. From the images we see how the doped regions within the active region react differently to the voltage bias, depending on their p or n dopant polarity. When the bias voltage is increased to larger positive voltages, the p-body (blue region) gets depleted and shrinks with almost no contrast at 1.75 V and 2 V anymore. The n$+$-source (red region on the right side) follows an opposite behavior with respect to the applied bias, and the signal can be observed only at 1.75 V and 2 V. Such a tip voltage induced migration of charge carriers has been also investigated in previous SMM studies and is in line with standard MOS semiconductor theory [26]–[29]. Depending on the dopant polarity and bias voltage, the charge carriers are either accumulated, partially depleted or completely depleted from the surface (inversion). The DC tip bias changes the width and the capacitance of the space charge region, affecting the *dC/dV* signal. The highest *dC/dV* signal can be measured in depletion, where the kHz signal can most effectively modulate the space charge capacitance. At small voltages (accumulation), holes from the p silicon are attracted to the surface, shrinking the width of the space charge region. Accordingly, the p-doped body shows the strongest *dC/dV* signal at 0.1–0.6 V. For strongly positive tip bias voltages, the holes are depleted from the surface and the width of the space charge region increases (inversion), resulting in a decreased *dC/dV* signal of the p-body at 1.75–2 V. The same mechanism, with opposite voltage dependence, holds for the n-type regions. The n$+$-type source shows the strongest *dC/dV* signal at 1.75–2 V because the free electrons accumulate closely to the surface, reducing the width of the space charge region. We observed a slight shift of the space charge region dynamics towards positive voltage values, mostly because of two contributions. Firstly, the work-function of the solid platinum tip influences the working voltage; secondly, the presence of oxide and surface charges influences the voltage dependence of the depletion capacitance [30]. This tip bias voltage dependence

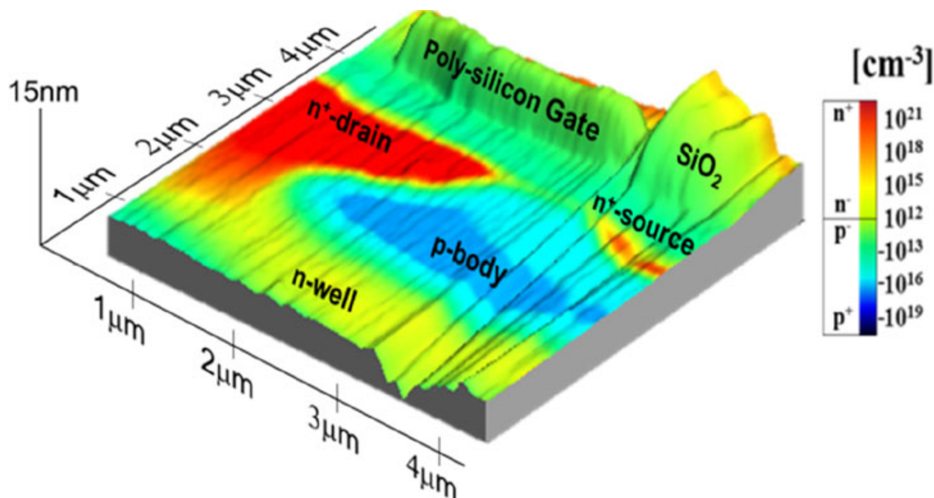

Fig. 6. 3D SMM dopant image obtained by combining the topography with the calibrated doping concentration of the transistor device. The superimposition allows having all the information in one image, highlighting both the differently doped p-type and n-type regions within the device and the topographical pattern.

of the space charge region's width and of the charge carriers is typically used to differentiate n-doped from p-doped areas in quantitative SMM imaging.

D. Quantitative Dopant Profiling

The *dC/dV* raw data were calibrated using a dopant profiling calibration sample (cf. Materials and Methods, [22]). A flat calibration sample with differently doped regions has been used [18], [24]. Fig. 5 shows the raw *dC/dV* image of the transistor and the raw image of the calibration sample, including both n-type and p-type regions with doping concentration in the range of 10^{15}–10^{20} atoms/cm^3. Again, the transistor image shows the n-channel LDMOS including the p-body, n+ source, n+ drain, poly-silicon gate, and field oxide regions. From the *dC/dV* calibration image, two calibration curves relating the p- and n- doping concentrations to the measured *dC/dV* values are derived. Using the calibration curves, the *dC/dV* image of the transistor has been converted into a 2D color map of the doping concentration [see Fig. 5(d)]. Note that the color-bar includes both p-type and n-type doping concentration values. What is shown in Fig. 5(d) is the numerical sum of the local (negative) electrons concentration and the local (positive) holes concentration. The information on the individual carrier concentration in the transition region between the n- and p-type areas is still available in the original SMM p-type and n-type carrier maps of the device, measured at the corresponding tip-bias voltages. The SMM doping concentration values have been compared to a TCAD model that was specifically defined to reflect the drain/drift region and the body/source area of the transistor with a channel length of 0.5 μm. Fig. 5(e) shows the modelling results in the area of interest, thus the p- substrate located below the deep n-well is not included. A quantitative agreement between model and experiments has been obtained on most of the transistor regions within the SMM accuracy of 20% for doping profiling [22]. The only area that shows a larger difference is the n-drain, where the doping concentration values measured with SMM are higher than the modelled ones. This can be attributed to the presence of trapped charges in the native oxide and surface charges, which alter the measured *dC/dV* signal and thus the doping concentration values. Fig. 6 shows a superposition of the topography image with the doping concentration 2D color-map. The superimposition helps locating the active doped regions within the device by showing their positions with respect to the topographical features such as the poly-silicon gate. Moreover, it shows that the calibrated doping concentration image generated from the *dC/dV* image has no unspecific crosstalk influence from the topography.

IV. Conclusions

The 2D doping concentration map of a n-channel LDMOS transistor in CMOS HV technology has been obtained at 20 GHz frequency using *dC/dV* SMM. Key device features such as n-source, p-body, and n-drain with a minimum feature size of 350 nm have been resolved and quantitatively measured with an electrical SMM lateral resolution of 60 nm. This suggests that SMM's electrical sensitivity and lateral resolution can be exploited to characterize nanoscale features within real electronic devices. The calibrated SMM doping images showed values of 10^{15} to 10^{19} atoms/cm^3, and they have been compared with the doping concentration map from TCAD simulations. The *dC/dV* experiments revealed the shape of the pn junction formed at the p-body/n-well interface, which is in accordance to TCAD modelling. *dC/dV* experiments at different DC tip bias allow further characterization of the differently doped regions including the p-body and n-source. As such the doping polarity can be investigated on top of quantitative doping concentrations. From S_{11} measurements, a calibrated capacitance image of the transistor device has been obtained. The capacitance of the poly-silicon gate, n-well, and the flat diffused pn junction formed at the p-substrate/n-well interface has been quantified with values in the range of 300 aF to 1fF. Our results suggest that both doping profiling and calibrated capacitance imaging capabilities

of SMM should be leveraged for a comprehensive electrical nanoscale analysis of a semiconductor structure.

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