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PHYSICS OF SEMICONDUCTOR DEVICES

Analysis of the Features of Hot-Carrier Degradation in FinFETs

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Abstract—For the first time, hot-carrier degradation (HCD) is simulated in non-planar field-effect transistors with a fin-shaped channel (FinFETs). For this purpose, a physical model considering single-carrier and multiple-carrier silicon—hydrogen bond breaking processes and their superpositions is used. To calculate the bond-dissociation rate, carrier energy distribution functions are used, which are determined by solving the Boltzmann transport equation. A HCD analysis shows that degradation is localized in the channel region adjacent to the transistor drain in the top channel-wall region. Good agreement between the experimental and calculated degradation characteristics is achieved with the same model parameters which were used for HCD reproduction in planar short-channel transistors and high-power semiconductor devices.

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1. INTRODUCTION

Miniaturization of the basic element of modern microelectronics, i.e., the field-effect transistor (FET), implies not only a decrease in the linear sizes of devices and gate-insulator thicknesses, but also optimization of the power consumption and maintenance of the proper electrostatic control of the channel [1]. In this case, the physical problems to be solved are an increase in the subthreshold slope and a decrease in the OFF current. By the time of the formulation of these requirements, the potential for the optimization of transistors of "conventional" planar architecture had been exhausted, which resulted in the appearance of devices of new three-dimensional topologies, such as multigate structures (multigate FETs, MGFETs), transistors with a fin-shaped channel (FinFETs), and nanowire FETs (NWFETs) [2, 3]. Among these devices, the FinFET [4, 5] is the most promising.

The most important criterion of the "vitality" of each technological generation, along with operation characteristics and power consumption, is the device reliability. FET reliability assurance implies a struggle against a variety of parasitic effects. As applied to FinFETs, it was recently shown that the main mechanism of dielectric/semiconductor system damage is hot carrier degradation (HCD) [5].

In the last few years, the HCD effect in FinFETs has been the object of intense experimental [6–8] and theoretical [9, 10] studies; however, the nature of this effect is still not completely understood, and a reliable predictive model based on physical principles has not yet been proposed. Attempts to simulate HCD in devices of this type were primarily based on empirical and phenomenological simplifications. They were reduced to estimating the device lifetime under the real condition of hot-carrier stress by extrapolating the data obtained at higher stress voltages. However, as experience shows [11–13], the change of conditions entails a change in the main microscopic mechanism responsible for HCD, which makes inconsistent the mentioned device-lifetime extrapolation.

A small number of models, within which descriptions of physical mechanisms responsible for HCD were proposed, used the impact-ionization rate as a quantitative criterion of the transistor damage due to hot carrier stress (see, e.g., [9]).

Such an approach seems controversial, since defect generation during HCD is associated with silicon—hydrogen (Si—H) bond breaking at the insulator—silicon interface, and the rate of this process exhibits a completely different dependence on the particle energy than the impact ionization rate. Furthermore, within such approaches it is supposed that the impact-ionization rate is a function of the electric field. However, we previously showed that the Si—H bond breaking rate (and, hence, the concentration of interface states N_{it}) follow the electric-field variation with a significant delay [14, 15]. Finally, the device operating voltage in modern transistors is often below 1 V, i.e.,

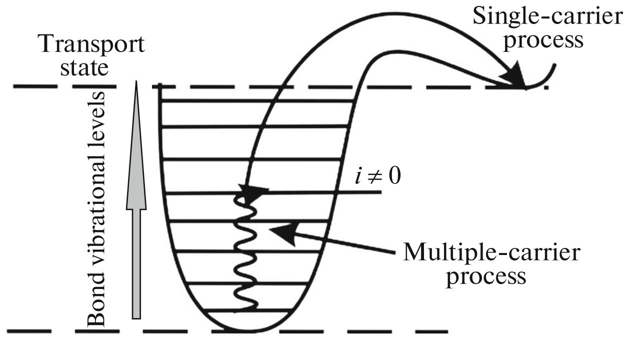

Fig. 1. Schematic of single-carrier and multiple-carrier Si–H-bond-dissociation mechanisms.

the impact-ionization rate is negligible and cannot be used to simulate HCD.

To describe HCD in FinFETs, in this study we use a physical model based on the modeling of carrier transport in semiconductor structures.

2. MODEL OF HOT-CARRIER DEGRADATION

HCD features were simulated and analyzed using the methodology we developed previously [16–19] and employed to describe device damage by hot carriers in short-channel transistors and high-power semiconductor devices (lateral double-diffused MOS–LDMOS–transistors) [20, 21]. This model can be conditionally divided into three basic blocks: carrier transport simulation in a semiconductor structure; description of the microscopic mechanisms of defect generation at the silicon–silicon dioxide (SiO_2/Si) interface; simulation of the characteristics of the damaged devices.

Carrier transport was described using the ViennaSHE simulator performing a deterministic solution (in contrast to stochastic approaches based on the Monte Carlo method) of the Boltzmann transport equation [22, 23]. Calculations are performed taking into account the real band structure of Si and different scattering mechanisms, i.e., scattering at ionized impurities, scattering at the interface, impact ionization, and electron–phonon and electron–electron interactions.

With ViennaSHE we calculated carrier energy distribution functions (DFs) for a given device architecture and stress conditions. The DFs are then used to calculate the Si–H bond breaking rates. Within the model, two bond breaking mechanisms are considered, i.e., the single- and multiple-particle processes. The former mechanism corresponds to classical HCD where a carrier ensemble contains a significant number of hot carriers with energies of $E > E_a$ (where E_a = 2.6 eV is the Si–H bond-breaking energy [24]). The latter mechanism is typical of low stress voltages, when bond dissociation is provoked by the cascade effect of cold carriers inducing multiple-carrier excitation of vibrational modes [11, 17, 18, 25–27]. Our model accounts for all superpositions of these two mechanisms.

We have shown [18, 21, 23] that the most efficient bond-degradation process is the scenario according to which the Si–H bond is initially excited by a series of cold particles to a certain intermediate bound state (with a required breaking energy lower than nominal E_a) and then it is broken by a sole hot carrier (with $E < E_a$, see Fig. 1).

We recall that the bond-dissociation rate according to the single-carrier mechanism is written as [17, 28]

$$I(E_a) = \int f(E)\rho(E)\sigma(E, E_a)v(E)dE + I_{\text{th}}, \quad (1)$$

where $f(E)\rho(E)$ is the generalized DF (the product of the occupancy factor f and the density of states ρ, the dimension is $\text{eV}^{-1}\,\text{cm}^{-3}$), $\sigma(E, E_a)$ is the energy-dependent cross section of the bond-breaking reaction with the corresponding activation energy E_a, and $v(E)$ is the group velocity of particles. Integration in Eq. (1) is performed over all energies of particles in the ensemble. The term I_{th} describes the thermal activation of the H atom through the barrier separating the bound and transport states.

If the multiple-carrier excitation of a bond to the level i (with the energy E_i) is taken into account, the potential barrier between this level and the transport mode is decreased by E_i, and the corresponding rate is calculated as

$$\begin{aligned} I_i(E_a) &= \int f(E)\rho(E)\sigma(E - E_i)v(E)dE \\ &+ \omega_{\text{th}} \exp\left(-\frac{E - E_i}{kT}\right), \end{aligned} \quad (2)$$

where ω_{th} is the "attempt frequency" of thermal breakage, k is the Boltzmann constant, and T is the lattice temperature. Then the cumulative bond-breaking rate is determined as the sum of contributions of individual levels, i.e., $I(E_a) = \Sigma I_i(E_a)$.

For both single- and multiple-particle mechanisms, the scattering cross sections are simulated by the Keldysh expression

$$\sigma^{\text{SP|MP}}(E, E_a) = \sigma_0^{\text{SP|MP}} \left(\frac{E - E_{\text{th}}}{1\ \text{eV}}\right)^{p^{\text{SP|MP}}} \quad (3)$$

with the parameters $\sigma_0^{\text{SP|MP}}$ and $p^{\text{SP|MP}}$ ($p^{\text{SP}} = 12$ and $p^{\text{MP}} = 1$); the superscripts "SF" and "MP" denote the single-particle and multiple-particle processes, respectively. For the single-carrier process, $E_{\text{th}} = E_a$; for the multiple-carrier process, E_{th} corresponds to the distance between oscillator levels (see Fig. 1).

Within the model, we believe [18] that bond dissociation occurs via the stretching mode; generally speaking, the bond has a second vibrational mode, the bending mode, which, however, is unrelated to its dissociation [24]. We also suppose that the activation

energy is a statistically fluctuating quantity described by the normal distribution with the mean value of E_a = 2.6 eV [24] and the standard deviation of σ_E = 0.22 eV. The quantity σ_E is one of two model fitting parameters along with the passive bond Si–H concentration at the interface ($N_0 = 5.6 \times 10^{12}$ cm^{-2}).

Both parameters depend on a specific technological process but are identical for transistors fabricated under identical conditions. Other parameters are fixed: e.g., we use $\sigma_0^{SP} = 5 \times 10^{-18}$ cm^2 and $\sigma_0^{MP} = 5 \times 10^{-19}$ cm^2, i.e., the same values as used for simulating HCD in planar transistors [18].

The calculated defect-generation rates are further used to calculate the coordinate-dependent interface state density N_{it} for each stress time step. The obtained densities are then used in the MiniMOS-NT simulator program [29] which computes device parameter variations with time. In this case, both local electrostatic perturbations associated with the presence of traps and a decrease in the charge-carrier mobility due to the appearance of additional scattering centers are taken into account.

3. DEVICES AND EXPERIMENTAL

To study the device degradation under the condition of hot carrier stress, we used FinFETs with a trapezoidal cross section (see Fig. 2). The gate electrode length in these devices is 40 nm, and the channel length is 28 nm; the operating and threshold voltages were V_{DD} = 0.9 V and $V_{\text{th}} \approx 0.4$ V, respectively. The high-k gate stack includes two components: silicon dioxide (SiO_2) and hafnium dioxide (HfO_2) films. The equivalent oxide thickness (EOT) of the resulting layer is 1.2 nm. The devices were fabricated according to the conventional technological process at *imec* (see [30]).

Transistors were subjected to hot carrier stress at voltages corresponding to the worst-case conditions of HCD, i.e., at $V_{gs} \approx V_{ds}$ (where V_{ds}, V_{gs} are the drain–source and gate–source voltages) [12, 13, 31], and room temperature. We note that we independently chose the values of V_{ds}, while V_{gs} values were adjusted so that to provide $V_{gs} - V_{\text{th}} = V_{ds}$. Finally, the following bias combinations were used: V_{ds} = 1.6 V, V_{gs} = 1.7 V; V_{ds} = 1.7 V, V_{gs} = 1.8 V; V_{ds} = 1.8 V, V_{gs} = 1.9 V. As a quantitative characteristic (metric) of HCD, we monitored the relative change in the linear drain current $\Delta I_{d,\text{lin}}(t) = [I_{d,\text{lin}}(t) - I_{d,\text{lin}0}]/I_{d,\text{lin}0}$, where t is the degradation time, $I_{d,\text{lin}0}$ is the drain current of an undamaged FET, which corresponds to V_{ds} = 0.05 V and V_{gs} = 0.9 V.

Preliminarily, we studied the question whether we deal exclusively with degradation due to interface-state generation or the contribution associated with trap charging/recharging in the insulating layer bulk should also be taken into account. These mechanisms are related to the recoverable component of the damage. This recoverable component was a subject of extensive studies performed using transistors from the same technological node [30] over a wide range of stress/recovery conditions. It was found that a recovery after degradation does not occur for a sufficiently long time interval, hence, it can be argued that HCD in the samples under study consists only in defect generation by Si–H bond breaking.

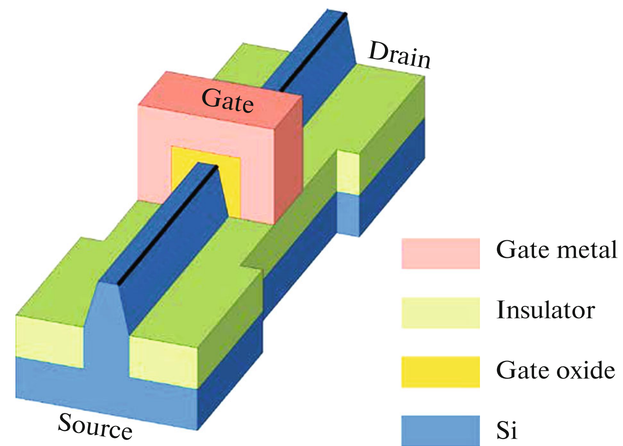

Fig. 2. (Color online) Schematic image of the FinFET under study. The channel cross section is trapezoid-shaped.

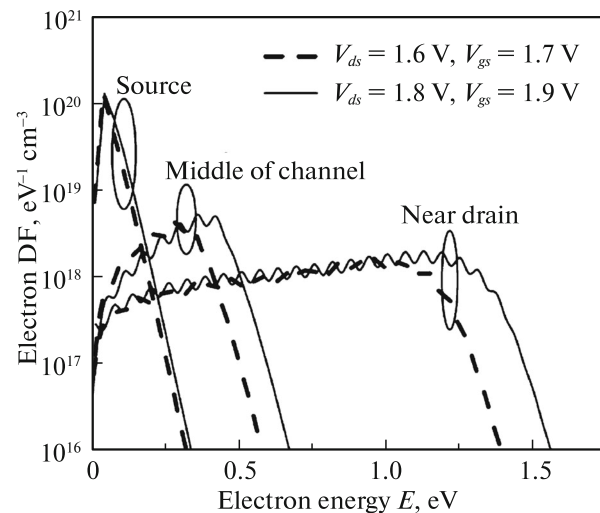

Fig. 3. Electron energy distribution function (DF) calculated using a ViennaSHE simulator program for V_{ds} = 1.6 V, V_{gs} = 1.7 V and V_{ds} = 1.8 V, V_{gs} = 1.9 V. The DFs were derived for the edge between the upper channel plane and its side wall in the source region, at the device center, and in the drain region.

4. RESULTS AND DISCUSSION

Figure 3 shows a set of generalized electron energy distribution functions calculated for two stress voltage combinations, namely, V_{ds} = 1.6 V, V_{gs} = 1.7 V and V_{ds} = 1.8 V, V_{gs} = 1.9 V. The DFs were calculated for

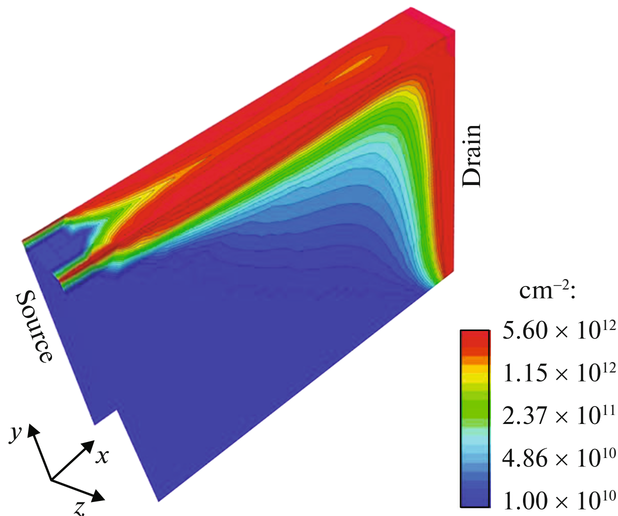

Fig. 4. (Color online) Density profiles of trap states at the channel–insulator interface, $N_{it}(x, y, z)$, for V_{ds} = 1.7 V, V_{gs} = 1.8 V, and $t \approx 200$ s. We can see that the most damaged device region corresponds to the upper part of the near-drain side of the channel.

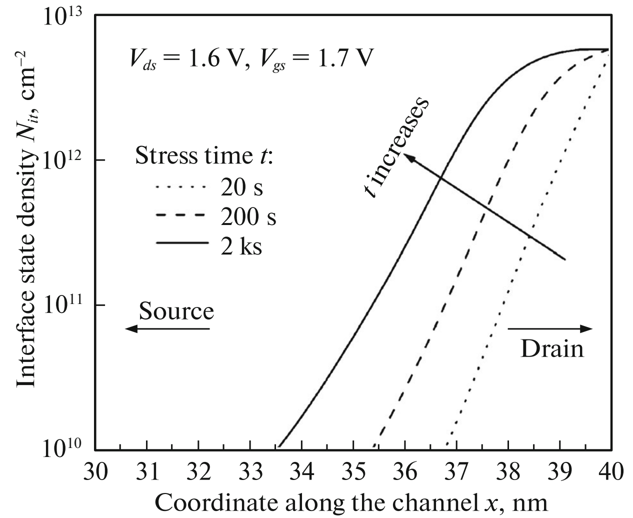

Fig. 5. Time evolution of profiles $N_{it}(x)$ for V_{ds} = 1.6 V and V_{gs} = 1. 7 V. The data is for the edge between the upper channel plane and its side wall.

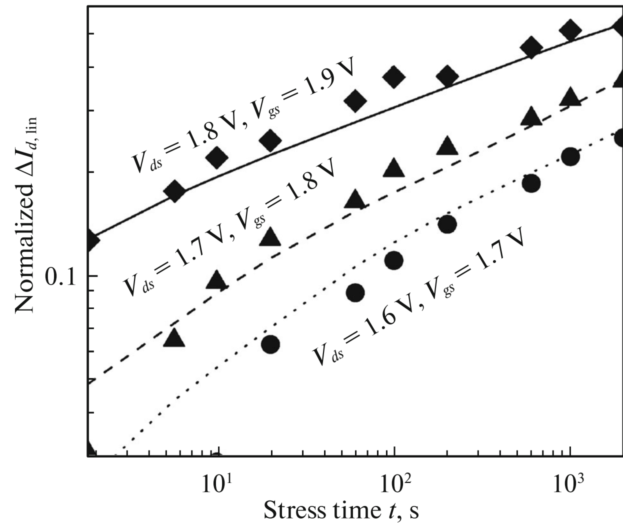

Fig. 6. Comparison of experimental and calculated characteristics $\Delta I_{d,\,\mathrm{lin}}(t)$.

the edge between the upper channel boundary and its side wall (bold line in Fig. 2), for three lateral positions (the drain–source direction denoted by the x axis, see Fig. 2) in the source region, at the channel center, and in the drain region (Fig. 2). We can see that thermalized electrons in the source region are described by a Maxwellian distribution while in the channel center and in the drain region, these functions are strongly nonequilibrium.

The profiles of the trap density, calculated for V_{ds} = 1.7 V, V_{gs} = 1.8 V, and the stress time $t \approx 200$ s are shown in Fig. 4. These profiles $N_{it}(x, y, z)$ allow the conclusion that degradation is localized in the upper region of the channel side adjacent to the drain. Furthermore, we can see that N_{it} increases for any lateral position x toward the channel top (in the direction of increasing coordinate y). Such a behavior is caused by the appreciable vertical field component and carrier heating not only in the source–drain direction, but also along the y axis. Figure 5 shows the evolution of the density N_{it} with time for softer stress conditions, V_{ds} = 1.6 V, V_{gs} = 1.7 V (like the DF in Fig. 3, the N_{it} profiles were simulated for the edge between the top and side wall of the channel). We can see that the drain region is most damaged, which appears, e.g., in HCD saturation under long stresses (t = 200 s and 2 ks), and the time dependence of HCD is defined by the N_{it}-front propagation toward the drain.

Finally, Fig. 6 shows that the model is capable of reproducing the experimental dependences $\Delta I_{d,\,\mathrm{lin}}(t)$ with good accuracy for all stress voltage combinations. The fact that the parameters used to simulate changes in FinFET characteristics are almost identical to those used to describe HCD in planar transistors with a channel length of 65 nm and in high-voltage LDMOS devices with a channel length of ~1.0 μm, is very important. This evidences for the universality of our model and allows us to conclude that it can be used to predict the lifetime of various devices at operating voltages.

5. CONCLUSIONS

In this study, the physical model for hot-carrier degradation was used for the first time to analyze features of this parasitic effect in field-effect transistors with a fin-shaped channel (FinFETs). The model is based on the analysis of carrier transport in semiconductor structures and considers the interaction of single-carrier and multiple-carrier mechanisms of sili-

con–hydrogen bond rupture. This ensures that our model can accurately capture HCD over a wide range of stress voltages starting at severe conditions with high V_{ds}, V_{gs} and ending at mild stresses and/or operating conditions.

It was revealed for the first time, where exactly the damage caused by hot carriers is localized: this is the upper channel region adjacent to the drain. Another detected HCD feature in FinFETs is an increase in the defect density upon approaching the upper channel edge. This is due to the vertical component of the electric field which accelerates carriers not only in the source–drain direction, but also in the direction from the bottom of the channel to its upper edge.

It is important that the set of parameters is almost identical to the values previously used to simulate HCD in planar short-channel transistors and in high-power devices. This circumstance allows us to conclude that our model is universal and predictive.

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