Understanding BTI in SiC MOSFETs and Its Impact on Circuit Operation

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***Abstract*—The threshold voltage hysteresis in SiC power MOSFETs is rarely studied. This paper investigates the capture- and emission-time constants of positive and negative charge trapped in the gate oxide and at the interface as a function of gate bias. We present a measurement technique which enables time-resolved measurement of the real V_{th} during application-relevant bipolar ac high temperature gate stress. In addition, we use capture and emission time maps to explain the temperature dependence of ΔV_{th} after stress and are able to simulate ΔV_{th} after positive ac stress considering the full stress-history. Furthermore, we will show that the threshold voltage hysteresis has no harmful impact on switching operation in real applications.**

***Index Terms*—BTI, CET, hysteresis, SiC, threshold voltage.**

I. Introduction

DUE TO the higher breakdown field of SiC compared to Si, high voltage power MOSFETs made of SiC have shorter drift zones than those made of Si with the same on-resistance R_{on} and voltage class. Therefore, the area can be reduced allowing SiC MOSFETs with 100 times lower gate-source and gate-drain capacitances [1], [2]. Switching losses as well as losses caused by gate driving for SiC are much smaller than those of their Si counterpart [3]. On the other hand, short-term as well as long term ΔV_{th} in SiC-MOSFETs under positive and negative gate bias stress are significantly higher, though recovering faster, than the ones observed in Si-MOSFETs [4]–[6]. This is observed in commercially available SiC-MOSFETs from various manufacturers [7], [8].

There are major differences to the well-known threshold voltage drifts in Si-MOSFETs, especially the well-investigated negative bias temperature instability (NBTI) effect in pMOSFETs. ΔV_{th} in SiC-MOSFETs recovers fast and goes in both directions from typically $+1$ V to -3 V, due to capture of both negative and positive charges in the gate oxide and interface [9]. In this paper, we compare parameters extracted from positive and negative DC stress tests as well as application-relevant AC stress under consideration of the measurement delay. Our measurement technique, being a measure-stress-measure (MSM) technique, provides quasi-instantaneous readouts of V_{th} with a 1 μs measurement delay (see Section II). This fast readout enables us for the first time to determine capture and emission time constants for positive and negative trapped charges as a function of the applied gate bias and temperature.

In Section III, in addition to our previous publication [10], we apply and verify the concept of capture and emission time (CET) maps for SiC and are able to explain the surprising temperature dependence of ΔV_{th} after stress. In Section IV, we will show measurements of the threshold voltage hysteresis at a typical 50 kHz bipolar rectangular AC gate signal and demonstrate that the measured threshold voltage hysteresis is fully recoverable. One of the goals of this paper is to show the necessity to improve the standard tests as developed for silicon (e.g., JEDEC) for SiC and to discuss the impact of the threshold voltage hysteresis on the switching behavior. We present in Section V time resolved R_{on} measurements during AC gate stress. Moreover, in Section VI, we will demonstrate the first successful model of the threshold voltage shift after long-term positive AC stress by the use of CET maps.

II. Measurement Setup

The samples used in this study were packaged SiC trench MOSFETs with a rated $V_{ds,max}$ of 1200 V and a $V_{gs,max}$ of $+20/-10$ V. ΔV_{th} after DC gate bias stress as well as during bipolar AC stress were measured using our ultra-fast measurement technique [11] with a measurement delay (the time between interruption of stress and the settling time of the V_{th}-readout) of 1 μs. The resolution in the stress-timing as well as the width of the shortest rectangular stress pulses we can apply is 100 ns. The resulting accuracy in the stress timing (also for the AC signals) is about $\pm$ 20 ns. These accuracy limits are mainly determined by the high gate capacitance of $\approx$2 nF, the length of the test leads of several cm, together with an imperfect impedance matching. Thus, our accuracy and lower limit in determining the short time constants of the V_{th}-transients under positive or negative gate stress is about $\pm$20 ns. Before each stress measurement, the initial V_{th} is recorded. All measurements are performed with a well-defined stress history,

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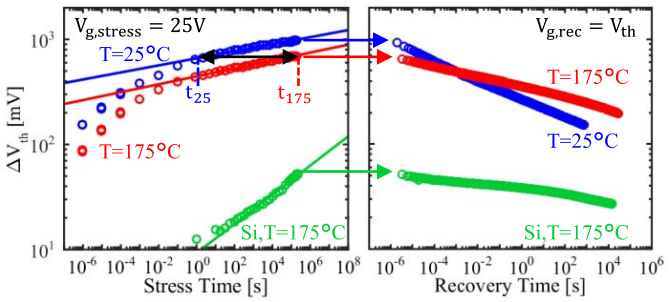

Fig. 1. **Left:** Comparison of SiC and Si-MOSFETs with the same t_{ox} and E_{ox} during positive gate bias stress with 1 µs measurement delay. SiC shows higher but fast recovering ΔV_{th} with a reversed temperature dependence compared to Si: ΔV_{th} at lower temperatures (T = 25°C) is larger than at higher temperatures (T = 175°C). Lines correspond to power-law fits with stress time. **Right:** Recovery after 200 ks stress with the same stress voltage. Recovery at lower temperatures is faster than at higher temperatures. A crossing of the measured ΔV_{th} is observed at 5 ms.

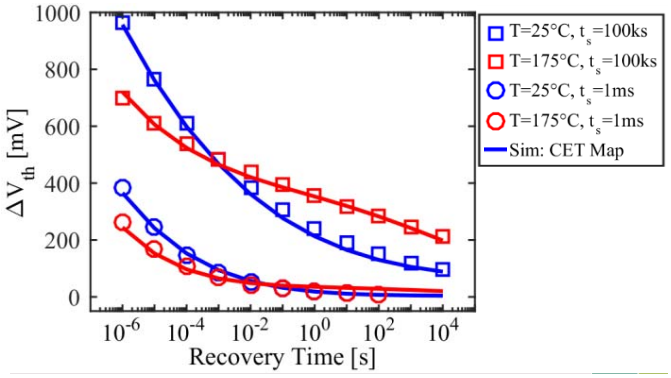

Fig. 2. Two exemplary ΔV_{th} recovery traces from Fig. 1 at T = 25°C (blue) and T = 175°C for two different stress times t_s = 1ms and t_s = 100ks. Symbols are experimental data. The solid lines show the fits for each temperature obtained by the analytic activation energy map shown in Fig. 3.temperature-independent constants, $\tau_{0,r}$ for the recoverable and $\tau_{0,p}$ for the more permanent defects.

e.g., 50 kHz AC stress for a given number of periods, and ending at, e.g., exactly 20% of a period and without voltage ramps to measure IV-curves (see Fig. 10). Therefore measurement comparability is guaranteed and the measurements are perfectly reproducible. Stress and measurement temperatures range from 25°C to 175°C.

III. DC Measurement Results

We compare the ΔV_{th} of SiC-MOSFETs after positive gate bias stress with the ΔV_{th} of Si-MOSFETs with the same gate oxide thickness t_{ox} and same oxide field E_{ox} (see Fig. 1). Si-MOSFETs show generally a lower ΔV_{th} due to a lower trap density compared to SiC. SiC-MOSFETs show a higher, but fast degrading and fast recovering ΔV_{th}. Already after 1 ms stress, we observe in Fig. 1 on the left a fast increase of the ΔV_{th}, the fast recovery within milliseconds after this stress is shown in Fig. 2. This increase and decrease of ΔV_{th} within milliseconds (in the following called fast component) is not detected in other SiC-MOSFET publications. Furthermore, we observe a peculiarity that is only visible at short measurement delays.

The measured ΔV_{th} at lower temperatures is higher than at high temperatures. For Si, it is already well established that threshold voltage shifts due to BTI can be understood as the collective response of an ensemble of independent defects [12], [13]. In addition the CET maps contain the required information about the kinetics of charge capture and emission [13]. In the following we will demonstrate that charge exchange and the correlated activation energies can be described consistently with previous work for both Si and SiC as two bivariate Gaussian distributions [13]: one for the defects having short capture and emission times and one for the charged defects having emission times mostly permanent in typical experimental time windows. The main parameters of the analytic model are the mean value μ_c and $\mu_{\Delta e}$ of the capture and emission activation energies $E_{a,c}$ and $E_{a,e}$ with their standard deviations σ_c and $\sigma_{\Delta e}$. Furthermore, the emission activation energies $E_{a,e}$ increase with larger capture activation energies $E_{a,c}$: $E_{a,e} = E_{a,c} + \Delta E_{a,e}$. The correlation between the standard deviations $\sigma_e^2 = r \cdot \sigma_c^2 + \sigma_{\Delta e}^2$ as explained in [14] is used, with the correlation parameter $r = 1$ for the recoverable component and $r = 0$ for the more permanent component. Thus the charged trap density $g(E_c, E_e)$. for each component is given by

$$g(E_c, E_e) = \frac{1}{2\pi\sigma_c\sigma_{\Delta e}} \times \exp\left(-\frac{(E_c - \mu_c)^2}{2\sigma_c^2} - \frac{(E_e - (rE_c + \mu_{\Delta e}))^2}{2\sigma_{\Delta e}^2}\right). \quad (1)$$

The threshold voltage shift, for a given stress- and a given recovery-time, is obtained from the activation energy map by integrating over all defects being charged up to the stress time and not yet being discharged at the recovery time. For Si, it has been shown that the temperature activation of a single trap follows the Arrhenius law with $E_{a(c,e)}$ the activation energy for capture and emission [15]:

$$E_{a(c,e)} = k_B T \cdot \ln\left(\frac{\tau}{\tau_0}\right) \quad (2)$$

where τ_0 denotes the time constant for infinite temperature. Following (2), the temperature dependence of the capture and emission time constants can be described as:

$$\tau_2 = \tau_o \cdot \left(\frac{\tau_1}{\tau_0}\right)^{\frac{T1}{T2}} \quad (3)$$

with τ_1 the capture/emission time constant at temperature T_1, τ_2 the transformed capture/emission time constant at temperature T_2.

The activation energy map is therefore a temperature-independent map and the capture and emission time maps at constant temperature can be calculated from the activation energy map using (2) with the two characteristic constants $\tau_{0,r}$ and $\tau_{0,p}$.

To analyze the physical nature of the defects responsible for the positive as well as the negative ΔV_{th}, spectroscopy on individual defects like for NBTI in Si devices would be mandatory [16]. Presently such measurements are not yet

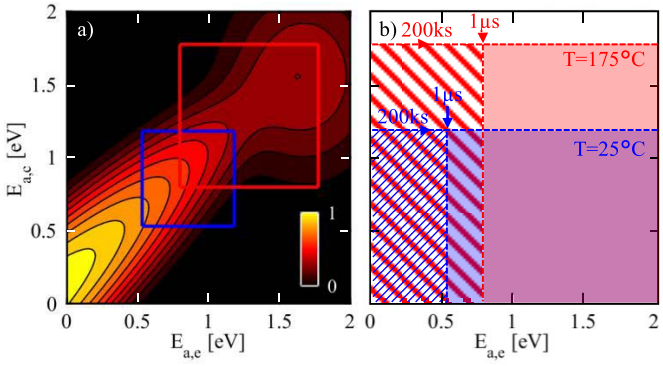

Fig. 3. **a):** Analytic activation energy map obtained with stress and recovery data like the ones shown in Fig. 2 with recovery traces for stress-times from 1 µs up to 200 ks. The charged trap density g is shown in dependence of the capture and emission activation energies and is normalized to 1 using $\log_{10}(1+\kappa\cdot\max(g))/\log_{10}(1+\kappa)$ with $\kappa = 100$ to emphasize all details [13]. The measurement range from 1µs to 200ks is marked in blue for T = 25°C and in red for T = 175°C. **b)** Charge trap occupation map shown for the DC stress at T = 25°C and T = 175°C. The blue and red filled rectangle mark the traps that are occupied for a stress time of 200ks and a measurement delay of 1 µs. The blue and red patterned areas indicate the region of the activation energy map that is out of the measurement range at T = 25°C and T = 175°C, respectively. The region where the red patterned and the solid blue area overlap marks the traps which are within the measurement range at T = 25°C but already recovered at T = 175°C.

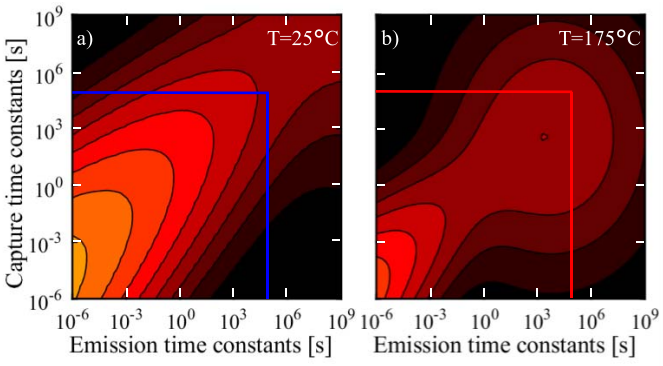

Fig. 4. Same map as Fig. 3 shown as a function of the capture and emission time constants at a) T = 25°C and b) T = 175°C. Fitting the data we obtain the two characteristic temperature-independent constants $\tau_{0,r} = \tau_{0,p} = 10^{-15}$s.

TABLE I
PARAMETERS USED FOR THE ANALYTIC ACTIVATION ENERGY MAP OF FIG. 3 AND THE CAPTURE AND EMISSION TIME MAPS IN FIG. 4

	μ_c (eV)	σ_c (eV)	$\mu_{\Delta e}$ (eV)	$\sigma_{\Delta e}$ (eV)	A (V)	τ_0 (s)
r	-0.47	0.55	-0.19	0.20	0.8	10^{-15}
p	1.53	0.36	1.64	0.35	1.09	10^{-15}

available, thus we refrain from speculations on the physical origin of these effects. Independent of the physical nature, commonly accepted facts are:

- Under positive gate bias, there is capture or trapping of negative charge in the oxide or interface leading to a positive ΔV_{th}. This effect is accelerated with increasing gate voltage and referred to as positive bias temperature instability (PBTI).
- Under negative gate bias, there is capture or trapping of positive charge in the oxide or interface leading to a negative ΔV_{th}. This effect is accelerated with decreasing gate voltage and referred to as negative bias temperature instability (NBTI).
- Recovery after both positive and negative gate bias stress occurs when the stress is removed. This recovery is accelerated when the voltage is switched into the direction opposite to the stress voltage.

In the following, we will present CET maps modeling the ΔV_{th} after positive gate bias stress. We fit the measurement data (examples shown in Fig. 2 with all recovery measurements of stress times from 1 µs up to 200 ks at T = 25°C and T = 175°C) by optimizing all parameters of the activation energy map in Table I. The activation energy map is shown in Fig. 3 a), the corresponding capture and emission time maps at T = 25°C and T = 175°C are shown in Fig. 4.

The measurement windows of the DC measurements are indicated in Fig. 3a) with the blue (T = 25°C) and red (T = 175°C) rectangles. We observe for SiC that many traps have very short capture and emission time constants also well below 1 µs. These are modeled with the charged trap density for the recoverable defects described in (1) with the correlation parameter $r = 1$. The fast increase of ΔV_{th} after short stress times (see Fig. 1a) is as well due to the many defects with short capture time constants. Since the traps with short capture time constants ($\tau_c < 1$ ms) have also short emission time constants ($\tau_e \ll 1$ ms), the increase of V_{th} vanishes as quickly as it appears within milliseconds (see Fig. 1, right). Due to the thermal activation, emission time constants of traps around 1 µs at T = 25°C decrease with increasing temperature and become shorter than the measurement delay at T = 175°C. The charged trap occupation map for a stress time of 200 ks and a measurement delay of 1 µs is shown in Fig. 3 b). The blue and red patterned areas indicate the region of the activation energy map that is out of the measurement range at T = 25°C and T = 175°C, respectively.

The area where the red patterned and the solid blue rectangle overlap marks the traps having emission times longer than the measurement delay (=recovery time) at T = 25°C, but having emission times shorter than the measurement delay at T = 175°C. Therefore the measured ΔV_{th} for short recovery times at T = 25°C (corresponding to the blue solid area in Fig. 3 b) is higher than at T = 175°C. A higher ΔV_{th} at lower temperatures has not been observed for Si, because there the defect density in the CET map increases from short to long capture time constants τ_c [17], [18]. For SiC, in contrast, the density of the recoverable component increases towards short time constants (see Fig. 3). Moreover, as seen in Fig. 1 on the right, the recovery at lower temperatures occurs faster than at higher temperatures. After 5ms recovery time, a crossing of the measured ΔV_{th} is observed.

This seemingly paradoxical dependence of ΔV_{th} on the recovery time and temperature can be well understood with the CET maps as demonstrated in Fig. 2. At T = 25°C traps with short capture as well as emission time constants contribute to ΔV_{th}, recovery of ΔV_{th} occurs therefore very quickly.

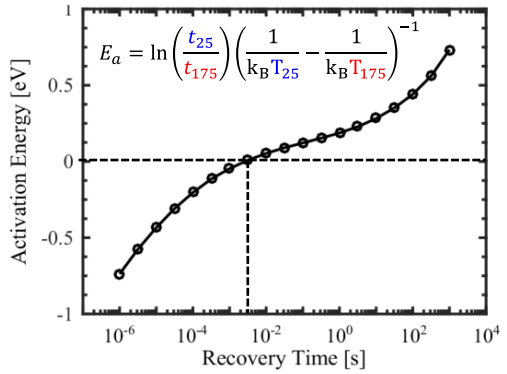

Fig. 5. Extracted apparent activation energy for the capture time constants as a function of the recovery times (=measurement delay) calculated with t_{25} and t_{175} (see example (double arrow) in Fig. 1 for a delay of 1 µs). Due to the different recovery slopes, the extracted apparent activation energy depends strongly on the measurement delay.

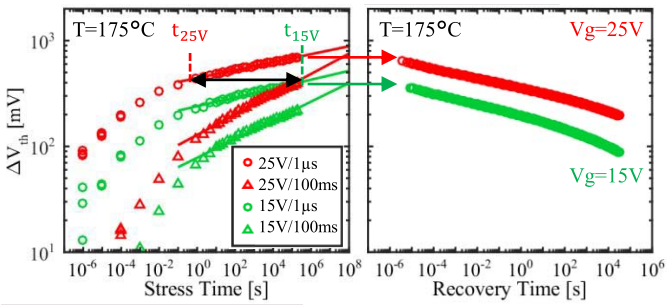

Fig. 6. **Left:** Comparison of the ΔV_{th} as a function of stress time at two different voltages with two different measurement delays (1 µs and 100 ms at T = 175°C). Labels in the legend denote stress voltage and measurement delay. The data is fitted with a power-law with the same exponent for both voltages. **Right:** Comparison of the recovery after 200 ks stress time. Within a few milliseconds the major part of the ΔV_{th} recovers, following a power law.

At T = 175°C also traps with longer emission time constants contribute to ΔV_{th}, therefore the recovery is slowed down compared to T = 25°C.

To Summarize: Charge capture due to gate stress is of course thermally activated, but recovery is even more thermally activated (note that all emission time constants in Fig. 3 and Fig. 4 are shorter than their corresponding capture time constants), so the remaining ΔV_{th} after a measurement delay <1 ms is less at high temperature than at low temperature. Measurements with standard measurement equipment and a measurement delay larger than 10 ms cannot resolve this temperature dependence and miss the change of ΔV_{th} caused by fast charging and de-charging traps.

The different measurement delays lead to a large unphysical dependence of the extracted apparent activation energy on the measurement delay (see Fig. 5). In particular for measurement delays shorter than 5 ms, a negative activation energy is extracted. For lifetime extrapolation, capture and emission time maps should be used in order to properly consider the recovery and avoid the artifacts caused by the measurement delay. As shown, the concept of a single activation energy is not valid, especially for traps with very fast recovering components [17]. A huge advantage of the CET maps is furthermore that ΔV_{th} after arbitrary gate stress can be simulated. Simulations and measurements of positive AC signals using the CET map shown in Fig. 3 will be presented in Section VI. Another recommendation is to cool down the sample with bias applied after high temperature stress. The ΔV_{th} should then be measured at room temperature with a measurement delay as short as possible.

This ensures that also for high stress temperatures the traps with low emission activation energies are within the measurement range, thus providing a comparability of all temperatures [19].

The comparison of ΔV_{th} at two different voltages shows a power law like dependence on stress time (see Fig. 6 on the left) for two different measurement delays (1 µs circles, 100 ms triangles). As observed for Si, ΔV_{th} increases with increasing stress voltage. For SiC devices the recovery is linear on a log-log scale (see Fig. 6 on the right), due to many traps with short emission times. Already after 100 ms for both stress voltages, half of the ΔV_{th} has vanished. In contrast to the SiC devices, the recovery after BTI for Si devices is approximately linear with the logarithm of recovery time. This is due to the broader distribution of the emission time constants of Si devices.

We conclude that with a higher stress voltage more traps are activated, but the distribution of the capture and emission time constants remains unchanged when increasing the stress voltage. A similar observation was made in [13] for Si, where the strong bias dependence of the individual traps did not directly translate into the distribution of time constants. The reason for this is that with different gate bias also the energetically available traps in the oxide changes [20].

To calculate the decrease of lifetime at accelerated stress conditions compared to use conditions, a voltage acceleration factor is commonly used. In Fig. 7 the voltage acceleration factor is shown for the longest stress time of the 15 V measurement (t_{15V}, green dashed line in Fig. 6 on the left) divided by the stress time needed to reach the same ΔV_{th} at 25 V (t_{25V}, red dashed line in Fig. 6 on the left). Due to the fast recovery after stress, the measurement delay also has a dramatic effect on the voltage acceleration factor, similar to the effect on the activation energy.

Dependent on the measurement delay, the extracted voltage acceleration factor differs by orders of magnitudes. Therefore, the parameters required for lifetime predictions, e.g., stress time dependence, measured apparent activation energies and voltage acceleration factor depend strongly on the measurement delay. Lifetime estimation according to the JEDEC [21] procedure allows a measurement delay of 48 hours which is clearly inappropriate for SiC. Furthermore, SiC-MOSFETs in switch-mode converters are operated with bipolar AC voltages or negative DC gate voltage, but positive long-term DC gate stress is never applied. Therefore we propose utilizing only gate bias stress occurring in the application and a shortest possible measurement delay (e.g., 1 µs).

To understand the impact of negative stress voltages during bipolar AC stress, we first analyze the threshold voltage after negative gate bias stress and its recovery (see Fig. 8). We

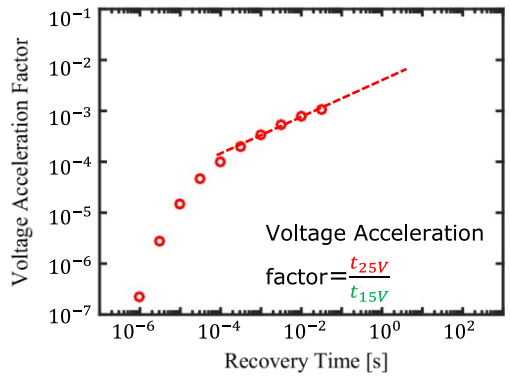

Fig. 7. The voltage acceleration factor taken at t_{stress} = 100 ks between 15/25 V (see arrows in Fig. 6) as a function of recovery time. The non-linear recovery leads to different voltage acceleration factors depending on the measurement delay, which hampers the extraction of lifetime models for SiC.

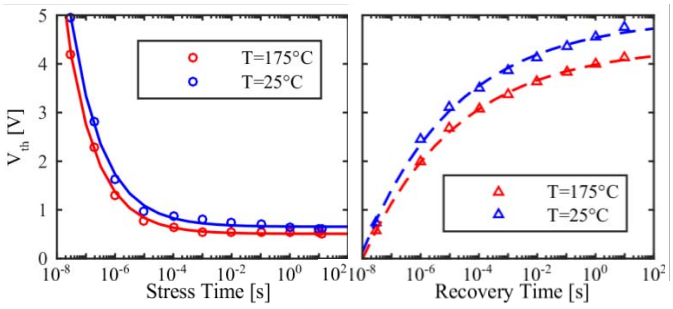

Fig. 8. Threshold voltage after negative stress and its recovery at (V_{gs} = −10V/0V) at T = 25°C and T = 175°C. Shown is on the left the saturation of V_{th} after stress at V_{gs} = −10V with increasing the stress time (circles,). The recovery to return to initial V_{th} at V_{gs} = 0V (triangles, right) takes longer than 10s of recovery.

observe a large and very fast negative ΔV_{th} under negative gate bias stress. Already after stress times of 10 µs the negative ΔV_{th} saturates. Obviously, the density of traps with capture time constants below 10 µs is very high. The emission time constants at V_{gs} = 0 V are broadly distributed and reach values up to 10 s (Fig. 8, on the right). Only a slight temperature dependence is observed for the negative gate stress. Due to the shorter capture and emission time constants at T = 175°C than at T = 25°C, the temperature difference is barely captured by a measurement delay of 1 µs.

We take a closer look at the time-constants of the recovery of V_{th}after negative stress back to the initial V_{th} shown in Fig. 9. At voltages above the operation voltage of 15 V, most of the negative ΔV_{th} disappears within ∼100 ns after switching V_{gs} back to positive bias. The recovery time exponentially depends on the gate voltage during recovery for both temperatures (see Fig. 9). This acceleration of the recovery is of utmost importance for the bipolar application and helps to switch the MOSFET faster.

The previously observed sub-threshold voltage hysteresis seen in the difference between IV-curve up-sweeps measurements and down-sweeps explained in [22] is caused by the negative gate stress. Due to the longer measurement delay (compared to our 1 µs), already the negative ΔV_{th} has recovered when measuring V_{th}. To further analyze the threshold

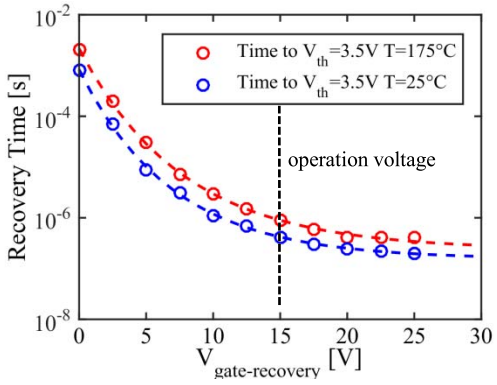

Fig. 9. Recovery from negative stress (V_{gs} = −10 V, t_s = 10 ms) at T = 25°C and T = 175°C. Shown is the required time at V_{gs} to recover V_{th} back to a value of 3.5V. The required time decreases exponentially with increasing recovery voltage (dashed lines), the charge emission at operation voltage occurs within 100 ns after switching to a positive V_{gs}.

voltage hysteresis, especially during bipolar AC stress, we have developed an advanced measurement technique, which provides additional information on the time-dynamics determined by the capture and emission time constants after bipolar AC stress.

IV. AC Measurement Results

In the next step, we study the threshold voltage hysteresis introduced by an application-like bipolar AC gate signal for different V_{high} and V_{low} combinations. We apply a frequency of 50 kHz, which is a typically recommended frequency for applications of SiC MOSFETs.

Furthermore, to measure the behavior of V_{th} in real-time during the AC stress, we interrupt the AC stress at different positions during the AC signal (see Fig. 10b). The full recovery back to the initial V_{th} (1 µs up to 10 ms) is shown in Fig. 10c) for each interruption of the AC gate signal. The measurement, keeping V_{gs} at V_{th} for 10 ms, disrupts the trap occupation state caused by the bipolar AC signal. To fully restore the pre-measurement trap occupation state before each interruption of the AC gate signal, another AC stress is applied (see Fig. 10a). The stress times are chosen to be 100 ms, such that only the traps with short capture and emission times are activated.

All measurements were performed on the same device and no increase of the long-term shift in V_{th} was observed for all measurements. The most relevant part for the application is the hysteresis at the shortest possible measurement delay.

In Fig. 10d), exemplary for one stress condition, the first measurement points of a V_{th} recovery trace with a measurement delay of 1 µs are shown with respect to their timing position at the interruption of the AC signal.

In Fig. 11a) and b), the measured V_{th} at T = 175°C during a 50 kHz AC signal is shown for a varied V_{low} at two different V_{high} voltages. We observe a short-term hysteresis of the threshold voltage of up to 4 V (see Fig. 11 b) for V_{low} = −10 V and V_{high} = 20 V). We have furthermore performed measurements for the different V_{high} and V_{low} combinations at T = 25°C. A first observation is the increased initial V_{th} compared to T = 175°C due to the intrinsic temperature dependence of the threshold voltage (see Fig. 11c–d).

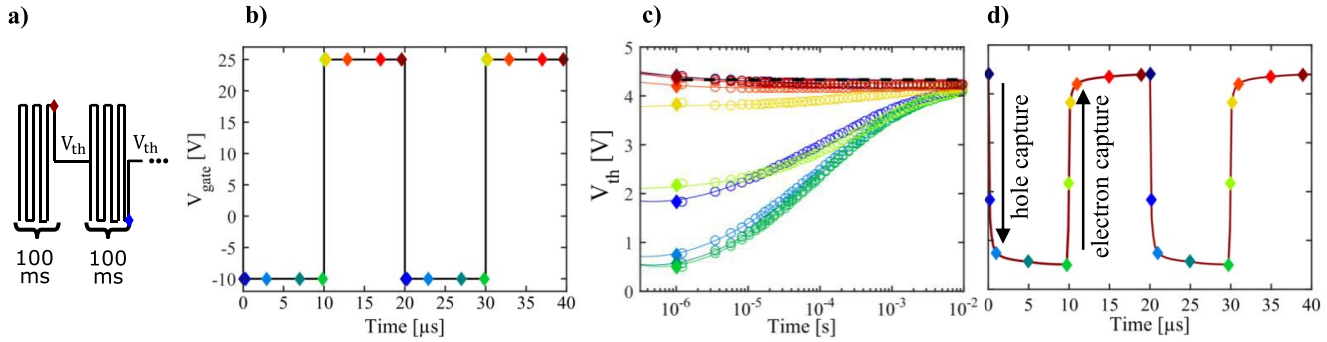

Fig. 10. Explanation of the measurement technique, example with real data (T = 175°C, V_{high} = 25 V, V_{low} = −10 V, f = 50 kHz): **a)** The AC stress is interrupted at different positions in time of the rectangular signal. Directly after end of stress, the threshold voltage is measured from 1 µs to 10 ms recovery time. Between each measurement point another AC stress of 100 ms is applied in order to restore the pre-measurement trap occupation state. **b)** An example 50 kHz bipolar AC signal is shown with different points of interruption as described for a). In **c)** The V_{th} measurement after each interruption of the AC signal is shown on a logarithmic time scale. **d)** The first measurement point (after 1 µs measurement delay) is shown with the corresponding timing position during the AC signal. The threshold voltage hysteresis is mostly due to capture and emission (neutralization) of positive charges (hole capture and electron capture).

For Si MOSFETs the short-term threshold hysteresis during AC stress amounts only to a few mV, due to a very small portion of traps with short capture and emission time constants. As we have already observed for the negative DC stress (see Fig. 8), for SiC there is a fast decrease in V_{th} during negative gate stress. This is caused by the previously described capture of holes with capture times below 1 µs. In contrast during the V_{high} signal we observe an increase in V_{th}.

This increase is both due to the capture of electrons during positive voltage stress (see Fig. 6) as well as the acceleration of recovery after negative gate stress with increasing V_{gs} (compare Fig. 9). The capture times for hole capture are a lot faster than for electron capture, therefore a fast saturation during the V_{low} signal is observed. The saturation within 10 µs is in a first approximation independent of the V_{low} voltage, whereas saturation of electron capture during the 10 µs V_{high} signal phase is only observed for V_{high} > 10 V (compare Fig. 11 a) and c). An analysis of all minimum values of V_{th} during the bipolar AC stress of the different V_{high} and V_{low} combinations can be found in Fig. 12.

The minimum value of V_{th} during the AC stress itself is exponentially dependent on V_{low} (see Fig. 12). Only a slight dependence on V_{high} is observed for both temperatures with an offset mainly due to the higher initial V_{th} at T = 25°C [23].

A comparison of all maximum values of V_{th} during the bipolar AC stress is shown in Fig. 13. The maximum value of V_{th} increases with increasing V_{low} and is linearly dependent on V_{high}. Nonetheless, the absolute ΔV_{th} hysteresis is dominated by the dependence on the V_{low} voltage. For the V_{high} phase, the most interesting parameter is the time it takes to reach the maximum value V_{th} during AC stress. This is mainly dependent on the recovery after the negative gate stress. The time until saturation decreases with increasing V_{high} (see Fig. 9). Furthermore, comparing Fig. 11 a) and Fig. 11 c), we observe a slower increase of V_{th} after the negative voltage phase for T = 25°C, which is consistent with the results presented in Fig. 9. Based on these measurements, the impact of the hysteresis on circuit operation is studied and estimated.

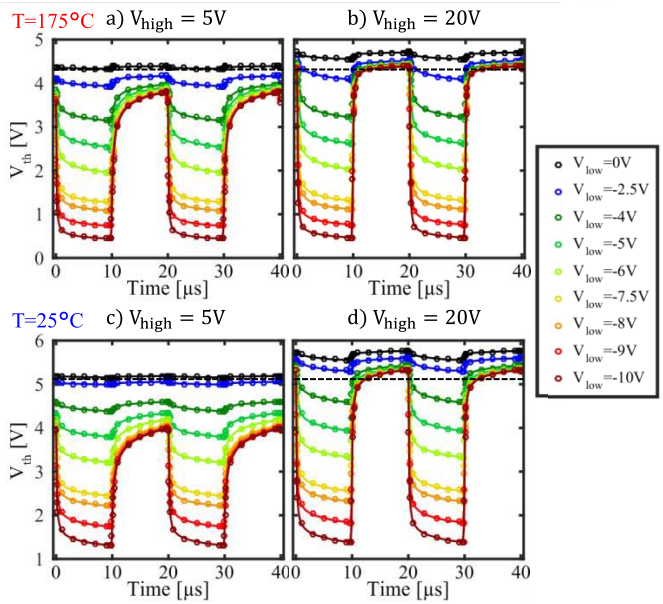

Fig. 11. Threshold voltage hysteresis at a bipolar AC signal with frequency of 50 kHz. The measured V_{th} dependence on the AC signal with varied V_{low} is shown for T = 175°C with a) V_{high} = 5 V and b) V_{high} = 20 V as well as for T = 25°C in c) and d). The initial V_{th} is marked as dashed line.

V. Impact on Circuit Operation

For Si, the V_{th} hysteresis during a bipolar AC signal amounts to only a few mV and is uncritical. For SiC, the short-term threshold voltage hysteresis mainly due to negative gate bias has been already observed during the measurement of IV-curves in a shift of the subthreshold voltage [4]. Fortunately, this effect is not permanent and recovers quickly within a fraction of the positive gate bias pulse. Also, the threshold voltage hysteresis itself does not increase after end of life. To estimate the effect of the threshold voltage hysteresis on the circuit operation performance in the sub-µs regime, we already studied the recovery after negative stress dependent on the recovery voltage (see Fig. 9). In these first 100 ns of the switch from

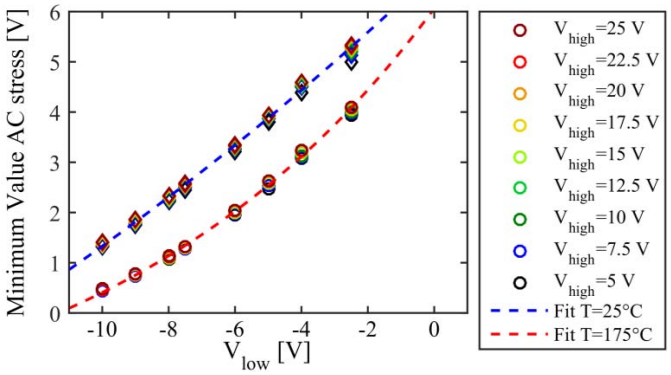

Fig. 12. Minimum V_{th} value during AC stress (see Fig. 11 dependent on V_{low} at T = 25°C and T = 175°C. It increases with increasing V_{low} (dashed fit) and is roughly independent on V_{high}. The minimum value at T = 25°C is increased compared to T = 175°C mainly due to the temperature dependence of 0h-V_{th}.

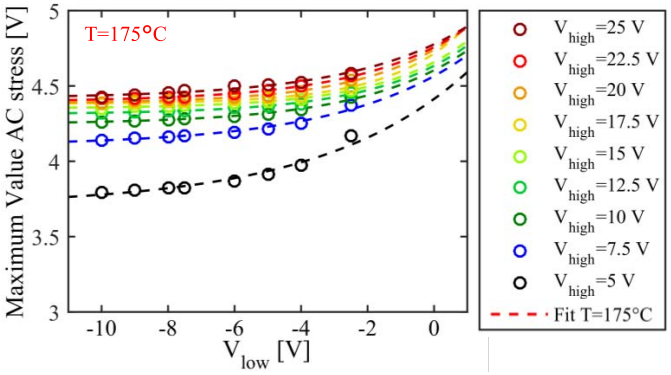

Fig. 13. Maximum V_{th} value during AC stress (compare Fig. 11) increases exponentially with increasing V_{low} at T = 175°C (dashed fit). However the more dominant dependence is the linear dependence on V_{high}.

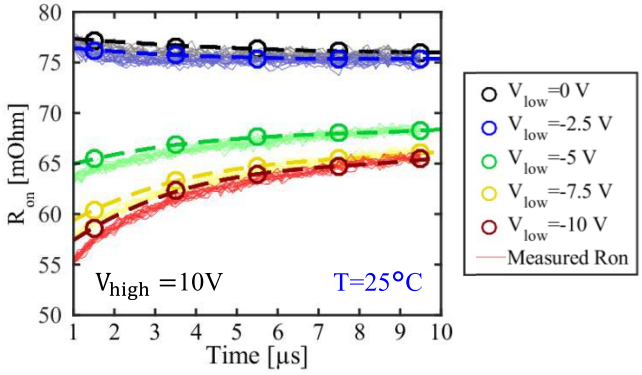

Fig. 14. R_{on} during the V_{high} period of the AC stress for different values of V_{low} with V_{high} = 10 V with I_d = 100 mA at T = 25°C. Thin lines: Directly measured R_{on} for 50 successive periods. Circles: R_{on} calculated from measured static I_d-V_g and the ΔV_{th} from The dashed lines are a guide to the eye connecting the circles. The change in R_{on} is therefore during AC stress fully recoverable.

negative to positive stress voltage, the negative ΔV_{th} actually helps to switch the MOSFET faster into the "on"-state than without this ΔV_{th}. As a matter of fact, R_{on} is actually lower after negative gate stress.

In Fig. 14 we present the measured R_{on} during the V_{high} period (transistor is "on") of the AC stress for different V_{low} voltages. For the comparison of R_{on} with ΔV_{th} we use a temperature of T = 25°C, because R_{on} is increased compared to T = 175°C and the transconductance decreases by a factor of three, which decreases the impact of ΔV_{th} on R_{on}. Furthermore, we chose V_{high} = 10 V because at higher gate voltages (i.e., 15 V) ΔV_{th} recovers too fast to be seen as a clearly measurable change in R_{on} (see Fig. 9). The change of R_{on} during AC stress is only correlated to the observed ΔV_{th} during AC stress and shows the same dependencies as ΔV_{th} in Fig. 11. With the measured ΔV_{th} during AC stress at T = 25°C and V_{high} = 10 V we calculate the change in R_{on} using a static I_d-V_g curve in the linear regime (R_{on} dependent on the gate voltage) as reference.

The observed ΔV_{th} can be directly mapped to R_{on} (see circles in Fig. 14) with a perfect agreement. Furthermore, R_{on} increases back to its initial value with recovering V_{th}. An even lower R_{on} is expected for t $\leq$ 1 μs which is not shown in Fig. 14 due to the finite settling time of the measuring amplifier. Note that ΔV_{th} is the only cause for ΔR_{on} and can fully explain the change in magnitude of R_{on}. Possible changes in the mobility apparently do not play a role. This has three highly positive conclusions: First, we can fully explain and model the change in R_{on} during AC stress. Second, the change in R_{on} is also fully recoverable just as V_{th} and third, R_{on} is lowered during the negative (V_{low}) period of the AC stress and therefore helps to switch the SiC-MOSFET faster, while minimizing static losses.

VI. Simulating Long Term AC Stress

We have shown in Section III that ΔV_{th} under positive gate bias stress contains large fast recovering components. Furthermore, we have demonstrated that we can model the DC ΔV_{th} using CET maps. The concept of CET maps is especially beneficial for the simulation of AC signals. To obtain the V_{th} response to a digital AC signal, the occupancy of the CET map has to be evaluated. For a digital signal a derivation of the occupancy level of the defects after AC stress can be found in [24]. In Fig. 15 we compare the measurements of ΔV_{th} after DC stress at two different temperatures (T = 25°C and T = 175°C, see Fig. 1) to the ΔV_{th} after stress for two different V_{high}/V_{low} combinations at T = 175°C with a frequency of 50 kHz. The ΔV_{th} after AC stress is measured directly at the end of the high voltage period with a measurement delay of 1 µs. We observe that ΔV_{th} after AC conditions (25/5 V as well as the 25/0 V) have the same power-law exponent as the DC stress (see Fig. 15 on the right). This already indicates that no further effects are involved during positive AC stress.

The activation energy map obtained by fits to the DC measurements (see Fig. 3) can therefore be used to obtain the simulations of all measurements. Because the recovery voltage used to obtain the activation energy map is the same as the V_{low} for the 25/5 V AC stress, the simulation can be directly obtained by the multiplication of the CET Map at T = 175°C with the defect occupancy map for the corresponding AC stress pattern. The obtained result shows very good agreement with

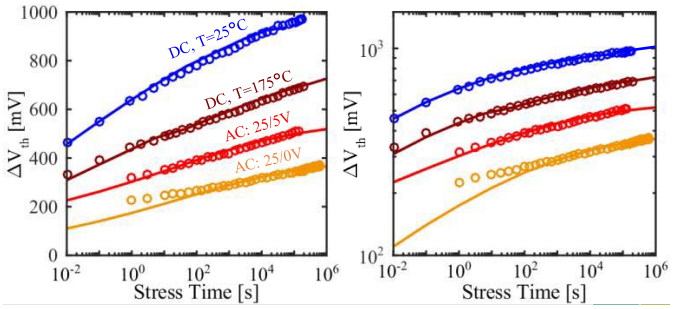

Fig. 15. Simulation from DC CET map (shown in Fig. 3) and measurements of ΔV_{th} after 25 V DC 25°C (blue) and 25 V DC (dark red), 25/5 V AC (red) and 25/0 V (orange) AC gate stress at T = 175°C (linear scale on the left, log scale on the right). Measurement delay is 1 µs. The AC measurements were performed at a frequency of 50 kHz and a duty cycle of 50%, equivalent to alternating $t_s = 10\mu s$ and $t_{rec} = 10\mu s$. The straight lines correspond to the fits of the measurement data obtained from the DC CET map. To simulate the 25/0 V AC signal the stress time is $t_s = 10\mu s$, the equivalent recovery time is $t_{rec,0V} = 3 \cdot t_{rec,V_{th}}$. Simulation and measurements show a very good agreement.

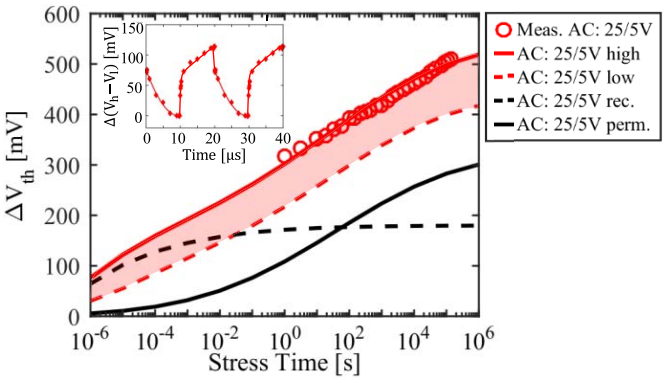

Fig. 16. Simulation and measurements of ΔV_{th} after 25/5 V AC (red) gate stress at T = 175°C and a measurement delay of 1 µs. The AC measurements were performed at a frequency of 50 kHz and a duty cycle of 50%. The lines correspond to the simulation obtained from the CET map shown in Fig. 3. The solid red line corresponds to the simulated ΔV_{th} of the CET map in Fig. 3 with interruption of the AC stress after the 10 µs high pulse (same as measurement condition, circles) and with interruption of the AC stress after the 10 µs low pulse (dashed red line). The black lines correspond to the contribution of the recoverable (dashed black line) and the permanent component (solid black line) from the CET map in Fig. 3. In the inset the threshold voltage hysteresis within the high and low pulse is shown.

the measurement data only limited by sample to sample variation. Up to now, the CET map only contains information about the recovery at the threshold voltage. It is also known for Si that the recovery is accelerated with decreasing gate voltage V_{gs}. The portion of ΔV_{th} recovery during the AC stress with $V_{low} = 0$ V is bigger than with $V_{low} = 5$ V. Thus, the degradation after 25/0 V AC stress is lower than at 25/5 V (compare Fig. 15). To simulate these results with the CET Map, we kept the high period time constant at $t_s = 10\mu s$ and varied the equivalent recovery time. We obtained a good agreement with the measurement data for $t_{rec,0V} = 3 \cdot t_{rec}$.

To demonstrate the impact of each component of the activation energy map, we show in Fig. 16 the evolution of ΔV_{th} within the 25/5 V AC stress at T = 175°C at a frequency of 50kHz (same data as red circles in Fig. 15).

Simulation results shown in Fig. 15 as well as the red solid line correspond to both the contribution of the recoverable and more permanent component of the activation energy map. The black solid line shows the contribution of the more permanent defects whereas the black dashed line shows the contribution of the recoverable defects in the capture and emission time map in Fig. 4. Already after 1 ms AC stress, the contribution of the recoverable defects does not increase any more – these defects are the defects responsible for the short-term hysteresis and do not contribute to the long-term ΔV_{th}. In contrast, the contribution of the more permanent defects increases, as expected, with AC stress time (compare to Fig. 4).

The measurements as explained above have been performed by interrupting the AC stress directly after the end of the high voltage period. The dashed red line shows ΔV_{th} simulated at the end of the low voltage period. The difference between V_{th} at the end of the low and end of the high voltage period is the short-term hysteresis within the long-term AC stress. Therefore, the highlighted red area marks the constant charging and discharging of the recoverable defects. The corresponding short-term hysteresis with a ΔV_{th} of 120 mV is shown in the inset of Fig. 16.

The hysteresis does not increase for the long-term AC stress which has been verified with hysteresis measurements before and after the AC stress. We demonstrated that the concept of analytic CET maps can be used with a high accuracy to predict the temperature and voltage dependence of DC SiC positive gate bias stress. Moreover the analytics CET map is a valuable method to simulate different AC gate stress signals.

VII. Conclusions

ΔV_{th} under positive gate bias stress contains large fast recovering components which remain undetected during JEDEC-like tests as defined for silicon devices. We observe a strong influence of the measurement delay on the parameters required for lifetime prediction, e.g., stress time dependence, measured apparent activation energies and voltage acceleration factors. A JEDEC test with measurement delay of hours will not be sufficient for lifetime predictions under application conditions and has to be improved [21]. An alternative to the standard JEDEC test is to use a preconditioning approach [25], which eliminates the contribution of the fast recovering components of the negative as well as the positive ΔV_{th}. With this approach the dependence of the extracted lifetime on the measurement delay is drastically reduced, but information about recovering components in the sub millisecond regime is lost. To investigate the impact of the fast recovering components, we propose utilizing only gate bias stress occurring in the application (negative DC and AC only) and a shortest possible measurement delay (e.g., 1 µs). Furthermore it is recommended to stress at high temperature and cool-down with stress voltage applied to measure the recovery at room temperature. This ensures that also for high stress temperatures the traps with low emission activation energies are within the measurement range and provides a comparability of all temperatures.

We have presented a measurement technique using a bipolar AC gate bias stress, which is application-relevant and can simulate any AC/DC stress sequence or history, exactly like in

the application. V_{th} read-outs are done at well-defined points of the AC-stress with a 20ns timing accuracy. Our measurements show that applying a bipolar AC gate bias stress causes large and very fast fully recoverable threshold voltage hysteresis as seen before in [4] with magnitudes up to 4 V. We can fully explain this behavior as being due to capture of positive charges in the oxide and at the interface when the gate is negative and neutralization of these positive charges as well as capture of negative traps within the 10 μs AC-positive period. We also observe, as expected, a voltage acceleration of the positive charge emission as well as capture of negative charges in the oxide when the gate is positive. Utilizing a fast measurement technique, that is short stress pulses (100 ns) and continuously measured recovery from μs to s, we are able to determine the time constants for capture and emission of these positive and negative charges as a function of the applied bias. The neutralization of the positive charges occurs within $\sim$100 ns after switching the gate to a positive voltage. It is clear that the threshold voltage hysteresis during normal operation makes a standard SPICE model, which assumes a fixed threshold voltage, not usable to explain effects caused by this threshold voltage hysteresis.

To analyze the physical nature of the defects responsible for the threshold voltage hysteresis, spectroscopy on individual defects like for NBTI would be mandatory [16]. Presently such measurements are not yet available, thus we refrain from speculations on the physical origin of these effects.

Furthermore, we have shown that with the analytic CET maps we can explain the temperature and voltage dependence of ΔV_{th} after DC stress and are able to calculate V_{th} at any positive AC gate stress. We have demonstrated that the AC long-term measurements can be simulated with high accuracy from the analytic CET maps. This modeling approach has proven to be also valid for SiC, enabling lifetime modeling after an arbitrary stress signal. In addition, we have shown that ΔR_{on} during AC stress can be fully attributed to ΔV_{th} and can fully explain the change in magnitude of R_{on}. Furthermore, this ΔR_{on} is, as ΔV_{th}, fully recoverable. At this point we want to emphasize that ΔV_{th} (and the related increase of R_{on}) which is relevant for an application is not any recovered ΔV_{th} measured after a delay. Instead, it is the completely unrecovered ΔV_{th} as occurring after the positive period of AC-stress. This unrecovered V_{th} cannot be measured but can only be estimated from the CET map. It has also been demonstrated that the change in R_{on} due to the hysteresis has no harmful effect when the MOSFET works in a switch-mode converter, because R_{on} is lowered during the negative period of the AC stress and therefore helps to switch the SiC-MOSFET faster while minimizing static losses and temperature increase of the device.

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