

# Preconditioned BTI on 4H-SiC: Proposal for a Nearly Delay Time-Independent Measurement Technique

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**Abstract**—When using JEDEC-like measurement patterns, MOSFETs based on 4H-SiC show amplified voltage shifts during gate bias stress compared to their silicon-based counterparts. We show that the majority of the extracted voltage shift originates from fully reversible components and strongly relies on stress-independent measurement conditions such as the reference point for the calculation of the voltage shift and timing parameters. An enhanced bias temperature instability measurement technique using device preconditioning is presented and compared to standard JEDEC-like measurement patterns developed for bias temperature instability evaluation of silicon MOSFETs. We show that preconditioned measurements allow for accurate and nearly delay and recovery time independent extraction of the permanent component within typical industrial timescales.

**Index Terms**—4H-SiC, bias temperature instability, delay time dependence, MOSFET, preconditioning, reliability, threshold voltage shift.

## I. INTRODUCTION

SILICON carbide (SiC) as a wide bandgap (WBG) semiconductor promises superior performance for power device operation due to the 10 times higher breakdown field and 3 times higher thermal conductivity than silicon (Si) [1]. As such, SiC power MOSFETs enable operation at elevated temperature, higher switching frequency, and power density than their Si-based counterparts. However, the larger bandgap of 3.23 eV at 300 K leads to extended interactions of free carriers with interfacial trap states. These states are within the SiC bandgap but outside the Si bandgap and lead to enlarged bias temperature instability (BTI) and hysteresis effects [2]–[4]. Although there have been enormous improvements to the electrical performance within the recent years by interface

annealing in nitrogen-containing atmospheres, such as nitrous oxide (N<sub>2</sub>O) or nitric oxide (NO), silicon carbide (SiC)-based power MOSFETs still show one to two orders of magnitude higher interface state densities  $D_{it}$  as their Si-based counterparts [5]–[7].

BTI, as one of the main topics of interest in countless reliability studies based on 4H-SiC MOSFETs [8]–[11], is caused by charge trapping at or near the SiC/SiO<sub>2</sub> interface during (high temperature) gate stress, resulting in threshold voltage  $V_{th}$  variations, which depend on the polarity of the stress voltage  $V_G^{str}$ . A positive  $V_G^{str}$  shifts  $V_{th}$  to more positive gate voltages, whereas a negative  $V_G^{str}$  shifts  $V_{th}$  to more negative gate voltages. Especially for SiC-based power devices, a large positive voltage shift  $\Delta V$  is undesirable because the voltage overdrive in the ON-state is decreased which in turn leads to increased on-resistance and static losses, respectively. A more detailed discussion on the application relevance of BTI for SiC-MOSFETs is given in [10].

In this paper, we focus on various  $\Delta V$  extraction techniques after positive bias stress (PBS). It will be demonstrated that the majority of  $\Delta V$  typically observed in standardized measurement tests (e.g., JEDEC-like) on 4H-SiC devices results from erroneous extraction techniques including stress independent but fully reversible components, which do not degrade the device performance under regular dynamic operation. A new drift evaluation technique based on what we call *device preconditioning* before each  $\Delta V$  readout is presented, which allows for a more comprehensive and nearly measurement delay-time independent determination of the permanent voltage shift component  $P(t_s)$ . This component emerges after ac and dc stress and is of fundamental importance from an application perspective. While this paper is based on our previous work [11], here the topic is discussed in far more detail and additional information on the temperature and time dependence of the preconditioning scheme is provided.

## II. THEORETICAL BACKGROUND

BTI results from charge trapping at or near the semiconductor–insulator interface after the creation of crystallographic defects or the charging of already existing precursors [12], [13]. Despite the fact that BTI in Si-based devices has been investigated for more than half a century, the detailed atomic origin is still heavily debated.

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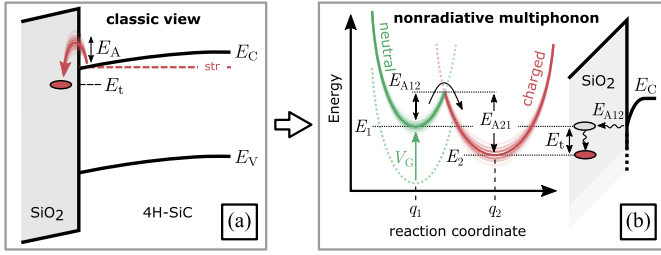


Fig. 1. (a) Classic view of the trapping mechanism extended with a distributed  $E_A$ . (b) Modern interpretation using NMP theory with distributed  $E_{A12}$  and  $E_{A21}$ .

Several microscopic defect candidates are under intensive investigation, including various interactions with hydrogen (diffusion, hopping, depassivation of Si dangling bonds, and so on) [14], [15],  $\text{SiO}_2$  intrinsic electron traps [16], [17], oxygen vacancies [18], or dangling bonds [19]. Although the absolute  $\Delta V$  is more pronounced in SiC-based devices, likely due to the larger bandgap, the BTI characteristics are, at least to some extent, analogous to Si-based devices, indicating similar atomic origins.

A typical model for the charge trapping mechanism is shown in Fig. 1(a) assuming a single trap state at the energy level  $E_t$  within the oxide close to the  $\text{SiC}/\text{SiO}_2$  interface. We extend the classic model by introducing an activation energy  $E_A$ , which depends on the Fermi-level  $E_F$ . Furthermore, we assume  $E_A$  of the trap state to change its occupancy to be normally distributed. A more comprehensive explanation of the atomic mechanism is given by nonradiative multiphonon (NMP) model [Fig. 1(b)], which also accounts for the atomic deformation of the defect when the charge state is changed and the electric field dependence for both capture and emission times of the defect [13]. In the NMP model, the neutral and charged states of a defect are described as a parabolic function representing the possible energy states. Here,  $q_1$  and  $q_2$  are the reaction coordinate equilibrium positions with the distributed local ground state energies  $E_1$  and  $E_2$  of the neutral and charged states, respectively. As an example, we start with a neutral precursor described by the green parabola. After providing enough energy  $E_{A12}$  through lattice vibrations to change the charge state, the states' configuration changes (e.g., bond length, equilibrium nuclei position, and so on) and is now described by the red parabola. Hence,  $E_A$  for the reverse transition from the charged (red) to the neutral (green) state is given by  $E_{A21}$ .

Assuming a distributed  $E_A$ , the capture/emission process is also distributed in time according to the characteristic capture or emission time constant  $\tau$

$$\tau = \tau_0 \exp\left(\frac{E_A}{k_B T}\right) \quad (1)$$

with the Boltzmann constant  $k_B$ , the temperature  $T$ , and the pre-exponential factor  $\tau_0$ .

The influence of a distributed  $E_A$  on  $\Delta V$  is shown in Fig. 2. For instance, a normally distributed  $E_A$  with a mean value  $\mu = 1$  eV and standard deviation  $\sigma = 0.1$  eV [Fig. 2(a) (green line)] will lead to a voltage shift versus stress-time behavior with trapping times within  $1 \times 10^4$  s

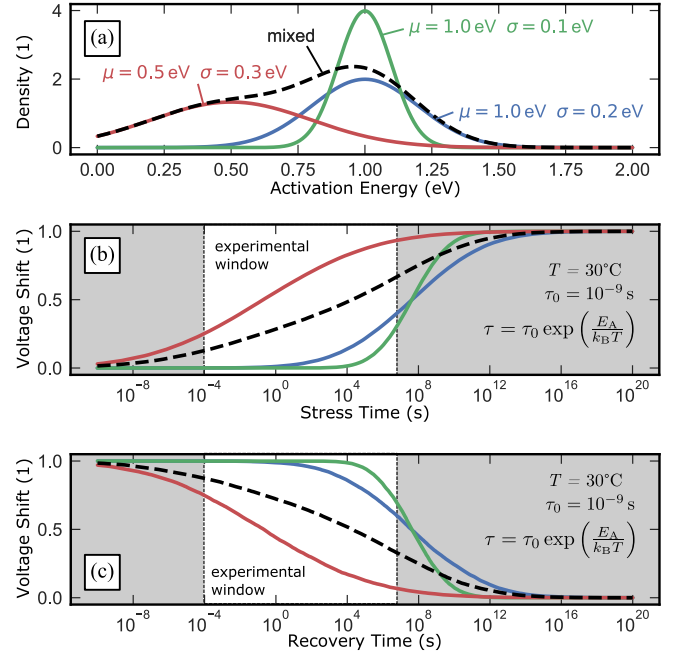


Fig. 2. (a) Simulated impact of distributed activation energies on the observed  $\Delta V$  during (b) stress and (c) recovery according to (3). The dashed black line represents a mix of the red and blue distributions, which leads to a broad distribution enabling the often used power-law approximation, within narrow experimental windows.

and  $1 \times 10^{12}$  s [Fig. 2(b) (green line)]. Increasing the width of the  $E_A$  distribution will lead to a larger stretch out of the stress-time dependence, as is shown in blue ( $\mu = 1$  eV,  $\sigma = 0.2$  eV) and red ( $\mu = 0.5$  eV,  $\sigma = 0.3$  eV). Fig. 2(c) represents the recovery behavior for the same set of activation energies assuming all trapping centers have been filled during the preceding stress. In real devices, a combination of various defects with characteristic energy barriers will contribute, leading to a convolution of the individual voltage shift versus time behaviors [13]. For a broadly distributed  $E_A$ ,  $\Delta V$  approaches the often used power-law approximation

$$\Delta V = A \cdot t^k \quad (2)$$

with the prefactor  $A$  and the power-law factor  $k$ , which is only valid within a certain time window. An example of a mixture between two individual defects (red and blue lines) is given in Fig. 2 as a dashed black line for stress and recovery.

Instead of using (2), a physical way to describe  $\Delta V$  during bias stress or recovery is given by [20]

$$\Delta V(t_x) = \frac{\Delta V^{\max}}{2} \operatorname{erfc}\left(K \frac{k_B T \ln\left(\frac{t_x}{\tau_0}\right) - \mu}{\sqrt{2}\sigma}\right) \quad (3)$$

with the complementary error function,  $\operatorname{erfc}$ , the stress or recovery time  $t_x = t_s$  or  $t_x = t_r$ , the maximum voltage shift  $\Delta V^{\max}$  as an additional fitting parameter and the parameters of the normal distribution  $\mu$  and  $\sigma$ . The prefactor  $K$  is  $-1$  for stress and  $1$  for recovery. Note that the parameters of the normal distribution of  $E_A$  for capture and emission processes,  $\mu$  and  $\sigma$ , do not necessarily correlate. A narrow distribution in  $E_A$  for the capture process  $E_{A12}$

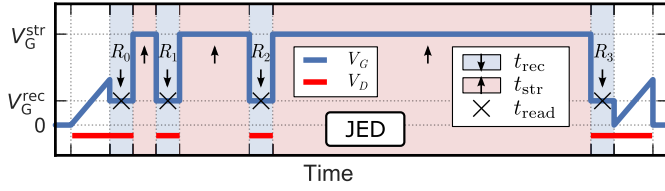


Fig. 3. BTI measurement pattern according to JEDEC standard JESD 241 [21]. In the sections marked with red lines,  $V_D = 0.1$  V, whereas  $V_D = 0$  V everywhere else.

usually results in a broadly distributed  $E_A$  for the emission process  $E_{A21}$  and vice versa [13]. As can be seen from (3), the time evolution of  $\Delta V$  scales with the logarithm of  $t_s$  or  $t_r$ , resulting in a fundamental dependence of the measurement timing on the extracted  $\Delta V$  as will be discussed in Section IV.

### III. EXPERIMENTAL SETUP

All devices were fabricated on 4H-SiC *n*-doped substrates using an industrial process. The *n*-channel (11 $\bar{2}$ 0)-plane (a-face) MOSFETs received a SiO<sub>2</sub> dielectric via chemical vapor deposition. Post oxidation anneal was done in a nitric oxide (NO) containing atmosphere for all samples. Measurements were performed on wafer level using an Agilent B1500A parameter analyzer and Agilent E5250A switching matrix at room temperature unless otherwise stated. Changes in temperature were done via an ATT Systems P40 cooling unit.

### IV. IMPACT OF THERMAL NONEQUILIBRIUM DURING THE REFERENCE READOUT

A BTI measurement test according to JEDEC standard JESD 241 [21] is shown in Fig. 3. The measurement pattern consists of a gate voltage  $V_G$  sweep from 0 V to the maximum sweep voltage  $V_G^{\text{swe}}$  for the calculation  $\Delta V$  followed by a repeated readout cycle at the recovery voltage  $V_G^{\text{rec}}$  in sequence with a stress cycle at  $V_G^{\text{str}}$  with logarithmically increasing  $t_s$ . The drain voltage  $V_D$  is turned off during every stress cycle to suppress device heating, nonuniform electric oxide fields, and hot-carrier degradation. After each stress pulse,  $\Delta V$  is calculated from the recovery drain current  $I_D$  with respect to the reference  $I_D$  at the initial readout cycle (marked with  $R_0$ ).  $I_D$  at each subsequent readout cycle  $R_i$  is extracted at  $t_{\text{read}} = 100$  ms after the end of the stress pulse. The resulting  $\Delta V$  is shown in Fig. 4 (JED, blue line) after application of a stress voltage equal to two times the operation voltage  $V_G^{\text{op}}$  for  $t_s$  up to 1444 s at 30 °C. Using JESD 241, a  $\Delta V$  of 400 mV after 1444 s stress is recorded. A slightly changed but common variation of the JESD 241 standard measurement is shown in Fig. 5. The pattern is similar to the pattern sketched in Fig. 3 with one small deviation: we introduce a 10 s delay at  $V_G = 0$  V before  $R_0$  to represent the influence of the often ill-defined measurement delay. Although at first glance this modification appears to be negligible, the influence on  $\Delta V$  is significant as can be seen in Fig. 4 (JED0, green line). While the trend over time does not change, an offset of approximately  $\Delta V_0 = 200$  mV is introduced which is merely due to changing the bias value prior to  $R_0$ .

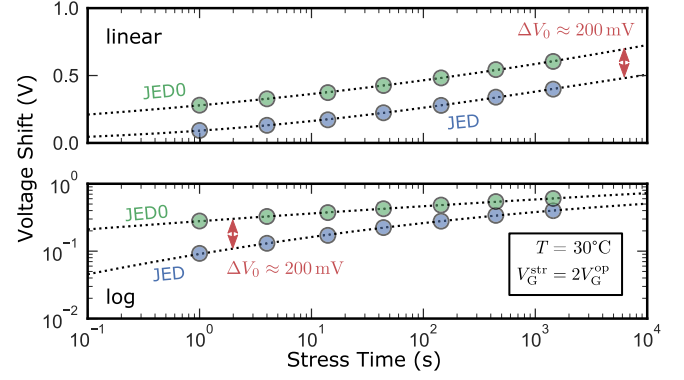


Fig. 4.  $\Delta V$  extracted via JED according to Fig. 3 in comparison with JED0 according to Fig. 5, where  $V_G$  was set to 0 V for 10 s before  $R_0$ . The minor change to the measurement pattern results in a 200-mV offset in  $\Delta V$ .

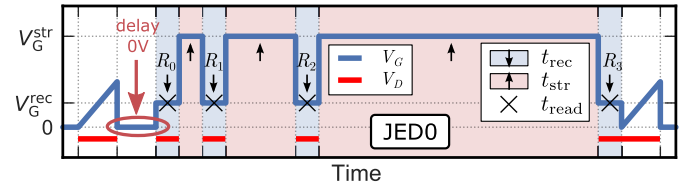


Fig. 5. Delayed BTI measurement pattern (JED0) similar to JED (Fig. 3), but with a delay at  $V_G = 0$  V before  $R_0$ .

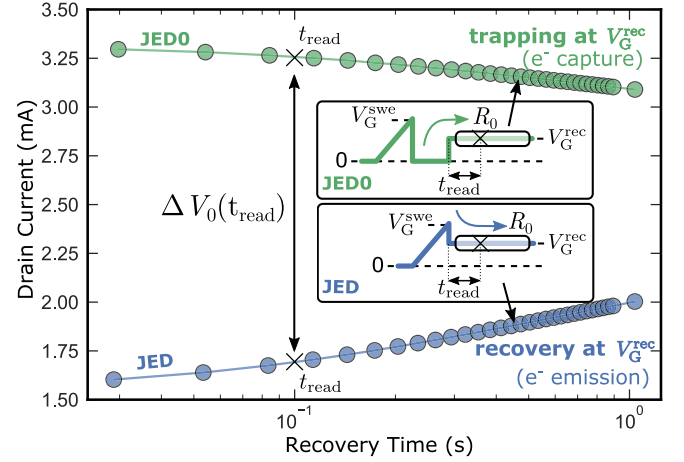


Fig. 6.  $I_D$  at  $R_0$  for JED (blue line—bottom) and JED0 (green line—top). Trapping or detrapping behavior depends on the preceding gate bias. After the 0 V phase,  $I_D$  is higher and decreases over time (JED0, electron capture), whereas after the switch from  $V_G^{\text{swe}}$  to  $V_G^{\text{rec}}$ ,  $I_D$  is lower and increases over time (JED, electron emission).

The offset  $\Delta V_0$  results from the fact that the interface charging state at  $R_0$  strongly depends on the bias history. Fig. 6 shows  $I_D$  at  $R_0$  ( $V_G = V_G^{\text{rec}}$ ) for both measurement patterns. The blue curve represents the measurement pattern according to JEDEC JESD 241 (JED), whereas the green represents the same pattern with a 10 s delay at  $V_G = 0$  V before  $R_0$  (referenced to as JED0). For JED, we observe increasing  $I_D$  after the bias change from  $V_G^{\text{swe}}$  to  $V_G^{\text{rec}}$ , indicating recovery of trapped electrons, which were captured at  $V_G > V_G^{\text{rec}}$  during the preceding voltage sweep. The opposite trend is observed for JED0 (green line). At the same  $V_G^{\text{rec}}$ , JED0 shows

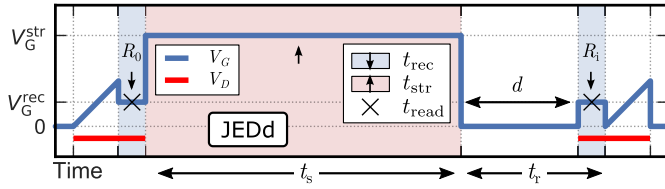


Fig. 7. Delayed JEDEC-like measurement (JEDd) similar to JESD 241 [21] extended with variable delay  $d$  at  $V_G = 0$  V after the stress.

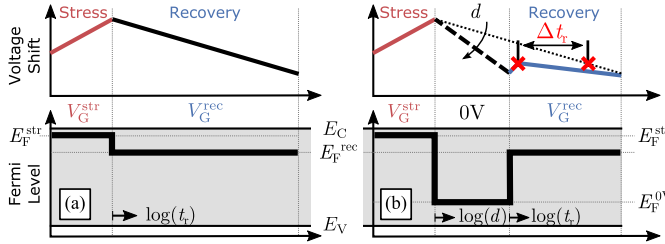


Fig. 8. Sketch of the impact of  $E_F$  on the recovery. (a) Switch from  $V_G^{\text{str}}$  to  $V_G^{\text{rec}}$  without delay. (b) Due to accelerated recovery during  $d$ ,  $t_r$  decreases by several orders of magnitude ( $\Delta t_r$ ).

a higher and decreasing  $I_D$  resulting from carrier trapping in oxide/border traps.

We therefore conclude that the discrepancy in  $I_D$  at  $R_0$  is due to the amount of time the system needs to reach thermal equilibrium at a certain  $V_G$ , meaning every trap state with an energetic position below  $E_F$  is filled with electrons and every trap state above  $E_F$  is empty. Especially in WBG semiconductors like SiC, reaching thermal equilibrium may take a long time (see Section II).

#### V. IMPACT OF MEASUREMENT DELAY TIMES ON $\Delta V$

In addition to a well-defined reference readout  $R_0$ , the timing of each subsequent  $\Delta V$  extraction point  $R_i$  after the stress cycle is of similar importance. An example for a delayed  $R_i$ , JEDEC-like, readout is shown in Fig. 7 (referred to as JEDd). The measurement pattern is similar to the JED pattern in Fig. 3, extended with a delay phase at  $V_G = 0$  V for the delay time  $d$  after the stress cycle. Especially, in industrial reliability tests, measurements are always delayed since the stress cycle is usually done in special high-temperature furnaces (accelerated BTI stress [22]) where many chips can be stressed in parallel for long times (e.g., 1000 h), whereas the readout is done outside the furnace sequentially for multiple devices at room temperature. The whole procedure of loading and unloading packaged devices naturally introduces a delay time between the termination of the stress pulse and the extraction of  $\Delta V$ .

The impact of  $d$  on  $\Delta V$  is sketched in Fig. 8 as a function of  $E_F$ , and data for multiple devices subjected to identical PBS is shown in Fig. 9.  $\Delta V$  is measured according to Fig. 7 (JEDd). Here,  $d$  varies from 0 to 30 s (black and blue lines). We see a decreasing  $\Delta V$  for increasing  $d$ . An explanation is given in Fig. 8 and in the inset of Fig. 9. The change in  $\Delta V$  is caused by varying  $E_F$  positions prior to the extraction of  $\Delta V$ . As such,  $\Delta V$  increases with stress time according to (3) (red line) during the stress cycle at  $V_G^{\text{str}}$ . By directly switching to  $V_G^{\text{rec}}$

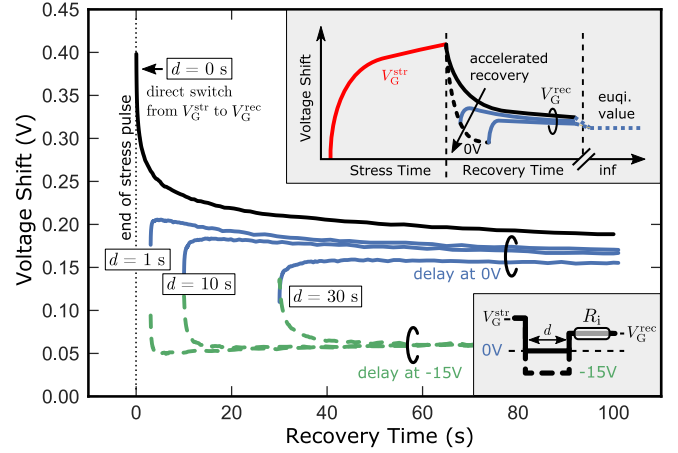


Fig. 9. Recovery behavior after identical PBS depending on  $d$ . The black solid line represents  $\Delta V$  with  $d = 0$  (direct switch from  $V_G^{\text{str}}$  to  $V_G^{\text{rec}}$ ). By introducing a delay phase at  $V_G = 0$  V between the stress and the recovery phase,  $\Delta V$  decreases with increasing  $d$  (blue line). Inset: mechanism via a steeper recovery curve at  $V_G = 0$  V (black dashed line). This effect increases by using an accumulation pulse during  $d$ , which results in less dependence of  $\Delta V$  on  $d$  (green dashed line).

without any delay ( $d = 0$  s),  $\Delta V$  follows the black recovery curve according to (3). By introducing a delay at  $V_G = 0$  V,  $E_F$  moves from a position close to the conduction band  $E_F^{\text{str}}$  to a position around the midgap  $E_F^{\text{0V}}$  leading to emission of trapped charges with energetic positions above  $E_F^{\text{0V}}$ , which results in a decrease of  $\Delta V$  (black dashed line). A subsequent bias change back to  $V_G^{\text{rec}}$  (blue line) will lead to a superposition of charge trapping for trap states with energetic positions below  $E_F^{\text{rec}}$  and above  $E_F^{\text{0V}}$  (visible as the rising edge) and the ongoing charge transition of states above  $E_F^{\text{rec}}$  which have not yet emitted their charge within  $d$ . As can be seen, the delayed recovery curve approaches a value smaller than recorded in the nondelayed trace. This shows that the delay phase at 0 V increases  $\Delta V$  recovery in comparison to  $V_G^{\text{rec}}$ .  $t_r$  is shifted to faster times by several orders of magnitude due to the strong dependence on  $\log(d)$ , as will be shown later in this paper. The same trend is observed for a floating gate contact (not shown), as would be the case in typical industrial measurements.

A feature that will be exploited in the following is the fact that  $\Delta V$  is further decreased by using an accumulation pulse instead of 0 V/floating [Fig. 9 (green dashed line)] during the delay phase. In this example, an accumulation pulse of  $-15$  V is used for the same range of delay times resulting in a decrease of  $\Delta V$  from  $> 150$  mV to  $\approx 60$  mV after  $t_r = 60$  s.

#### VI. PRECONDITIONED BTI

As mentioned before, BTI measurements of SiC-MOSFETs are highly sensible to the exact and timing conditions of each  $\Delta V$  readout (Fig. 9). Therefore, no reliable estimation of  $P(t_s)$  can be given. This is due to two essential facts: first, the extracted  $\Delta V$  depends on the reference readout timing and gate bias history since thermal equilibrium is not reached within a reasonable period of time, meaning  $I_D$  transients are still noticeable due to ongoing charge capture/emission



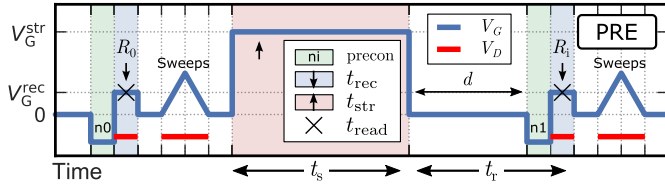


Fig. 10. Preconditioned BTI pattern (PRE) with accumulation pulse ( $n_i$ , green) before  $R_0$  and  $R_i$  to maintain identical switching conditions.

during  $R_0$ . Second, the switching condition of each subsequent readout usually differs from the switching condition of  $R_0$ . For example, in the JEDEC JESD 241 standard (Fig. 3),  $R_0$  is monitored after  $V_G^{\text{swe}}$ , whereas  $R_i$  is monitored after  $V_G^{\text{str}}$ . Therefore, the interface charging state differs for each readout, resulting in a stress independent offset in the extracted  $\Delta V$ .

To overcome timing and bias-dependent variations of  $\Delta V$ , we propose an optimized measurement pattern which we refer to as device preconditioning. The basic scheme is sketched in Fig. 10 for a PBS pattern and consists of the following features: first, we introduce exactly the same accumulation preconditioning pulse before *each* readout cycle to ensure a well-defined and comparable interface charge state at the instant  $V_G$  is switched to  $V_G^{\text{rec}}$ . By this, we isolate fast interface states (charging state is able to follow the gate signal) from application relevant border states with slower time constants allowing for an extraction of  $\Delta V$  nearly independent of  $d$  as shown in Section VI-A. Second, voltage sweeps (if needed for calculation of  $\Delta V$ ) are moved behind the readout. Therefore, the bias sweep does not influence the charge state of the trapping centers during the readouts, allowing for more comparable  $\Delta V$  extraction.

### A. Consequences of Preconditioning

Fig. 11 shows the impact of various readout arrangements on the  $\Delta V$  recovery curves after a 1 ks PBS (STR). Here, we start with an  $I_D$ - $V_G$  curve (SWE) for the calculation of  $\Delta V$ , to include its impact on the subsequent readouts. For  $R_0$ , we either use a bias switch from  $V_G = 0$  V to  $V_G^{\text{rec}}$  (JED0) or a preconditioned accumulation pulse readout as shown in Fig. 10 with bias switching from 0 to  $-15$  V ( $t_{\text{pre}} = 1$  s) to  $V_G^{\text{rec}}$ , which we refer to as  $n_0$ . Subsequent to STR,  $\Delta V$  extraction is done according to JEDEC JESD 241 by switching from  $V_G^{\text{str}}$  to  $V_G^{\text{rec}}$  (JED1) or via accumulation pulse preconditioning similar to  $n_0$ , referred to as  $n_1$ .

Each  $\Delta V$  recovery trace in Fig. 11 is given relative to one of the reference readouts JED0,  $n_0$ , or SWE (indicated via the minus sign). For simplicity, we start by analyzing JED0, a simple bias change from 0 V to  $V_G^{\text{rec}}$ . As shown in Fig. 6,  $I_D$  changes over time and can be converted to  $\Delta V$  by using SWE as reference. The outcome is shown in Fig. 11 as dotted purple line (JED0-SWE). In the JEDEC 241 measurement standard and numerous other studies, only a certain point in time  $t_{\text{read}}$  is used as the reference point for the calculation of  $\Delta V$  after bias stress. Due to this major drawback of JEDEC-like measurements,  $\Delta V$  changes drastically in amplitude and time dependence if  $t_{\text{read}}$  is changed. In our case,  $t_{\text{read}}$  represents the interface charge state 100 ms after switching to  $V_G^{\text{rec}}$ .

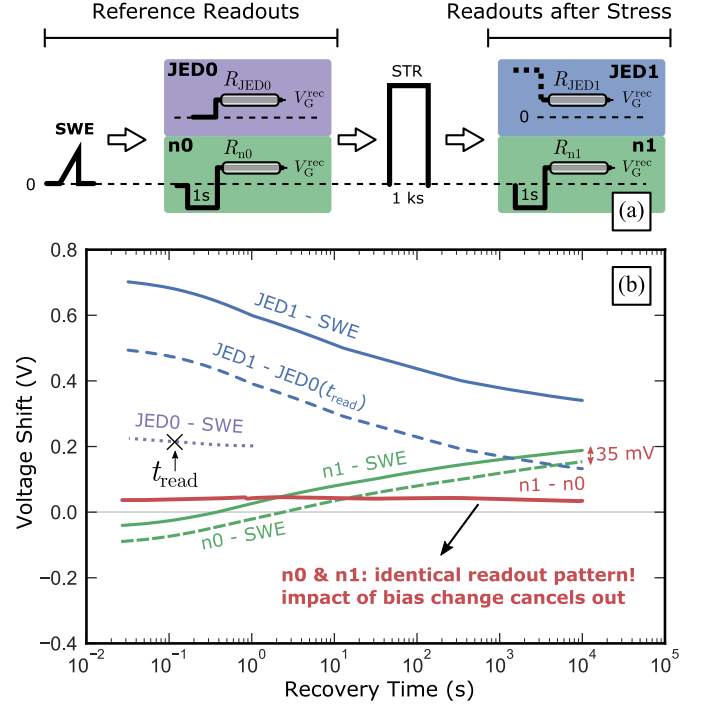


Fig. 11. (a) Reference and readout variations for  $\Delta V$  calculation. (b) Resulting  $\Delta V$  as a function of the chosen readout-reference combination. Preconditioning results in less recovery time dependence and more exact  $\Delta V$  extraction due to identical and, therefore, comparable switching conditions before each readout.

By using either SWE or JED0( $t_{\text{read}}$ ) as a reference point, we are now able to extract  $\Delta V$  induced by STR as a function of  $t_r$ . Fig. 11 shows the outcome in reference to SWE (blue solid line) or JED0( $t_{\text{read}}$ ) (blue dashed line). Both curves only differ in an offset of  $\Delta V_0 \approx 200$  mV, which is exactly  $\Delta V$  of JED0 at  $t_{\text{read}}$ .

Compared to the  $\Delta V$  recovery curves of JED1 (blue line), the time dependence changes drastically if we switch to the accumulation pulse preconditioned readout and, more importantly, always compare  $\Delta V$  within identical time frames, meaning  $t_{\text{read}}$  equals  $t_r$ . The solid and dashed green curves represent  $\Delta V$  at the readouts  $n_0$  and  $n_1$  with respect to SWE.  $n_0$ -SWE shows  $\Delta V$  before the stress, whereas  $n_1$ -SWE shows  $\Delta V$  after the stress. Since both readouts are performed under *identical and well-defined* switching conditions from accumulation to inversion,  $n_0$  and  $n_1$  show the same trend over time. This indicates that the form of the recovery curve mainly depends on the switching conditions since STR does not result in any noticeable change in the time dependence of  $\Delta V$ . The difference between both curves represents the real BTI due to STR since any impact from the switching cancels out. The resulting  $\Delta V$  is indicated in red and is nearly stable at 35 mV within the measured recovery time of 10 ks, giving a good estimation for  $P(t_s)$ . The comparison with the JEDEC-like measurement JED1-JED0, which shows a  $\Delta V$  of  $\approx 500$  mV recovering to 140 mV within the same recovery time, proves the importance of comparing pairs of values ( $\Delta V$ ,  $t_r = t_{\text{read}}$ ) rather than  $\Delta V$  prior and after the stress for reliable  $\Delta V$  measurements. Note that for industrial measurements, it is

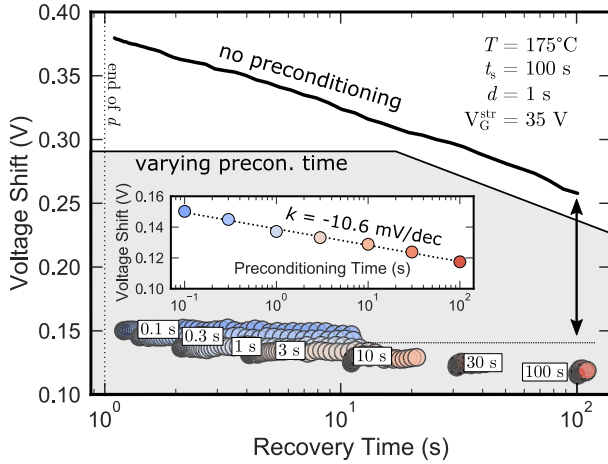


Fig. 12. Impact of  $t_{pre}$  varying from 0.1 to 100 s (circles) on  $\Delta V$ .  $\Delta V$  decreases with  $\log(t_{pre})$ . Therefore, even a short  $t_{pre}$  decreases the recovery time by several orders of magnitude. The mean  $\Delta V$  after  $t_{pre}$  is given in the inset.

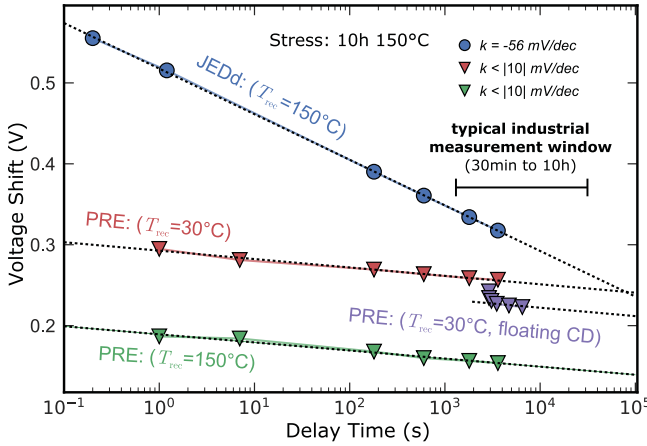


Fig. 13. Delay time dependence of  $\Delta V$  after 10 h, 5-MV  $\text{cm}^{-1}$  PBS at 150 °C. Readout was done at either 150 °C or 30 °C. The impact of  $d$  on  $\Delta V$  is reduced by more than a factor of 5 for PRE measurements, since fully recoverable components of  $\Delta V$  cancel out due to the preconditioning pulse.

usually sufficient to extract only one pair of values instead of the complete recovery transient as long as  $t_r = t_{read}$ .

The impact of the preconditioning time  $t_{pre}$  on  $\Delta V$  is shown in Fig. 12. As for  $t_r$  and  $t_s$ ,  $\Delta V$  decreases with  $\log(t_{pre})$ . Therefore, even a short  $t_{pre}$  of 1 s is sufficient to decrease the recovery time by several orders of magnitude.

### B. Minimized Impact of Delay Times

Especially in industrial BTI measurements with a large number of devices stressed simultaneously, delay times between the end of the stress pulse and  $R_i$  are inevitable. As shown in Fig. 9, delay times lead to high inaccuracy in the extracted  $\Delta V$  in JEDEC-like measurement due to ongoing recovery. Preconditioned BTI measurements, on the other hand, show much less dependence of  $\Delta V$  on  $d$  between the end of  $V_G^{str}$  and the beginning of  $R_i$ , allowing for more reliable extraction of application relevant  $\Delta V$ .

Fig. 13 shows the delay time dependence of  $\Delta V$  for a 10 h, 5 MV  $\text{cm}^{-1}$  PBS at 150 °C for delay times up to 1 h, which is in the range of typical industrial delay times. The delayed

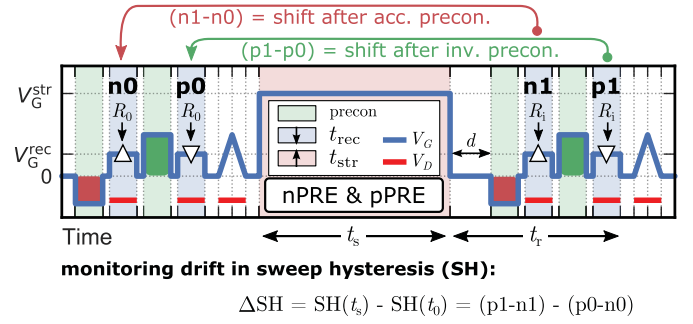
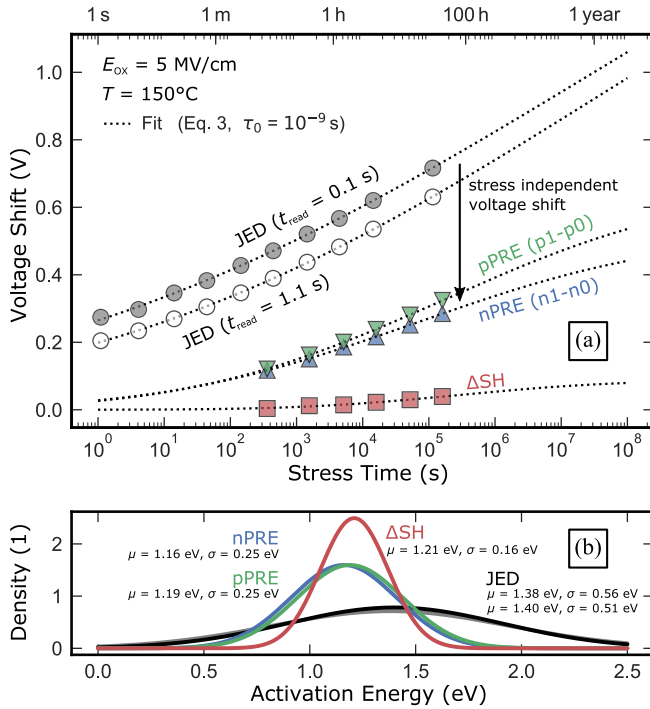


Fig. 14. Preconditioned BTI measurement pattern with accumulation and inversion pulse preconditioning allowing for additional hysteresis monitoring.

JEDEC-like measurement JEDd (see Fig. 7) is shown in blue circles, whereas the preconditioned measurements (according to Fig. 10) are shown with triangles labeled PRE. Readout was done at 150 °C (green and blue) or 30 °C with cooldown under  $V_G^{str}$  (red) or floating (purple). JEDd exhibits strong dependence of  $\Delta V$  on  $d$  and recovers from 560 mV for  $d = 0.2$  s to 320 mV for  $d = 1$  h representing a recovery slope of  $-56$  mV/dec at a recovery temperature of 150 °C. The preconditioned measurement at the same recovery temperature is shown in green triangles and represents  $\Delta V$  after identical stressing conditions. Since recoverable components, which are irrelevant for application, are eliminated,  $\Delta V$  shows five times less dependence on the delay time and ranges from 190 mV for  $d = 1$  s to 155 mV for  $d = 1$  h with slopes smaller than 10 mV/dec. The red curve represents PRE with readout performed at 30 °C and cooling down under  $V_G^{str}$  resulting in higher shift and less recovery, but identical dependence on  $d$ . The purple data represent  $\Delta V$  after cooling down performed under floating conditions, which results in data points shifted to longer delay times since the time needed to reach 30 °C adds to  $d$ . It is important to state that PRE does not lead to any additional degradation: a comparison of the change in charge pumping current after JEDd and PRE shows only a minor increase ( $<2\%$ ), which is within the device variation.

## VII. MONITORING OF FAST-STATE HYSTERESIS EFFECTS

4H-SiC MOSFETs show a hysteresis (SH) between gate voltage upsweeps from accumulation to inversion and the downsweeps from inversion to accumulation, which is especially visible in the subthreshold regime. The majority of SH is caused by fast interface states, which are fully recoverable during normal device operation within nanoseconds [4], [10], [23] and therefore cancel out as a result of using preconditioning pulses. However, the impact of BTI on the interface states causing the hysteresis has not been investigated until now. To enable monitoring changes in the hysteresis during high temperature gate stress,  $n0$  is extended via a second inversion preconditioning pulse  $p0$  at use-voltage, resulting in the measurement pattern shown in Fig. 14. By using negative and positive preconditioning pulses, ac-use conditions are mimicked. SH before the stress phase is given by the voltage shift after the positive  $p0$  and negative  $n0$  preconditioning,



**Fig. 15.** (a)  $\Delta V$  for  $t_s$  up to  $\approx 40$  h at  $150^\circ\text{C}$  for JEDEC JESD 241 (circles) with two different values for  $t_{\text{read}}$  and preconditioned BTI according to Fig. 14 after negative (nPRE, blue triangles up) and positive (pPRE, green triangles down) preconditioning. Although stress conditions are identical, PRE measurements show significantly less shift. The difference between pPRE and nPRE represents the change in SH as a function of  $t_s$  (red squares). (b) Parameters of the normally distributed  $E_A$  ( $\sigma$ ,  $\mu$ ) are extracted using (3) (assuming  $\tau_0 = 10^{-9}$  s).

whereas SH after the stress is given by the difference between p1 and n1. The change in SH due to BTI is therefore given by  $\Delta SH = (p1 - n1) - (p0 - n0)$ . Fig. 15 shows a comparison of the JEDEC JESD 241 and the preconditioned BTI after a 1 s accumulation pulse (negative PRE, triangles up) and after a succeeding 1 s inversion pulse (positive PRE, triangles down) for a 40 h,  $5 \text{ MV cm}^{-1}$  PBS at  $150^\circ\text{C}$ .

For JEDEC readouts,  $\Delta V$  is overestimated for given stress times and depends strongly on  $t_{\text{read}}$  because stress independent components, such as fully recoverable hysteresis effects, are not excluded. Preconditioned measurements eliminate a large fraction of these components resulting in an approximately 2–3 times lower and more application relevant  $\Delta V$ . The difference in  $\Delta V$  for negative and positive PRE results from the hysteresis (red squares), which slightly increases during high temperature, high field PBS. The fit (dashed line) was done according to (3) assuming  $\tau_0 = 10^{-9}$  s [22]. Extracted parameters of the normally distributed  $E_A$  ( $\sigma$ ,  $\mu$ ) are given in Fig. 15(b). PRE measurements show significantly reduced standard deviation with  $\mu = 1.18 \pm 0.05$  eV.

### VIII. CONCLUSION

We investigated the impact of various BTI measurement parameters on the extracted  $\Delta V$  of 4H-SiC power MOSFETs. A satisfying BTI procedure should assess exclusive parameter drifts, which degrade the *application relevant* device performance. However, using JEDEC-like measurements, the majority of  $\Delta V$  after high bias stress originates from

fully recoverable and stress independent shift components, which strongly depend on the measurement parameters and incorrectly add to the extracted  $\Delta V$ .  $\Delta V$  changes drastically by changing the reference point for the shift calculation and strongly depends on recovery and delay times of the measurement. To overcome this issue, we demonstrate a sophisticated BTI measurement pattern using device preconditioning for an exact determination of the application relevant  $\Delta V$ . By using similar and well-defined preconditioning pulses before each readout, fully reversible shift components are eliminated, thereby allowing for a more accurate extraction of the application relevant permanent component. Voltage shifts extracted via preconditioned BTI are less dependent on measurement delay times within industrial timescales and do not include fully recoverable hysteresis effects. Therefore, they enable more accurate lifetime prediction of 4H-SiC MOSFETs.

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