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Comprehensive Evaluation of Bias Temperature Instabilities on 4H-SiC MOSFETs Using Device Preconditioning

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Abstract. In comparison to silicon based devices, MOSFETs based on silicon carbide show more complex threshold voltage variations due to positive and negative gate bias stress. We show that the majority of the voltage shift in standard JEDEC-like bias temperature instability measurements originates from stress independent measurement parameters like timing and switching conditions. A more sophisticated bias temperature instability measurement technique using device preconditioning is presented allowing for more accurate and nearly delay time independent extraction of the permanent voltage shift component within typical industrial timescales.

Introduction

In SiC devices, bias temperature instability (BTI) is caused by charge capture/emission at or near the SiC/SiO_2 interface during (high temperature) gate stress V_G^{str}. Depending on the polarity of V_G^{str}, BTI results in a positive (electron capture) or negative (hole capture) shift of the threshold voltage V_{th}. A large positive V_G^{str} causes a positive threshold voltage shift ΔV and therefore reduces the overdrive in the on-state leading to increased on-resistance R_{on} and static losses [1,2].

A simplified classic model of the charge trapping mechanism during BTI is shown in Fig. 1 (left) assuming a single trap state near the SiC/SiO_2 interface at the energetic position E_t. At a fixed Fermi-level position E_F (e.g. during bias stress), the activation energy E_A of the trap state to change its occupancy is assumed to be normally distributed. Previous work on Si/SiO2 interfaces has shown that it is mandatory to consider the correct picture is given by the non-radiative multi-phonon (NMP) model (Fig. 1, right), which also accounts for atomic deformation of the defect subsequent to charge capture and the electric field dependence for both, capture and emission times [3, 4]. The activation energy for the reverse transition from the charged to the neutral state is therefore given by E_{A21}. Assuming a distributed E_A, the capture/emission process is also distributed in time according to the characteristic capture/emission time constant $\tau = \tau_0 \exp(E_A/k_B T)$ with the Boltzmann constant k_B, the temperature T and the pre-exponential factor τ_0. An example of the impact of distributed E_A on ΔV is given in Fig. 2. In real devices, a large variation of defects with characteristic energy barriers will contribute to the overall voltage shift leading to a mix-up of the individual ΔV over time behavior (Fig. 2, dashed line) [5]. For broadly distributed E_A, ΔV approaches the often used, but unphysical power-law approximation

$$\Delta V = A \cdot t^k \tag{1}$$

with the pre-factor A and the power-law factor k. Instead of using Eq. 1, a more physical way to describe ΔV during bias stress (assuming normally distributed E_A) is given by [5]

$$\Delta V(t_{str}) = \frac{\Delta V^{max}}{2} \cdot \mathrm{erfc}\left(-\frac{k_B T \ln(\frac{t_{str}}{\tau_0}) - \mu}{\sqrt{2}\sigma}\right) \tag{2}$$

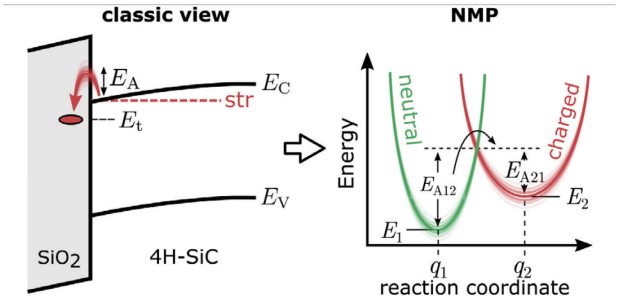

Fig. 1. Left: classic view of trapping mechanism with trap level E_t and distributed E_A. Right: Non-radiative multi-phonon (NMP) interpretation with distributed activation energies for capture E_{A12} and emission E_{A21}.

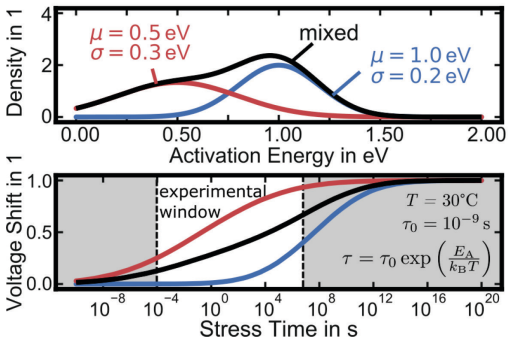

Fig. 2. Simulated impact of distributed activation energies (top) on the observed voltage shift during bias stress (bottom) according to Eq. 1. The dashed line represents a mix of the distributions $\mu = 0.5$ eV and $\mu = 1.0$ eV leading to a broadly distributed stress behavior.

with the complimentary error function erfc, the stress time t_{str} , the maximum voltage shift ΔV^{max} and the parameters of the normal distribution μ and σ. ΔV recovery also scales with $\log(t)$ resulting in a crucial dependence on timing parameters. Due to these facts, we present a preconditioned measurement method which minimizes the impact of delay and recovery times on the extracted ΔV.

Experimental Setup

All devices were fabricated on 4H-SiC n-doped substrates using an industrial process. The n-channel MOSFETs received a SiO_2 dielectric on the $(11\bar{2}0)$-plane deposited via chemical vapor deposition. Post oxidation anneal was done in a nitric oxide containing atmosphere for all samples. Measurements are performed on wafer level using an Agilent B1500A parameter analyzer and Agilent E5250A switching matrix at room temperature unless otherwise stated.

Results and Discussion

The consequences of measurement delay times. Fig. 3 shows a typical delayed JEDEC-like measurement pattern (JEDd) used in industrial BTI measurements. The pattern consists of a gate voltage V_G sweep for the subsequent calculation of ΔV, a reference readout R_0 at the readout voltage V_G^{rec}, a stress cycle at the stress voltage V_G^{str} for the stress time t_{str}, a delay cycle at $V_G = 0$ V for the delay time d and a readout R_i at the readout voltage V_G^{rec} for the recovery time t_{rec}. Especially in industrial BTI measurements, delay times of 1 to 10 h between the end of the stress and R_i are always present since the stress cycle is usually done in high-temperature furnaces to accelerate degradation, whereas the readouts are done at room temperature outside the furnace in series for multiple devices. The impact of d on ΔV is shown in Fig. 4 for multiple devices subjected to identical positive stress according to JEDd. Delay time varies from 0 s to 30 s. We observe decreasing ΔV for increasing delay times. The explanation for the increased recovery is shown in the inset of Fig. 4. During the stress cycle, ΔV increases with t_{str} according to Eq. 2 (inset, red). By directly switching to V_G^{rec} without any delay (d = 0 s), ΔV follows the blue recovery curve. Introducing a delay at $V_G = 0$ V results in increased recovery (inset, dashed black) because recovery depends on the Fermi level position. A subsequent bias change back to V_G^{rec} leads to a superposition of charge capture at V_G^{rec} (rising edge) and ongoing recovery. As can be seen, the delayed recovery curve ends up at less ΔV than the non-delayed trace. This increased recovery effect scales with delay time showing that the delay phase at 0 V clears a fraction of the recoverable ΔV component. The clearing characteristic of the delay pulse increases by using an accumulation pulse instead of just 0 V (dashed lines). In

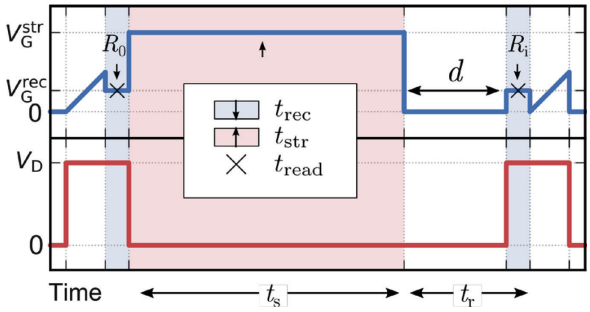

Fig. 3. JEDEC-like bias temperature instability measurement with delay d between stress cycle and ΔV_{th} readout R_i.

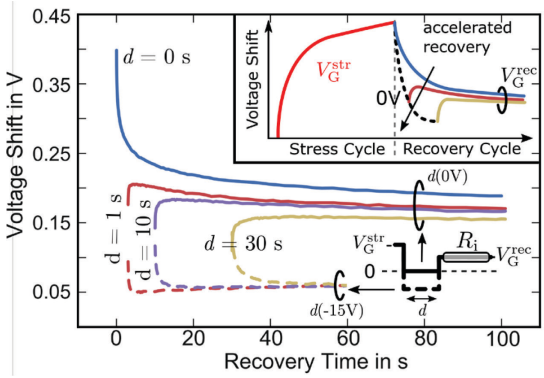

Fig. 4. Impact of the delay on ΔV_{th} recovery behavior for varying d at $V_G = 0$ V (solid lines) and $V_G = -15$ V (dashed lines).

Fig. 4 an accumulation clearing pulse of −15 V was used for the same range of delay times resulting in a decrease of ΔV from 175 mV to 60 mV after 60 s.

Preconditioned BTI. As shown in Fig. 4, JEDEC-like BTI measurements show varying recovery curves depending on the exact bias and timing conditions of each ΔV readout for identical bias stress. This is due to two essential facts: First, extracted ΔV depends on the reference readout R_0 timing and preceding gate voltage since thermal equilibrium is not reached within the measurement time. Second, the way the readouts R_i are performed usually differs from the initial readout R_0. For example, in the JESD 241 standard [6], R_0 is monitored after the end-of-sweep voltage whereas each subsequent readout is done after applying the stress voltage. This difference alone already results in a different interface charging state and therefore leads to an offset in ΔV which is independent of the stress pulse itself.

To overcome bias and timing dependent variations of ΔV, we propose an optimized measurement pattern using preconditioning. Fig. 5 shows the impact of various readout patterns on ΔV after a 1 ks positive bias stress (STR). As reference for the calculation of ΔV we either use the sweep (SWE) itself, a bias switch from 0 V to V_G^{rec} (JED0) or preconditioned readout (PRE0) with a -15 V accumulation pulse for 1 s. After STR, readout is preformed according to JESD 241 via switching directly to V_G^{rec} (JED1) or via preconditioning similar to PRE0 (PRE1). Each ΔV recovery trace in Fig. 5 is given in relation to one of the reference readouts which is indicated by the minus sign. For the JEDEC-like readout JED1-JED0 (dashed blue), ΔV recovers from ~500 mV to ~100 mV within 10 ks recovery time after STR. ΔV recovery changes drastically by using preconditioned readout. The solid and dashed green curves represent ΔV before (PRE0) and after (PRE1) STR. Since both readouts are performed under strictly identical switching conditions and show the same recovery trend, recovery behavior mainly depends on the switching conditions and is nearly independent of STR. The difference between both curves (PRE1-PRE0) gives the offset-free ΔV caused by STR and is indicated in red and almost constant at 35 mV. This value gives a good estimation of the permanent component of ΔV and can be reliably measured no matter if the delay is as short as 20ms or as long as 3 hours.

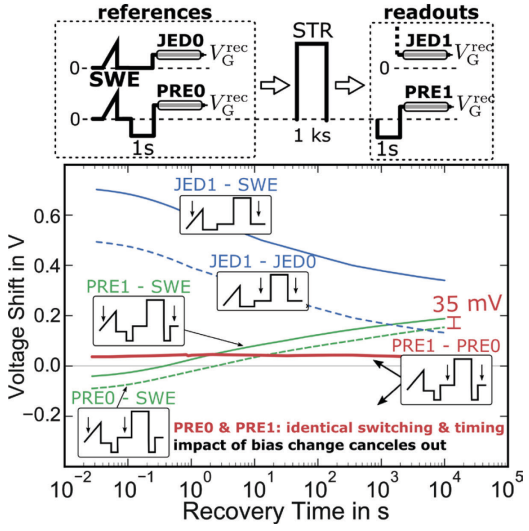

Fig 5. Top: switching variations for ΔV calculation. Bottom: ΔV resulting from chosen readout-reference combination.

Hysteresis Monitoring. To enable monitoring of hysteresis (SH) effects [7] during high temperature gate stress, the accumulation pulse readout is extended via a second inversion preconditioning pulse at use-voltage (see Fig. 6). SH before the stress is given by p0-n0, whereas SH after the stress is given by p1-n1. The change in SH due to BTI is therefore given by ΔSH = (p1-n1) – (p0-n0).
Fig. 7 (top) shows a comparison of JESD 241 (JED, circles) and preconditioned BTI after a 1 s acc. pulse (nPRE) and after a succeeding 1 s inversion pulse (pPRE) for a 40 h, $V_G^{str} = 2.3\ V_G^{use}$ positive bias stress at 150°C. For JED, ΔV is overestimated due to the offset induced by the different switching conditions. PRE measurements result in ~2 times lower and more accurate ΔV. The difference between nPRE and pPRE results from the hysteresis (red squares) which slightly increases during high-T positive bias stress. In addition to the offset-free extraction of ΔV, PRE allows for nearly delay time independent measurements. Fig. 7 (bottom) shows the impact of the delay time at $V_G = 0$ V. Between $d = 1$ s and $d = 10\ ks$, ΔV decays from 520 mV to 290 mV for JEDd, and from 190 mV to 160 mV for PRE allowing for nearly delay time independent extraction of ΔV.

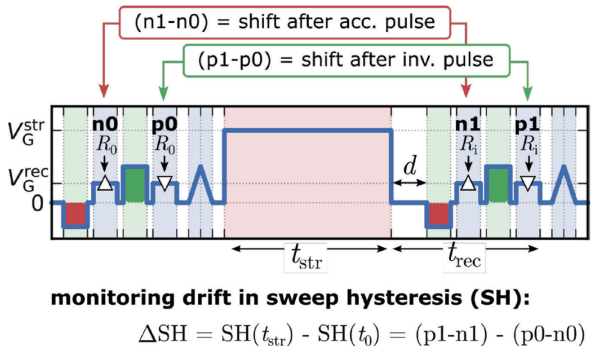

Fig. 6. Preconditioned BTI measurement PRE with accumulation and inversion pulse preconditioning allowing for additional hysteresis monitoring.

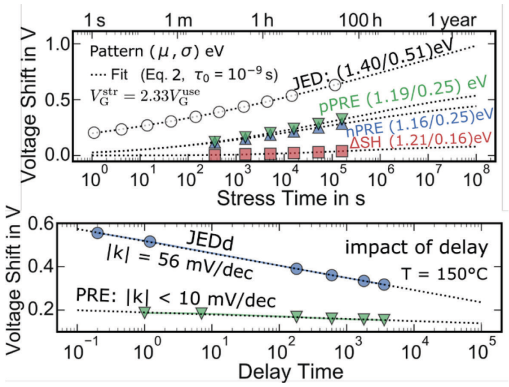

Fig. 7. Top: ΔV for t_{str} up to 40h for JESD 241 and PRE under identical stress. Fit is done according to Eq. 2. Bottom: impact of d on ΔV for JESD241 and preconditioned BTI.

Summary

We investigated the impact of various BTI measurement parameters on the extracted voltage shift of 4H-SiC power MOSFETs. Using JEDEC-like measurements, the majority of ΔV originates from recoverable and stress independent shift components solely defined by varying timing and switching parameters of each ΔV extraction point. To overcome this issue and provide identical switching conditions, we demonstrate a sophisticated BTI measurement pattern using well defined preconditioning pulses prior to each ΔV extraction point. Using this technique, shift components originating solely from the bias change cancel out allowing for accurate extraction of the permanent ΔV component induced by the stress pulse. Voltage shifts extracted via preconditioned BTI are less dependent on measurement delay times within industrial timescales and do not include the impact of fully-recoverable hysteresis effects. Therefore, only this approach enables an accurate lifetime prediction of 4H-SiC MOSFETs.

Acknowledgement

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