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Characterization of charge trapping phenomena at III–N/dielectric interfaces

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ABSTRACT

Charge trapping related phenomena are among the most serious reliability issues in GaN/AlGaN MIS-HEMTs technology. Today, many research efforts are undertaken to investigate and identify the defects responsible for device degradation. This work focuses on the trap sites located close to the interface with the dielectric, which are responsible for large voltage drifts in on-state conditions. We study the response of GaN/AlGaN/SiN systems to small and large signal excitation. Measurements performed with a lock-in amplifier enable us to deeply understand the dynamic behavior because of the improved time resolution and the versatility of the instrument. We investigate the frequency dispersion and the hysteresis of these devices and conclude that direct analysis of impedance characteristics is not sufficient to extract information about the interface trap response. We propose a methodology to study trapping phenomena based on transient measurement analysis, describing the approximations made and their effect on the accuracy of the result. Results on MIS test structures confirm the existence of a broad distribution of trap states. Capture time constants are found to be uniformly distributed in the experimental time window between 50 μs and 100 s.

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1. Introduction

In the past years the interest of semiconductor industry and scientific research for wide-bandgap materials has grown consistently. The superior material parameters with respect to silicon will allow a series of significant improvements in different fields, from power electronics to high frequency switching applications.

A number of technological as well as reliability issues have to be investigated and understood. In some cases, untangling the problem requires the development of accurate methods which take the novel challenges and properties of such new materials into account. One of the major research topics of GaN-based device reliability is charge trapping during operation. This phenomenon plays a key role in the degradation of HEMTs (high electron mobility transistors) and MIS-HEMTs (metal-insulator-semiconductor HEMTs) performance. The two main fields of study are defects in the intrinsic (bulk) material [1–3] and the ones arising at interfaces between different layers [4–7]. The former case regards contaminants, dislocations, lattice irregularities and the effect of dopants; the latter imperfections located in the transition layer between one material and the next one (interface traps), or very close to it (near-interface traps).

The object of this work is to investigate charge trapping mechanisms at or near the interface between GaN-based semiconductors and dielectrics. Special attention is paid to the properties of such systems, especially to composite GaN/AlGaN structures. Research carried out in the past years has unveiled many details about the degradation mechanism during operation (performing continuous or pulsed stress-recovery experiments) [4,8] and the response of devices to small signal excitation (frequency dispersion, analysis of impedance characteristic) [9,10]. The aim of this work is to combine these two aspects, by investigating the role of large and small signal excitation. We will therefore develop a comprehensive methodology for the experimental characterization of device instabilities. Starting from the first results on GaN/AlGaN/SiN MIS-HEMTs [11], we thoroughly study the device impedance characteristics, with special attention to measuring modalities. Furthermore, we examine in depth the techniques for calculating the amount of trapped charge at the interface during forward gate bias stress introduced in [11], the *measurement-stress-measurement* and the *on the fly* approaches. We establish a setup for impedance measurement based on a lock-in amplifier, and we optimize it in order to measure fast transients after the application of a stress voltage to the devices under test (time resolution in the order of

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μs). Finally, we show the comparison of devices with and without an additional Si-doping layer buried in the GaN buffer. This example makes the limitations of one of the techniques clear, therefore proving the importance of an exhaustive understanding of all concurrent degradation mechanisms of the device, and their impact on the characterization method in use.

2. Experimental details

The test structures under investigation in this work are on-wafer GaN/AlGaN/SiN MIS structures, grown on a silicon substrate. A 25 nm thick AlGaN layer with 25% of aluminum content is grown on the GaN surface, on top of which a 50 nm thick SiN layer is deposited. The metal contact is made of aluminum. Throughout this paper we use devices with two different kinds of substrate. The first wafer has an additional Si-doped GaN (10^{18} cm^{-3}) layer inserted 100 nm deep into the unintentionally doped (UID) GaN, as shown in Fig. 1a. We have studied this sample and compared it to similar structures without the AlGaN layer in [11]. The second wafer instead has only a 300 nm thick UID GaN layer above the carbon-doped buffer.

Both GaN and AlGaN are polar materials, characterized by an intrinsic spontaneous polarization field. Furthermore the lattice mismatch between the two causes a piezoelectric field in the strained AlGaN layer. The result of the discontinuity of the polarization field at the interface is the formation of a two dimensional electron gas (2DEG). Fig. 1 illustrates the position of the localized electrons (a) and the band diagram (b). For this reason composite GaN/AlGaN devices are normally on: Fig. 1c shows the transfer characteristic of a HEMT and the capacitance–voltage (CV) curve of a MIS; note the negative value of the threshold voltage.

In order to investigate the behavior of the test structures under both small and large signal excitation, we perform impedance measurements. We apply a large signal (DC) bias to bring the device to the desired state (stress, recovery) and an oscillating small signal (AC) to obtain its small signal response. Impedance measurements are performed with a standard Agilent 4294A impedance analyzer and with a Zurich Instruments HF2LI lock-in amplifier. The versatility of the lock-in amplifier allows a deeper insight into the impedance properties of the devices under test, as discussed in detail in the next section.

3. Impedance measurement with the lock-in amplifier

Lock-in amplifiers are versatile instruments used to measure signals with a known carrier wave. They provide reliable results even if the noise is few order of magnitudes larger than the signal. The ratio between the amplitudes of the largest tolerable noise and the detected signal, expressed in decibel (dB) is called dynamic reserve. In our case, this is typically 100 dB [12], which means we are able to measure a periodic signal ten thousand times smaller than the noise at other frequencies. In the next paragraphs we briefly summarize the core of the lock-in amplifier working principle, the phase sensitive detection (PSD) and we describe how the instrument can be used for advanced sampling measurements.

3.1. Phase sensitive detection (PSD)

The lock-in amplifier needs a reference signal, which can be provided from an external function generator, or from its internal oscillator. In our setup, illustrated in Fig. 2, the reference signal $\widetilde{V}_{\mathrm{ref}}(t)$ is a sinusoidal wave with amplitude $\sqrt{2}$V, whose frequency can be customized. The typical value in this work is 10 kHz. The maximum frequency for reliable measurements is limited by the cables and probes contacting the device at the wafer probe station: in our case the limit is 1 MHz because standard DC probes are used.

The output signal is used as the excitation to the device under test (DUT). It has the same frequency as the reference signal and customizable amplitude, tipically 500 mV. An auxiliary output allows to change its DC bias baseline, V_{DC}. The response of the DUT is amplified with a current to voltage converter and then digitized into the measured signal $\widetilde{V}_{\mathrm{sig}}(t)$. Generally it will have the same frequency as the excitation signal, but a different phase θ_{sig}. The phase sensitive detector mixes the measured signal and the reference twice, with a phase shift of $\theta_{\mathrm{ref}} = 0$ and $\theta_{\mathrm{ref}} = 90°$. The analog multiplier introduces the coefficient $k = 1\ \mathrm{V}^{-1}$. Indicating the amplitudes and frequencies of the two signals with $V_{\mathrm{ref}} = \sqrt{2}$ V, V_{sig} and $\omega_{\mathrm{ref}}, \omega_{\mathrm{sig}}$ respectively, the result is

$$\begin{aligned} k \times \widetilde{V}_{\mathrm{sig}} \times \widetilde{V}_{\mathrm{ref}} &= k \times V_{\mathrm{sig}} \sin(\omega_{\mathrm{sig}} t + \theta_{\mathrm{sig}}) \times V_{\mathrm{ref}} \sin(\omega_{\mathrm{ref}} t + \theta_{\mathrm{ref}}) \\ &= k \frac{V_{\mathrm{sig}} V_{\mathrm{ref}}}{2} \cos\left((\omega_{\mathrm{sig}} - \omega_{\mathrm{ref}})t + \theta_{\mathrm{sig}} - \theta_{\mathrm{ref}}\right) + \\ &\quad - k \frac{V_{\mathrm{sig}} V_{\mathrm{ref}}}{2} \cos\left((\omega_{\mathrm{sig}} + \omega_{\mathrm{ref}})t + \theta_{\mathrm{sig}} + \theta_{\mathrm{ref}}\right). \end{aligned} \tag{1}$$

If the frequency of the two signals is the same, the result is a DC component which is proportional to the signal amplitudes, and an additional component at frequency 2ω. This operation is called *homodyne detection*. The aim of the lock-in amplifier is to shift the spectrum of the demodulated signal to base band, *i.e.* as close to DC as possible. In this way, the desired $\widetilde{V}_{\mathrm{sig}}(t)$ amplitude is found

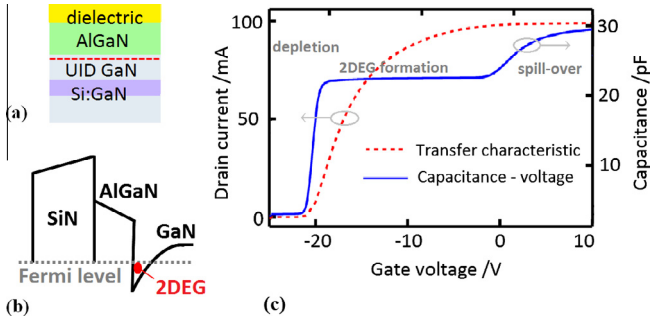

Fig. 1. (a) Schematic cross-section of the test structures. The red dashed line shows the position of the two-dimensional electron gas (2DEG). (b) Band diagrams (conduction edge only): the GaN/AlGaN structure is normally-on. (c) Typical transfer characteristic of a MIS-HEMT and a MIS CV curve of devices with Si-doping. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

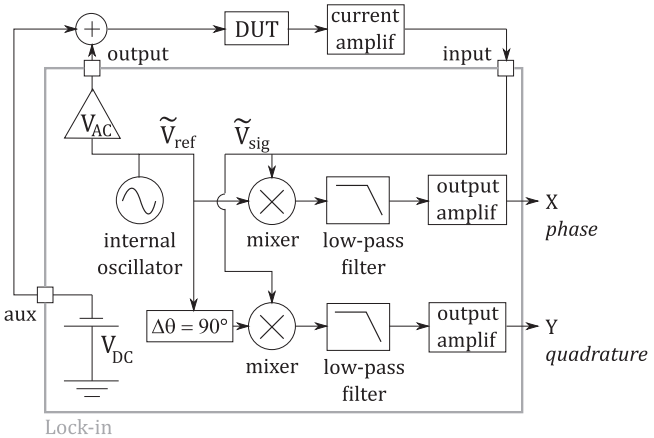

Fig. 2. Schematic illustration of the lock-in amplifier setup.

by filtering out the high-frequency component with a digital low-pass filter. This is equivalent to calculate the average of the demodulated signal: for $\theta_{ref} = 0$ and for $\theta_{ref} = 90°$, respectively

$$k\,\langle \widetilde{V}_{sig} \times \widetilde{V}_{ref} \rangle = k\,\frac{V_{sig} V_{ref}}{2} \cos\theta_{sig} = \frac{V_{sig}}{\sqrt{2}} \cos\theta_{sig} = X$$
$$k\,\langle \widetilde{V}_{sig} \times \widetilde{V}_{ref} \rangle = k\,\frac{V_{sig} V_{ref}}{2} \sin\theta_{sig} = \frac{V_{sig}}{\sqrt{2}} \sin\theta_{sig} = Y. \quad (2)$$

The lock-in amplifier outputs are two values which describe the complex vector $Re^{i\phi} = X + iY$. In polar coordinates, R is the amplitude $V_{sig}/\sqrt{2}$, which is the amplitude of the signal $\widetilde{V}_{sig}(t)$ in V_{rms}, and ϕ is its phase θ_{sig}. In cartesian representation the real and imaginary parts X and Y, in V_{rms}, are called *phase* and *quadrature* respectively, as they represent the part of the signal in phase and out of phase with respect to the reference.

3.2. Sampling measurement

In sampling measurements the time resolution is given by the sampling rate of the instrument, which can be as high as 210 MSa/s for the Zurich Instruments HF2LI used here. According to Nyquist's principle, it must be at least twice the maximum signal frequency in order to avoid aliasing. An important figure for the measurement accuracy is the time constant (TC) of the digital filter. A trade-off must be found between high signal to noise ratio (large TC) and fast sampling (small TC). The choice must be made keeping in mind the time response of the filter: some time is needed until the correct final value is reached, as shown in Fig. 3. This takes a multiple of the TC depending on the filter order. This is due to their different roll-offs, *i.e.* the slope of their transfer functions. If the measurement starts before the settling time of the filter, the result will be a convolution of the signal with the filter time response. In the following a 4th order filter is used, which has a roll-off of 24 dB/octave. The filter needs ten times the chosen TC to reach 99% of the correct measurement value [12]. With a typical time constant of 5 µs, the time resolution is therefore approximately 50 µs.

In order to achieve the best time resolution in measuring the impedance transient we start sampling with the maximum sampling rate just before the trigger is sent to the auxiliary output. Recording the auxiliary bias as well, it is possible to set the measurement time to zero in correspondence of the actual start of the excitation, with a step detection algorithm implemented in the measuring software. During the rest of the experiment the sampling rate is constantly adjusted so that we record approximately logarithmically spaced samples in time.

3.3. Impedance measurement

The complex vector obtained from the lock-in amplifier can be transformed into the capacitance and conductance of the DUT. Its relationships with the complex impedance measured between the two terminals, Z_m and the complex admittance Y_m are

$$Z_m = \frac{\widetilde{V}_{output}}{\widetilde{I}_{input}} = -\frac{R_G V_{AC}}{\widetilde{V}_{sig}} = -\frac{R_G V_{AC}}{R}\, e^{-i\phi}$$
$$Y_m = \frac{\widetilde{I}_{input}}{\widetilde{V}_{output}} = -\frac{\widetilde{V}_{sig}}{R_G V_{AC}} = -\frac{X}{R_G V_{AC}} - i\frac{Y}{R_G V_{AC}}, \quad (3)$$

where R_G is the total gain of the input current amplifier and V_{AC} is the amplitude of the sinusoidal excitation in V_{rms}. Assuming a parallel capacitance–conductance model for the DUT, the desired values C and G can be calculated as

$$G = \mathcal{R}e\{Y_m\} = -\frac{X}{R_G V_{AC}}$$
$$C = \frac{\mathcal{I}m\{Y_m\}}{\omega} = -\frac{Y}{\omega R_G V_{AC}}. \quad (4)$$

If needed, the parasitic components introduced by the cables and fixtures can be corrected in the following way: two measurements with open and shorted terminals allow to determine the residual impedance Z_s and the stray admittance Y_0. The actual measured impedance is the admittance of the DUT in parallel with the stray admittance and in series with the residual impedance:

$$Z_m = Z_s + \frac{1}{Y_{DUT} + Y_0}. \quad (5)$$

Fig. 4 shows the capacitance–voltage curve of a GaN/AlGaN MIS structure measured with the lock-in amplifier, with and without the parasitic component correction. There is good agreement with the measurement performed with the impedance analyzer.

4. Impedance characteristic of GaN/AlGaN MIS devices

Capacitance and conductance characteristics provide an insight into the device behavior when a gate bias is applied. It is possible to distinguish three main regions, as indicated in Fig. 1c: (i) depletion, (ii) 2DEG formation and (iii) *spill-over*. When the gate bias is below the threshold voltage, it is possible to completely deplete the polarization induced electron layer. At further negative values a depletion region extends into the GaN, according to its doping concentration. Because of the large generation time constant for minority carriers (holes), an inversion layer cannot be created. For this reason we neither observe the saturation of capacitance at high frequency, nor an increase to the dielectric capacitance at

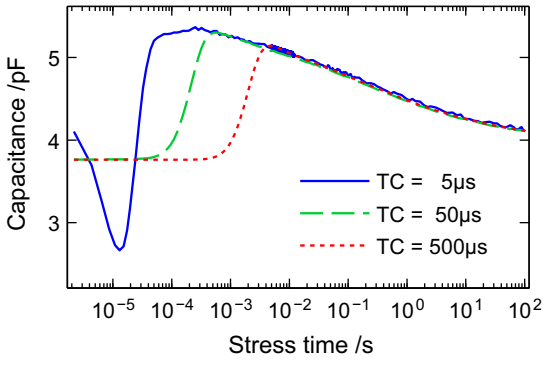

Fig. 3. The measured transient is the convolution of the filter response with the actual signal from the DUT. A fourth order filter needs ten times the TC in order to achieve the correct value with 99% accuracy.

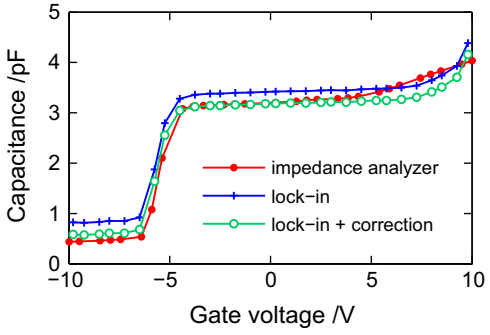

Fig. 4. Capacitance–voltage characteristic of devices without Si-doping taken with the impedance analyzer and the lock-in amplifier, before and after the correction for the parasitic components.

low frequency as in silicon: we have always a *deep depletion* curve. Above the threshold voltage, the channel forms at the GaN/AlGaN interface. The capacitance value is the series of the capacitances of the AlGaN and of the dielectric layer. This region includes zero gate bias conditions. At positive gate bias, the CV curve increases up to the dielectric capacitance. This means that electrons from the 2DEG found their way to the AlGaN/dielectric interface, being transported through the AlGaN barrier. This part of the characteristics depends on the excitation signal frequency, as shown in Fig. 5a and b for both wafers under investigation. The two samples behave in a similar way, for this reason in the following we report the results on the Si-doped wafer only, if not indicated otherwise. The conductance characteristics show the behavior of displacement currents in the system depending on the applied bias. In Fig. 5c and d two peaks are visible: the one at negative voltage corresponds to the depletion and formation of the 2DEG, the other is due to the frequency dependent transfer of electrons to the interface with the dielectric.

The AlGaN layer behaves as an insulator until the gate bias reaches a threshold called *spill-over voltage*, when it becomes conductive. Fig. 6a shows the model associated with such behavior: a capacitor in series with a bias-dependent resistor [13]. Such an RC branch gives rise to a certain time response: for this reason the values of the device capacitance measured at different frequencies differ from each other. This model alone explains the observed frequency dispersion and the change in position of the spill-over voltage [14]. Fig. 6b schematically illustrates the band diagram before and after spill-over regime. The spill-over voltage is large enough to bring the AlGaN conduction band edge at the interface with the dielectric below the Fermi level, thus creating the conditions for the formation of a second electron channel.

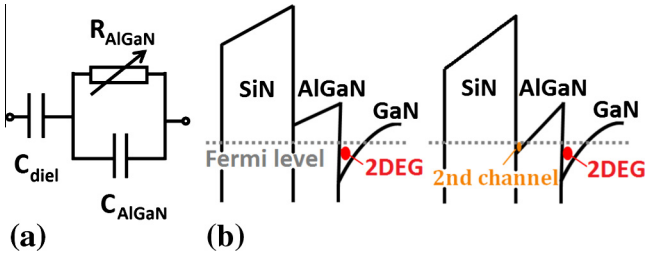

Fig. 6. (a) Circuit diagram model of the composite GaN/AlGaN MIS structure. (b) Band diagrams before (left) and after (right) spill-over conditions.

The most appropriate way to determine the onset of spill-over is to perform a quasi-static CV curve. This method evaluates the device capacitance by applying a small, linear increase of voltage to the gate. In this way, the displacement current in the MIS structure is directly measured. This current is proportional to the incremental capacitance of the MIS structure. The capacitance is calculated by integrating the current over time, after subtracting the leakage current. The experimental curves are shown in Fig. 5a and b. This measurement provides the smallest value for the spill-over voltage, because the charging of the second channel is measured directly. The test structures with and without Si-doping are in spill-over conditions from about −4 V and 1 V, respectively.

With such understanding of the response of the device to small signal excitation, it is clear that the methods developed for silicon to extract the density of interface states cannot be applied to composite GaN/AlGaN structures. These techniques rely on the direct analysis of CV curves in the limit for high or low frequency

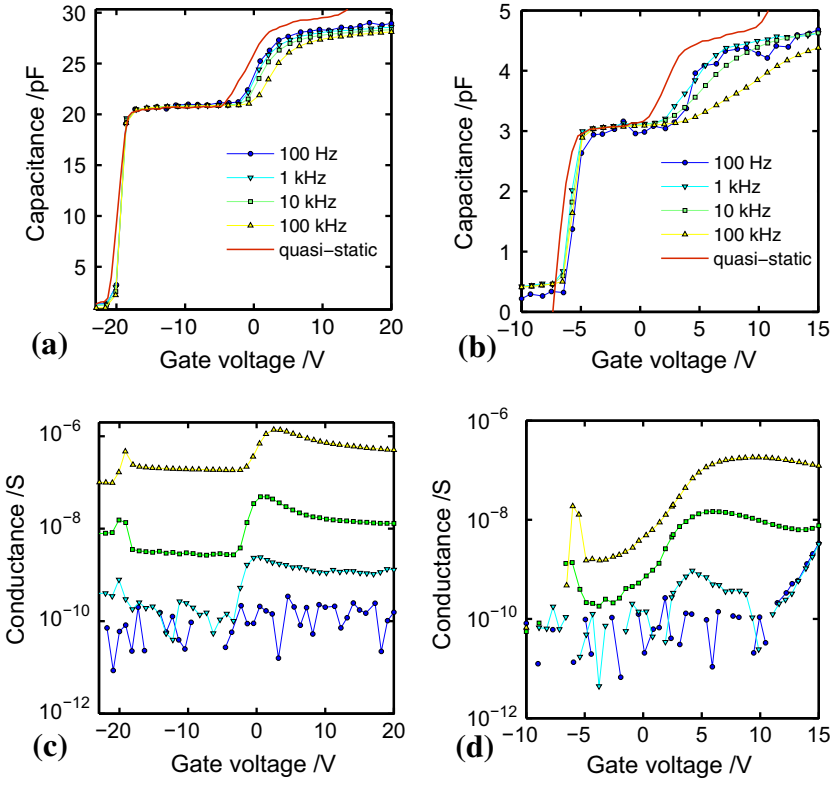

Fig. 5. (a) Frequency dispersion of the CV curve for GaN/AlGaN/SiN MIS on the wafer with Si-doping. The CV curves at various frequencies are taken with the impedance analyzer; a comparison with a quasi-static CV is shown. All curves have the same sweep rate. (b) CV curves on devices without Si-doping. (c) Conductance characteristics at various frequencies on the wafer with and (d) without Si-doping.

[15–17], or on the frequency dependence of the conductance [18]. The basic concept for all of them is to model the contribution of interface states as an admittance in parallel with the semiconductor depletion region capacitance. Only under such assumption the impedance characteristic dependence on frequency can be entirely attributed to charge trapping. However, in this way the response of the AlGaN barrier layer is completely neglected, while its contribution to charge trapping dynamics has been confirmed [13,19]. Furthermore, all of these techniques assume the validity of the Shockley–Read–Hall (SRH) model [20,21] in order to extract the distribution of trap states over the dielectric bandgap [9]. Stress and recovery investigations on GaN/AlGaN MIS-HEMTs provided evidence that a more complete trapping model is necessary to fully explain the experimental observations [13].

Alternative methods have been developed on silicon MOSFETs to investigate the negative bias temperature instability (NBTI), in particular stress-recovery experiments [22]. The fundamental idea is to evaluate the time dependence of the drain current transients when the gate bias is applied or changed. From the evolution of the drain current under forward gate bias the distribution of traps near the Si/SiO_2 interface is extracted. Further experiments give an insight into the role of temperature and contaminants, and simulations provide evidence that such transitions cannot be explained with the SRH model [23]. An exhaustive treatment of the physics of the Si/SiO_2 system can be found in literature [24]. The choice of an alternative method for GaN/AlGaN MIS structures has the additional benefit of being free of any assumption on charge exchange, like the SRH model. We propose the evaluation of charge trapping at the interface by measuring the time evolution of the device capacitance in spill-over conditions. Since most electrons are located at the AlGaN/dielectric interface and are screening the 2DEG, changes over time can be interpreted as the drift of the whole capacitance curve due to charge trapping.

Another important property of GaN-based MIS CV curves is their strong hysteresis behavior. Fig. 7a shows the characteristic of a number of fresh devices, starting from zero gate bias to various values in reverse or forward direction. The green curves are the starting sweep, other colors indicate the return sweeps as indicated by the arrows. We clearly see hysteresis along the whole gate bias axis, towards left for negative bias (red color scale) and towards right for positive bias (blue color scale). Furthermore, Fig. 7b shows the effect of repeating cycles of sweeps in the two directions between 0 V and 10 V: the higher the number of cycles, the larger the shift to the right of the final CV curve. If the same device is now used for the same experiment after few minutes in floating conditions (labeled "stressed" in Fig. 7b), we see that its initial CV curve remains shifted to the right with respect to the fresh one. The final CV curve instead is close to the previous one, reaching some sort of saturation. However, the position of the CV curve after many cycles depends on the value of the maximum voltage reached during the sweep, in this example 10 V.

In summary, the CV curve depends heavily on the measurement parameters. This means that any defect characterization method based on the direct analysis of the impedance curve gives different outcomes depending on the sweeping modalities. This is a further argument in favor of an alternative approach to charge trapping investigations. The impact of measurement conditions on impedance curves must be taken into account in characterizing the device as well as in evaluating the effect of gate bias stress, as discussed in the next section.

5. Evaluating interface trapped charge

When a trapping event occurs, a certain amount of charge $Q_{trapped}$ is captured at defect sites. The electrostatics of the MIS structure change accordingly. The applied bias at the gate V_{GB} is distributed throughout the device as

$$V_{GB} = V_{FB} + \phi_{GaN} + \phi_{AlGaN} + \phi_{diel}, \tag{6}$$

where $\phi_{GaN}, \phi_{AlGaN}, \phi_{diel}$ are the potential drops at the GaN surface, at the AlGaN/dielectric interface, and through the dielectric layer respectively. The flat-band voltage V_{FB} differs from the ideal value V_{FB}^0 by the amount of trapped charge, assuming $Q_{trapped}$ to be located at the interface with the dielectric

$$V_{FB} = V_{FB}^0 - \frac{Q_{trapped}}{C_{diel}} = V_{FB}^0 - \Delta V_{FB}, \tag{7}$$

where C_{diel} is the dielectric capacitance. Therefore, we can interpret the degradation due to charge trapping phenomena as a shift of the flat-band voltage ΔV_{FB}. Because of its linear dependence on the amount of charge captured by interface or near-interface states, this quantity and its dependence on time, applied bias and other parameters is the key to understand the mechanisms of charge trapping. We focus hereinafter on the experimental methods to evaluate the voltage drift, indicated as ΔV_{FB} or simply as ΔV.

5.1. Measurement-stress-measurement (MSM) technique

Even if the device characteristics depend on the measurement parameters, it is possible to compare CV curves before and after stress, provided that they are taken exactly in the same way. This

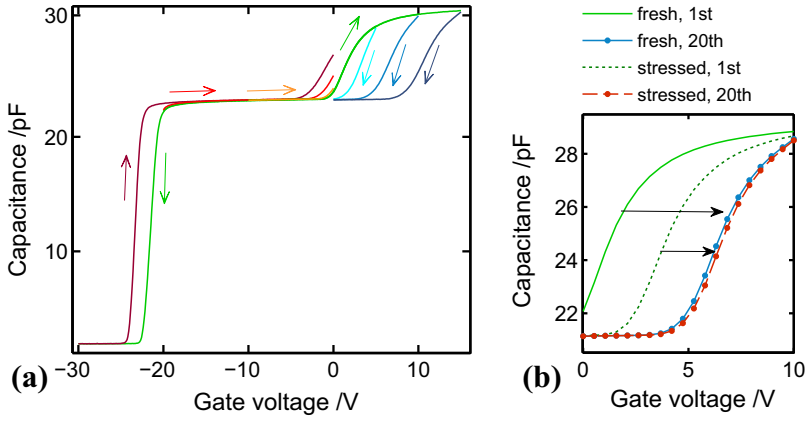

Fig. 7. (a) CV curves show hysteresis in the whole gate bias range. (b) Repetitive cycles between 0 V and 10 V, for a fresh device and after few minutes in floating conditions. Only the first and the last curves are reported.

approach is called *measurement-stress-measurement* (MSM) [25]. The goal is the extraction of the voltage drift ΔV from couples of capacitance or conductance curves like the ones shown in Fig. 8a and b. The difference between stressed and fresh curves (Fig. 8c) is different from zero in two separate regions, corresponding to the transitions from depletion to the 2DEG formation (C_1 and G_1), and from there to spill-over (C_2 and G_2).

The relative horizontal shift shown in Fig. 8d as a solid line is calculated in the following way: for each measured gate bias point, the corresponding capacitance is chosen from the fresh curve. The same capacitance value is found on the stressed curve, and the relative gate bias is interpolated. The ΔV is the difference between the two gate bias values. Furthermore, the voltage drift from the conductance data is extracted as the difference in the stressed and fresh peak positions. Fig. 8d also shows the amount of charge trapped at interface states after stress. We indicate this quantity with ΔN_{it}, which is calculated from Eq. (7) as

$$\Delta N_{it} = \frac{Q_{trapped}}{q} = \frac{C_{diel}}{q}\Delta V. \quad (8)$$

We observe that capacitance and conductance curves give the same information about drift in the first region: here a parallel shift of the two curves occurs. Interestingly, the ΔV from the CV curve in the second region is not completely uniform with gate bias, but it has a rising and falling behavior, the ΔV from conductance peak being its average value. This is the result of the CV curve distortion after stress. When the charge state of interface states changes due to stress, the second CV curve can show a different response to the large signal sweep than before. This effect is usually smaller than the frequency dispersion; the case shown here is for a rather high stress level of 10 V.

Because of the strong hysteresis behavior and the difficulty in returning to initial conditions (very slow recovery in floating conditions and drift in the opposite direction when applying negative bias) two devices are needed for the two curves. However, device to device variation is small enough for the test structures we are considering, as shown by the voltage drift after a transient of 100 s at 0 V, shown in Fig. 9a. This holds true for various choices of sweeping parameters as frequency, small signal amplitude, sweep rate and DC bias extrema. This also proves that the application of a small signal alone does not wear out the device. For this reason, we can continuously measure the impedance value during the stress transient at constant DC bias.

Further experiments are carried out again with different measurement parameters. While varying the small signal properties the result does not change, differences are observed when changing sweep rate and voltage extrema values. The extracted ΔV values can vary up to 40% if the sweep rate is increased ten times, or if the starting gate voltage is −10 V rather than −30 V, as reported in Fig. 9b. This result proves not only that the impedance characteristics change with the sweep parameters, but also that the influence of the sweep can be larger than a stress transient at the rather high level of 10 V for 100 s.

It is therefore necessary to perform the CV measurement in a way such that it does not conceal the effect of stress. We observe that the calculated ΔV becomes smaller the longer a negative bias is applied. This is due to the fact that negative bias is a recovery condition after forward bias stress. In fact the voltage drift, which reaches its maximum value at the end of stress, decreases suddenly as soon as the gate bias changes. This makes the measurement challenging. A solution is to optimize the sweep starting value V'_G to a voltage in the proximity of the interesting region C_1, as sketched in Fig. 10a. In this way, the device remains at negative gate bias conditions for the shortest time possible. Such delay depends on the instrument capabilities: for the impedance analyzer it is 250 ms, for the lock-in amplifier it can be as low as 50 ms. For this reason, the voltage drift measured with the MSM method is an underestimation of the real value.

Fig. 11a shows the ΔV extracted from lock-in measurements with different time delay. The effect of waiting more or less time while the bias is applied results in a variation of the drift value of less than 10%. This is again the effect of the additional recovery, but in this case the optimization of the sweeping mode leads to a more accurate result. This highlights the importance of choosing the measurement parameters which have the least influence on the device characteristics.

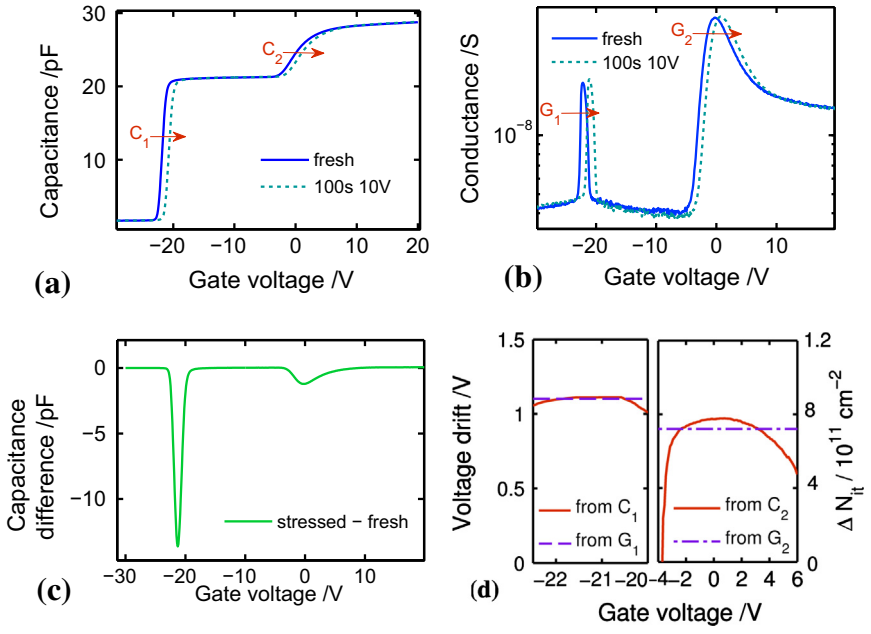

Fig. 8. Impedance characteristics before and after 100 s at 10 V: (a) capacitance and (b) conductance. (c) The difference between stressed and fresh curves determines the two regions of interest. (d) Voltage drift calculated in the C_1 and C_2 regions: from capacitance curve (solid line) and from the position of the conductance peaks (dashed lines). The corresponding density of traps at the interface ΔN_{it} is shown on the right axis.

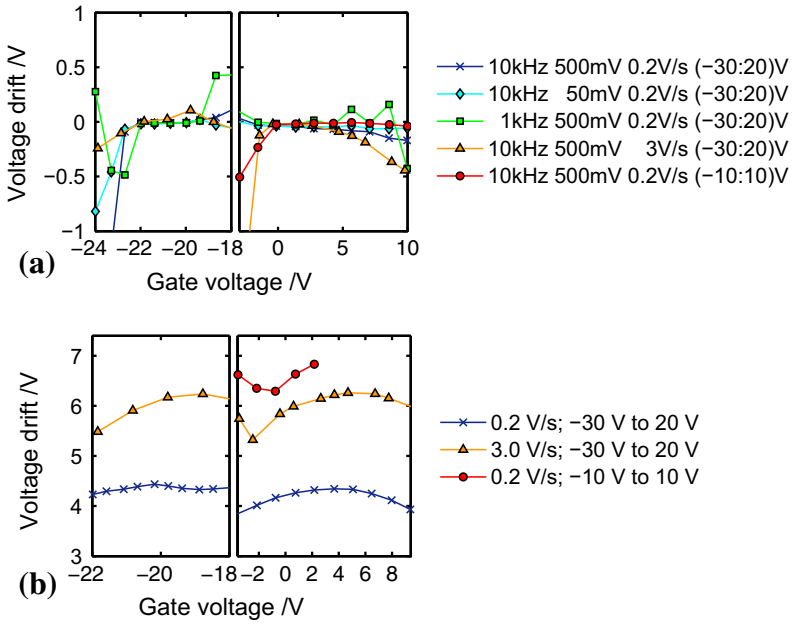

Fig. 9. (a) Voltage drift after 100 s at 0 V for various measurement conditions. The different measurement parameters do not affect the result: ΔV is zero in all cases. (b) The voltage drift after 100 s at 10 V stress varies for different DC bias sweeping conditions (sweep rate and range).

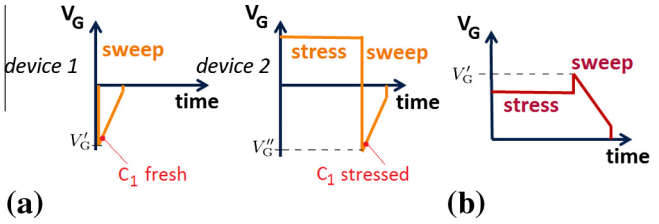

Fig. 10. Schematic representation of transient measurements: (a) MSM: comparison of the capacitance value at C_1 on a fresh device (left) and after stress on another device (right) with the MSM technique, and (b) OTF: impedance stress transient followed by a reference CV characteristic.

Furthermore, also the starting voltage of the sweep after stress V''_G must be carefully optimized. During the stress transient the whole CV curve moves towards positive bias. The capacitance value C_1, measured at V'_G before stress, shifts to the right accordingly. In order to measure at C_1 after stress, the ideal bias value to start the sweep from is $V'_G + \Delta V$. Fig. 11b shows the result with and without V''_G optimization. If the sweep extrema is fixed at −19.5 V the difference between the measured capacitance at the first point and the desired C_1 value is larger, the longer the stress duration. This causes an underestimation of ΔV which is more severe at long stress times, thus resulting in a smaller slope coefficient of the linear relationship between voltage drift and the logarithm of time. For this reason, it is necessary to make sure that the chosen V''_G bias corresponds to the desired C_1 value.

Nevertheless, the unavoidable measurement delay introduces a systematic error intrinsic to the MSM technique. Due to the impossibility to measure instantaneously as soon as the gate bias is switched to the *measurement* phase, which correspond to recovery conditions, the calculated voltage drift is always an underestimation of its real value. This is valid also for investigations on MOSFETs and MIS-HEMTs after on-state stress [25,26]. In fact, in these cases the drain current is read out after the stress transient at a voltage close to the threshold voltage, which is again a recovery condition with respect to a more positive gate bias.

5.2. Capacitance-on the fly (C-OTF) technique

Comparing impedance characteristics before and after stress is not the only way to monitor device degradation. A sampling measurement of capacitance at constant DC forward bias V_{stress} results in a decreasing transient over time. If the stress voltage is large

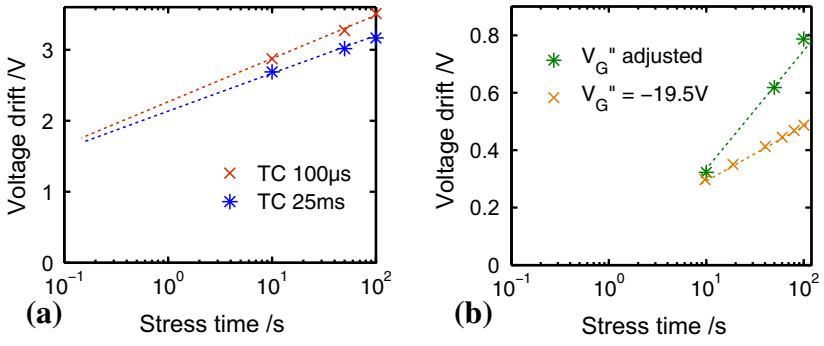

Fig. 11. (a) Voltage drift extracted with the MSM technique with different time delays, namely 1 ms and 250 ms for the two data sets. (b) Voltage drift extracted with always the same $V''_G = -19.5$ V and by optimizing it to the C_1 value.

enough to bring the structure in spill-over conditions, we can interpret the capacitance decrease as a right drift of the CV curve due to charge trapping. From each measured point during stress it is possible to extract the current status of the voltage drift *on the fly* (OTF). A similar technique has been previously used for investigating the threshold voltage drift of silicon MOSFETs under bias temperature instability stress [25,26].

The capacitance transient is directly related to ΔV and $Q_{trapped}$ according to eq. (7). In order to extract the time evolution of the voltage drift a single CV curve is used as a reference. Usually it is recorded just after the stress transient, as sketched in Fig. 10b. The capacitance value at V_{stress} in the CV curve corresponds to the capacitance of the last measurement point of the transient, at t_{stress}. The capacitance at the first measurement point t_0 instead gives the position of the CV curve of the fresh device. For each value t^* in the transient, the correspondent gate bias value is interpolated in the CV curve. It is therefore possible to calculate the ΔV as difference between each interpolated gate voltage points with the first one. This procedure is illustrated in Fig. 12.

The choice of the sweeping mode for the reference CV curve is of course as important as in the MSM case. We must determine the optimal sweep rate, the bias extrema V'_G and the sweep direction to be used. The next paragraph is dedicated to this subject.

5.3. Choice of the reference CV curve

In order to understand the impact of each sweep parameter on the CV curve measurement, some preliminary experiments with the lock-in amplifier are carried out. We apply a staircase pattern as DC gate bias, changing the voltage step by step and holding it for a period T. From the measured transients at each bias, the capacitance is chosen as the value at the time t_{extr}. In this way we can build the CV characteristics point by point.

Fig. 13a shows the result of choosing a shorter or longer duration for each bias step, while t_{extr} is always 100 µs. Since the gate biases used are always in forward direction, at each step the right drift increases with time. Therefore, CV curves taken with sweeps in both directions (*up* and *down*) are shifted towards more positive bias with increasing step duration.

Fixing now T to 1 s and changing the extraction time, we observe the opposite behavior in the sweeps of opposite direction (Fig. 13b). If the gate bias is increasing (*up* sweep) capacitance decreases with time. The effect of waiting more time to extract the capacitance value results in a right drift of the whole characteristic, because of electron capture. Such drift increases from the first to the last measurement point, thus resulting in a distortion of the CV curve. When the voltage staircase starts from a positive value and goes towards zero (*down* sweep), capacitance increases in time: every new gate bias induces a slight recovery with respect to the previous one. The charge trapping due to positive gate bias (right drift, electron capture) and the partial recovery due to the decrease of gate bias (left drift, electron emission) are competing effects. Since the characteristic times for capture and emission processes are distributed in a similar way [8], at each bias step the two effects balance each other out. The aim of the C-OTF technique is to investigate the trapping behavior from the stress transient, by using a reference CV curve which represents the device status at the end of stress. We must therefore minimize trapping events during the sweep. For this reason, the negative sweep direction measurement provides a more accurate representation of the real CV curve of the device.

An additional argument in favor of this choice is shown in Fig. 14. Here the voltage drift is extracted using CV curves taken

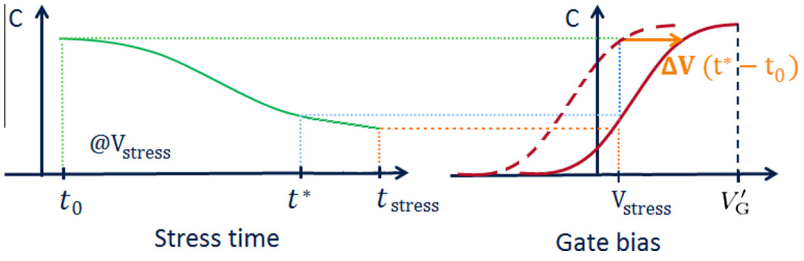

Fig. 12. Illustration of the C-OTF basic principle. After a stress transient (left) a CV curve is measured (right), which is used as a reference to extract the voltage drift ΔV for each point of the transient.

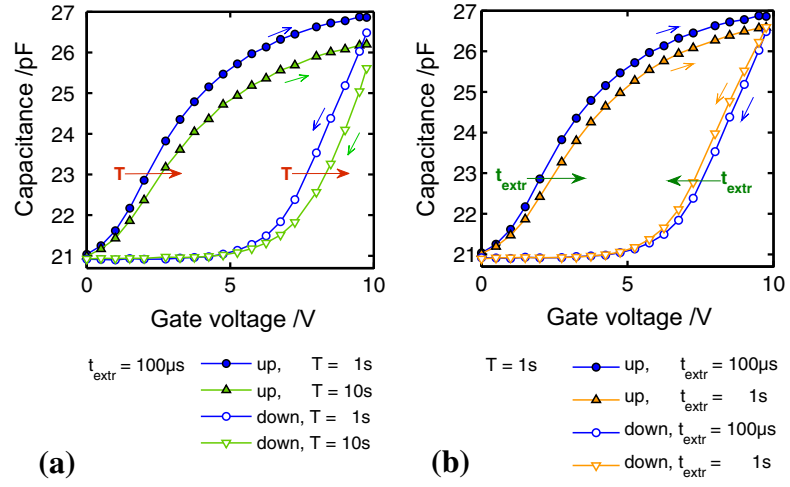

Fig. 13. CV curves taken with the lock-in amplifier with a gate voltage staircase. (a) Each bias step is held for a period T of 1 s or 10 s and the capacitance value is extracted at t_{extr} = 100 µs. (b) Each step duration is 1 s and the extraction time t_{extr} is 100 µs or 1 s.

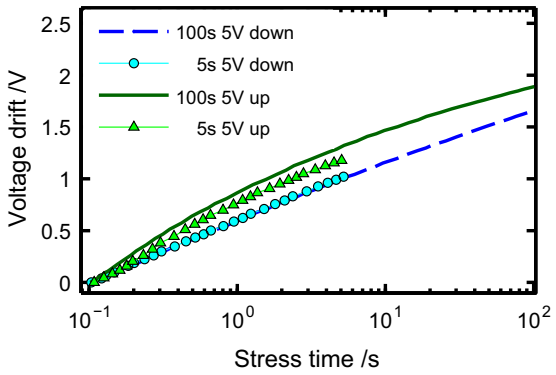

Fig. 14. Voltage drift time evolution extracted for different stress duration with CV references taken with positive and negative sweep directions.

in opposite directions. Two measurements with different stress duration are carried out. We expect to find the same result from the long and short measurement in the portion of stress time they have in common. This is true if the sweep direction is negative. If a positive direction is chosen, the time evolution of ΔV up to 100 ms is significantly different. This means that the distortion caused by sweeping cannot be neglected in this case.

As a conclusion from these tests we can summarize the requirements for the reference curve measurement. The sweep must have a negative direction; the bias extrema V'_G must be chosen such that the effect of sweeping does not exceed the drift due to stress; finally, a rather high sweep rate must be used to minimize charging or discharging of traps during the measurement.

5.4. Approximations and inaccuracies of the C-OTF technique

The first approximation of the C-OTF method is to neglect the unavoidable stress added by the reference curve: since the sweep must be taken with a decreasing voltage staircase, the application of a positive bias larger than the stress level will induce a certain amount of additional stress. Fig. 15a shows the CV curves measured after 100 s of stress at 5 V with a different choice of V'_G. It is clear that if the starting voltage V'_G is much larger than $V_{stress} + \Delta V$ the effect of sweeping can dominate over the drift due to stress. This leads to an overestimation of the voltage drift, as shown in Fig. 15b. The most accurate result would be the one obtained with the least additional forward stress, *i.e.* when using the reference curve with V'_G closest to the sum of stress level and stress induced drift. In this case, the choice of a V'_G more than twice the stress level leads to an error of 20%. Obviously, this means that a trade-off between the least additional stress and the possibility to measure capacitance values corresponding to the initial part of the stress transient needs to be found. As shown in Fig. 15b, a too small V'_G value (in this example, 5 V after a stress level of 5 V) does not allow to extract the ΔV on the whole stress time range, but only from approximately 10 s. This problem is more severe in the case of lock-in amplifier measurements: the transients here start from very large capacitance values, reachable after stress only with a very large V'_G. This is the reason why, even if the measured transients have a time resolution of 50 μs, the shortest time at which a ΔV extraction is possible can be as large as 10 ms, depending on the stress level and duration.

Another limitation of the C-OTF technique is the impossibility to determine the voltage drift value at the first measurement point. If an instantaneous measurement after the application of stress were possible, the first point would have zero ΔV. In fact, capacitance transients decrease starting from the first measurement points; we never observed the onset of such behavior. This means that the time constants associated with such decrease are smaller than our measurement capability, *i.e.* the phenomena responsible for the transient behavior starts before our shortest time resolution of 50 μs. In all calculations shown in this work, the initial value ΔV_0 is arbitrarily set to zero.

Finally, a third approximation made by the C-OTF technique is to assume a parallel shift of the CV curve. While this is true for small stress level and short duration, the impedance characteristic in the region C_2 can be subjected to distortion if the interface charge state changes severely, as we have shown in Fig. 8d. This is also visible in Fig. 15a: the shape of the curves taken with very different V'_G changes slightly. In Fig. 15b we calculate the voltage drift with the lock-in amplifier after a stress of 5 V for 100 s with different starting voltages between 5 V and 10 V. For the smallest V'_G the ΔV can be extracted only after about ten seconds. A V'_G of 8 V allows ΔV calculation starting from 100 ms. We note that the time dependence is the same as in the former case. Larger V'_G induce distortion in the CV characteristics, which leads to a slight overestimation of the extracted ΔV value. The error in the slope of the voltage drift transient resulting from the choice of V'_G is however less than 10%. This example shows that the optimization of the CV curve is of fundamental importance for the C-OTF technique as well. Preliminary tests about how to characterize at best the device are necessary to achieve acceptable accuracy in the final result.

6. Experimental results and discussion

The C-OTF technique is applied to GaN/AlGaN/SiN MIS structures, for a few values of forward bias stress. The results are shown in Fig. 16. The voltage drift increases with stress level and time: we observe a logarithmic behavior, consistent with other investigations such as stress-recovery experiments (based on the MSM tech-

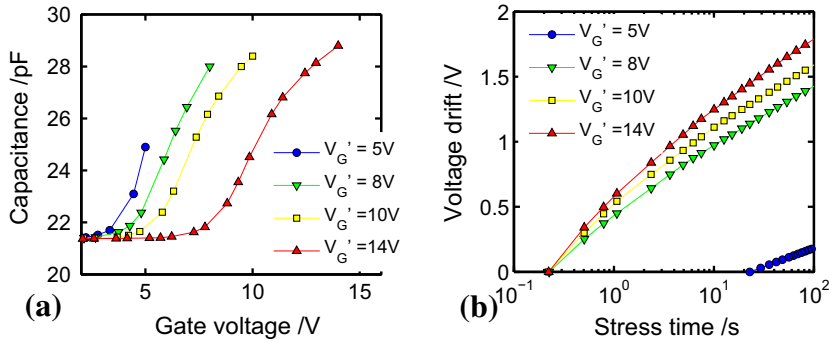

Fig. 15. (a) CV characteristics and (b) extracted voltage drift with the C-OTF technique for different values of V'_G.

nique) on MIS-HEMTs [13]. The number of electrically active interface states at the interface is in the order of 10^{12} cm^{-2}.

The logarithmic temporal evolution excludes the presence of a unique trap site with a specific time constant, similarly to what has been observed in silicon devices [27]. Such a behavior can be explained with a number of defects with associated time constant distributed from very short (less than 50 μs, according to the measured capacitance transients) to very large (100 s, the duration of stress) values.

The techniques presented have different principles and offer a different perspective on the results. The MSM is the basic concept behind the intuitive comparison of the device characteristic before and after stress. It is also the principle of repetitive stress-recovery experiments, which focus on both capture and emission processes and their interplay. Such an approach enables investigation of complex dynamic behavior including feedback effects. The C-OTF technique offers a deeper insight into the capture mechanism only. The main advantage is the direct access to the temporal evolution of degradation with a measurement on a single device. It requires a full understanding of the parameters affecting the reference curve measurement. For this reason, preliminary tests are needed to evaluate the best method to record the device characteristics.

Both methods rely on certain assumptions and have some inherent unavoidable, but minimizable drawbacks. A fundamental requirement for using the MSM technique is a suitable operating point for the device in recovery conditions. In order to be sensitive to device drift, specific bias ranges (or device operation points) can be used. In our case, gate voltages corresponding to the C_1 region are good choices, but a measurement where the capacitance shows its *plateau* would not allow ΔV extraction. In a similar way, a MOSFET must be measured with a gate bias close to the threshold voltage, where the transfer characteristic increases continuously. However, in the case of GaN-based devices this could be a regime suitable for buffer trap contributions: for a complete understanding it is essential to study and distinguish the role of each source of device degradation. Furthermore, it is necessary to ensure that the calculated ΔV value does not depend on the chosen operation point, or on other measurement parameters.

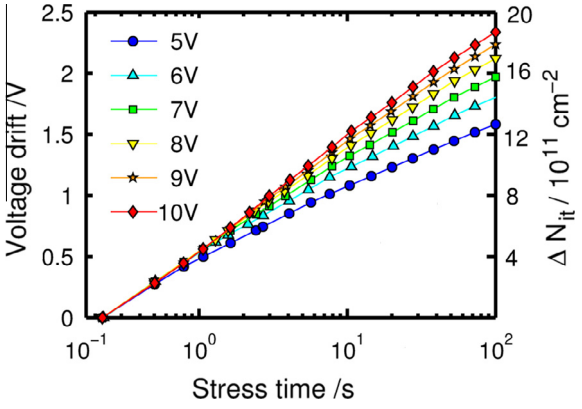

Fig. 16. Results on the Si-doped test structures with the C-OTF technique, for various values of forward gate bias $V_{stress} > V_{spill\text{-}over}$ for the Si-doped devices. The chosen V'_G is 3 V larger than the stress voltage.

For the C-OTF technique two approximations are necessary. Starting a sweep at larger gate bias than stress causes some unwanted additional stress whose influence on the shape of the characteristics, which is neglected in the analysis. However, it is possible to optimize V'_G in order to minimize such error. Furthermore, any difference in the curve shape before and after stress is also neglected. The impact of this last point might be very small in the case of a MOSFET if the mobility does not change together with the interface charge state during stress, but it might become important if the stretch-out of a MIS CV curve is very pronounced. In our case the capacitance characteristics do not stretch out consistently during stress, but a too high V'_G can indeed induce such a distortion. The optimization of the sweeping parameters is therefore of crucial importance also in this context.

A limitation of both techniques is the inevitable underestimation of device degradation due to the measurement delay. In the case of MSM, the time the instrument needs to record the first point after stress already implies some recovery, since V''_G brings the device in relaxation conditions. The larger the time delay, the larger the error in estimating ΔV. Regarding the C-OTF method, while the two aforementioned approximations result in an overestimation of the device drift, the measurement delay at the beginning of stress prevents an accurate calculation of the ΔV value at the first point. This results in an unknown offset, indicated as ΔV_0. This error is due to the impossibility to measure the device response fast enough during recovery for the MSM method, and during stress for the C-OTF technique. Given a certain measurement delay t_{delay}, the technique for which the underestimation is more severe depends on the relative speed of capture and emission processes. Since the stress and recovery curves for GaN/AlGaN/SiN MIS-HEMTs are found to have similar behavior for the wafer without Si-doping [8], the ΔV_0 is expected to be of the same order of magnitude. This can be seen in Fig. 17a, where good agreement is obtained with the two approaches for a stress duration of 100 s.

For structures with the additional Si-doped layer instead there is a difference of about 40% in the total amount of drift, as shown in Fig. 17b. This can be explained with a different rate for capture and emission processes. If the detrapping of electrons at interface states is faster than the trapping mechanism, then the error made with the MSM approach is larger than with the C-OTF method. In this case, the ΔV_0 missed during t_{delay} is more severe under

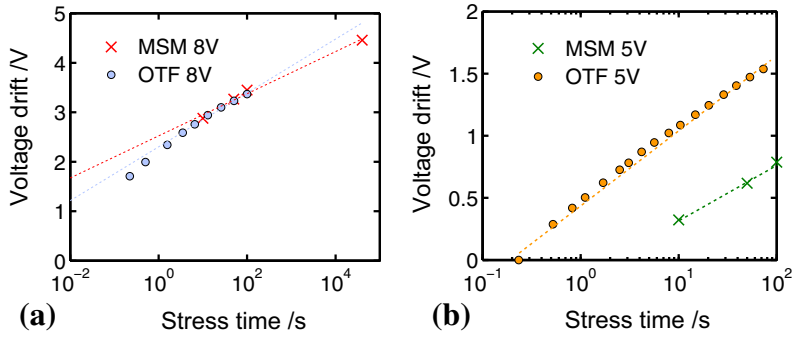

Fig. 17. Device degradation during stress, calculated with MSM and C-OTF methods (a) for devices without and (b) with Si-doping. The dashed lines show a logarithmic fit to the data.

recovery conditions than during stress. We can associate such behavior with the influence of the Si-doped GaN layer close to the interface with AlGaN. Defects located in this region have an effect on the device recovery at the read-out voltage V''_G, thus underestimating the total voltage drift. This example highlights the benefits of applying different techniques for the same investigations. In our case this has proven to be decisive for a comprehensive understanding of the physical trapping mechanism.

A final remark about the characterization techniques presented here regards temperature investigations. Since charge trapping and detrapping are considered to be temperature-activated processes, such experiments provide very important information. In fact, they are the next step towards the development of a comprehensive physical model, which can explain the device degradation dependence on temperature, stress bias and its temporal evolution. Heating up the device allows access to very long time constants, cooling it down to very short ones [28]. However, due to experimental restrictions both stress and recovery transients must be carried out at the same temperature. This brings further inaccuracies in the MSM technique. First, the read-out point might vary with temperature, causing an incorrect evaluation of ΔV. Secondly, at high temperature both degradation and recovery increase, partly balancing each other out. In this way it is impossible to determine the real dependence on the temperature. The C-OTF technique instead, focusing on the stress transient only, gives reliable results at each temperature allowing further insights into the charge trapping phenomena.

7. Conclusions

In this paper we have discussed in detail the properties of the impedance characteristics of GaN/AlGaN MIS structures, highlighting the challenging properties like frequency dispersion and hysteresis which hinder the evaluation of interface defect density at the interface with the dielectric. We have shown that the effect of having a barrier AlGaN layer introduces a dynamic response which is undistinguishable from the one of the trap ensemble, thus invalidating techniques based on the direct analysis of capacitance or conductance curves.

We propose and apply on our test structures methodologies previously suggested for investigations on silicon devices. Such methods constitute an alternative approach to characterize trapping phenomena at the dielectric interface. In particular, we do not need to assume the validity of the Shockley–Hall–Read model, which has been proven to be insufficient to explain bias temperature instability on silicon MOSFETs.

We have implemented a setup based on a lock-in amplifier for impedance measurements. The versatility of the instrument allows a deeper insight into CV characteristics, as well as a time resolution as low as 50 μs for sampling measurements. Experiments with these new capabilities provided the knowledge necessary to choose the most accurate way to evaluate the device impedance characteristic.

The main focus of this work is to emphasize the importance of using the appropriate measurement parameters in order to investigate device degradation. We show that a wrong choice in this sense can lead to severe errors in the calculated drift value. It is therefore crucial to be aware of the device behavior under different operation conditions, and to optimize the necessary parameters.

We present two different techniques to evaluate the voltage drift under forward gate bias. The MSM method is an intuitive approach based on the comparison of device characteristic before and after stress. In the C-OTF approach the voltage drift is extracted from a capacitance transient at constant gate bias, using the CV characteristic as reference.

Results on our test structures show a logarithmic temporal evolution of device degradation and recovery. The defects responsible for such a drift therefore exhibit a broad range of time responses. Furthermore, the time constants associated to these interface states are uniformly distributed. This would be compatible with a defect family whose activation energy for charge trapping is uniformly distributed over a certain range of energies. The development of a physical model which could shed light on the nature of these defects, however, requires further investigations. The first aspect to be studied is the influence of temperature on the distribution of interface states. Therefore, forward gate bias stress experiments on MIS-HEMTs using the MSM or the C-OTF techniques will contribute to fully understand interface state properties and, eventually, their identity.

Acknowledgments

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