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The Exploitation of the Spin-Transfer Torque Effect for CMOS Compatible Beyond Von Neumann Computing

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CONTENTS

The exponential growth in (affordable) computational power over the last decades was only sustainable due to continuous successful scaling of CMOS devices. The shrinking of the CMOS transistors allowed not only an increase in the speed and performance of circuits, but also ensured that the costs per transistor dropped for every technology generation. However, with each technology generation, new and ever harder to resolve obstacles appeared. Currently, out of the multitude of potential showstoppers in charge-based CMOS technology, the dissipated power and the energy associated with the transport of information are major concerns. The fast evolving field of spintronics offers a potential remedy for these problems by introducing "More than Moore" devices. The quest for the future universal memory candidate not only led to spin-based magnetoresistive random-access memory (MRAM), but also culminated in the first off-the-shelf MRAM products. Nevertheless, the core of the MRAM, the magnetic tunnel junction (MTJ), is not limited to memory applications. It can also be exploited for building logic-in-memory circuits with nonvolatile storage elements, as well as very compact on-chip oscillators with low power consumption. In general, the advent of nonvolatile elements, and especially spintronics in circuits, gives the unique opportunity to rethink how information is processed and moved. The concept of continuous information exchange between physically separated memory and processing units—also known as the Von Neumann architecture—has become a performance limiting bottleneck. The transition towards beyond Von Neumann architectures obviously also requires a redesign of all basic computational building blocks. In the this chapter, we will give an overview about the ideas and concepts for such beyond Von Neumann systems. First, we will present a short introduction into the physics necessary to understand the spintronic effects, like the magnetoresistance effect, spin-transfer torque (STT), spin Hall effect, and the magnetoelectric effect. Then we will move towards spintronic devices and circuits and their different concepts and architecture levels, where they introduce nonvolatility, such as thermally-assisted (TA)-MRAM, STT-MRAM, domain wall (DW)-MRAM, spin-orbit torque (SOT)-MRAM, spin-transfer torque and spin Hall oscillators, logic-in-memory, all-spin logic, buffered magnetic logic gate grid, ternary content

addressable memory (TCAM), and random number generators. From our point of view, there will be no disruptive transition from pure CMOS to pure spintronic circuits. Instead, there will be a gradual introduction and substitution of existing CMOS devices by spintronic devices, where they outperform CMOS devices in one or more aspects. Therefore, we will concentrate on and emphasize concepts and devices that are CMOS compatible and present possibilities for different levels of integration into CMOS technology.

Finally, we summarize the current state-of-the-art and extrapolate an outlook regarding future development of the field and prospective devices from our point of view.

4.1 Introduction

The persistence and ingenuity of scientists and engineers made it possible to maintain the miniaturization of electronic components and interconnects for many decades. This still ongoing strategy led to the current 14 nm node with multi-gate three-dimensional transistors [3] and culminated in the announcement of the mass production of 10 nm node products for 2017 [4–6]. In principle, devices with a few nanometers gate length are feasible [7], but their introduction into large scale manufacturing is rather challenging due to fabrication and control issues that translate into reliability problems. In conjunction with their broad variability, which manifests in high integration costs, it is clear that in the foreseeable future scaling will come to a halt.

However, looking at the very core of the MOSFET operation, the interaction between the electrons' charge and an electric field, reveals that there is another intrinsic electron property, which can be harnessed as an alternative degree of freedom—the electron spin. It not only holds the potential to complement, but to substitute the currently omnipresent charge degree of freedom for future electronic devices [8,9]. The electron spin is the angular momentum of the electron due to its intrinsic rotation and is commonly measured by its projection along a given axis. The introduction of the axis results in two possible projections (parallel and antiparallel to the axis), which can be facilitated for digital information processing. A further advantage of exploiting spin as a degree of freedom is the very small amount of energy, which is required to invert its orientation. All spin-based technologies share advantageous features like a low supply voltage, small device count, and zero static power [10]. An essential aspect for the realization of all-spin-based computing is the understanding and control of the injection, propagation, and detection of spin signals, which has been achieved only recently. The difficulties to demonstrate spin injection from a ferromagnetic layer into a semiconductor origin from the inherent spin impedance mismatch between these materials [11]. This problem can be solved by the introduction of a potential barrier between the metal and the semiconductor [12]. Another obstacle on the way towards all-spin computation is the growth of contacts with low resistivity per area for good spin injection. In [13], it has been shown that spin injection through single layer graphene contacts are a promising close to optimal solution [14].

One of the major differences between spin and charge injected into a semiconductor is that the spin signal is not conserved. During the diffusion of the spin information carrying electrons, their net spin relaxes through scattering events to the equilibrium value of nonmagnetic semiconductors—zero. Even though Huang et al. [15] successfully demonstrated spin injection and propagation over 350 μm through a silicon wafer at 77 K, the diffusion length is reduced to approximately 200 nm at room temperature [14].

Unfortunately, this length reduces even further in CMOS technology mainly due to the increased number of scattering events at the interfaces [16]. However, there is a trick to boost the spin lifetime in such systems. In (001) silicon films, the governing scattering mechanism that reduces the spin lifetime is the intervalley scattering between equivalent valleys. If one introduces uniaxial stress along the (110) direction, the degeneracy is lifted and the respective intervalley scattering is significantly reduced, which leads to a large increase in the spin lifetime [17,18]. Strain has been used for many years in the semiconductor industry to boost the electron mobility; thus, it is easy to exploit the same well established methods for enhancing the spin lifetime.

Furthermore, it has been shown that purely electrical spin manipulation in InGaAs heterostructures with point contacts is possible at low temperatures [19]. The down side of this is the very poor control of the spin signal by voltage-dependent spin-orbit interaction in silicon channels. Therefore, the only feasible way to introduce spin into nano-scale CMOS technology is to add ferromagnetic source and drain contacts [20]. Such structures exhibit different currents depending on the relative orientation of the magnetization orientation of source and drain, which can be exploited for the realization of reprogrammable nonvolatile logic. However, this is quite unsatisfying due to the rather low magnetoresistance ratios in comparison to MTJs. Therefore, the most promising way for the introduction of practical spin-driven applications within the next few years will likely be an MTJ-based solution.

An MTJ comprises two magnetic layers that sandwich a nonmagnetic thin insulating layer (cf. Figure 4.1). Depending on the relative orientation between the magnetizations of the two magnetic layers, MTJs either exhibit a low resistance state (LRS, parallel) or a high resistance state (HRS, antiparallel). The two resistance states LRS and HRS are assigned to logic "0" and "1," respectively [21,22].

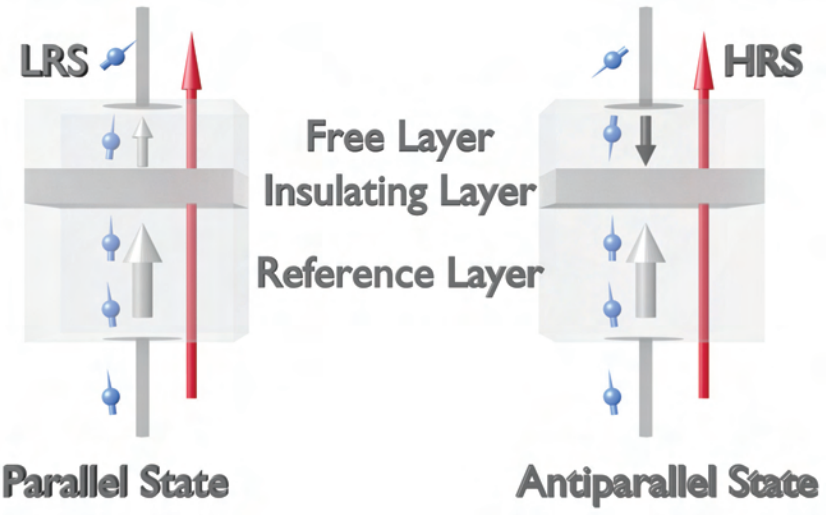

FIGURE 4.1
An MTJ consists of two magnetic layers separated by a nonmagnetic insulating layer. Depending on the magnetization orientation of the free and the reference magnetic layer with respect to each other, the electrons traversing through the layer stack experience more (antiparallel) or less (parallel) scattering, which is reflected in a high (HRS) and a low resistance state (LRS), respectively.

A universal memory that squares the circle of simultaneously being fast, nonvolatile, small in size, allows high integration density, and is CMOS compatible is spin-transfer-torque-based MRAM, one of the most promising candidates so far [22–25].

But the emerging spin-based technology has much more to offer. For instance, it can be used to build very compact versatile on-chip oscillators with low power consumption for consumer electronics and telecommunication applications. MRAM is also exploitable for logic-in-memory architectures, where the memory elements sit on top of the CMOS logic circuits. The combination of the nonvolatility of the memory elements and the considerably shorter interconnects guarantee low power losses and fast operation. There are already spin-based solutions able to compete with pure CMOS with respect to energy consumption and speed; however, one of the key aspects to be competitive in the market—the integration density—is still worse than in pure CMOS. Therefore, we will also look into ideas and technologies that have the potential for high integration density.

In the following section, we will first give an overview about the physical fundamentals of spintronics to allow the reader to concentrate on the devices and circuits in later sections. Since the peculiarities of the employed materials and their processing are essential to understand the current limitations for designing and manufacturing spintronic devices, the subsequent section is dedicated to these aspects. Then the different types of spintronic memory will be elucidated, followed by a spintronic logic section where different possibilities to implement logic will be explained. Afterwards the applications section will highlight some spintronic solutions to demonstrate the potential of spintronics in future applications. Finally, we will conclude the chapter and try to extrapolate how spintronics will develop in the future.

4.2 Fundamentals of Spintronics

In order to enable the reader to concentrate on the spintronic devices and circuits without the need to take breaks to look up physics details, a short section that will help to grasp the most relevant basic physical effects is provided here.

4.2.1 Magnetoresistance

The discovery of first the giant magnetoresistance (GMR) and later the tunneling magnetoresistance (TMR) were essential for the development of widely usable spintronic devices.

4.2.1.1 Giant Magnetoresistance

The GMR has been observed for the first time in Fe/Cr superlattices in the late 1980s by two independent researchers Baibich et al. [26] and Binasch et al. [27].

The GMR effect is observed when a current is passed through a stack of two or more magnetic layers that are separated by nonmagnetic conducting spacer layers. The measured resistance depends on the magnetization orientation of the magnetic layers with respect to each other. Commonly the strength of the GMR effect is expressed as the ratio between the high and low resistance states [28]:

$$GMR = \frac{R_{AP} - R_P}{R_P} = \frac{\rho_{AP} - \rho_P}{\rho_P} = \frac{\sigma_P}{\sigma_{AP}} - 1 \tag{4.1}$$

R_{AP} (high resistance) and R_P (low resistance) denote the resistances for antiparallel and parallel layer magnetization orientations, ρ_{AP} and ρ_P are the associated resistivities, and σ_{AP} and σ_P the corresponding conductivities, respectively.

According to the definition in Equation 4.1 the GMR can become larger than 1, if $\rho_{AP} > \rho_P$. To avoid confusion, there is also an alternative definition where the GMR is never larger than 1 ($\rho_{AP} > \rho_P$) [28]:

$$GMR' = \frac{\rho_{AP} - \rho_P}{\rho_{AP}} = 1 - \frac{\sigma_{AP}}{\sigma_P} \tag{4.2}$$

The simplest explanation for the GMR effect assumes that the electrons, which are traveling through the magnetic stack, can be described by two independent conduction channels. One channel describes electrons with a certain direction; for example, "Up," while the other channel describes electrons with opposite direction "Down" (see Figure 4.2) [29]. The sum of these two spin currents (I_{Up} and I_{Down}) forms the total charge current that passes through the stack. If these two spin currents flow through a ferromagnetic layer with a fixed magnetization direction, the electrons with "Up" and "Down" orientation experience different scattering rates depending on their orientation with respect to the orientation of the magnetic layer. This difference is reflected in different resistances for the two groups of electrons. For instance, if the magnetization orientations of the spin valve stack from Figure 4.2 are parallel, there is always one electron channel whose spin is antiparallel (electron spin and magnetic moment are antiparallel) and, thus, able to travel through the stack with only little scattering. On the contrary, if the magnetization orientation of the layers is antiparallel one of the channels always experiences enhanced scattering. As a result, the total resistance of the spin valve is lower for parallel magnetization ("Down"

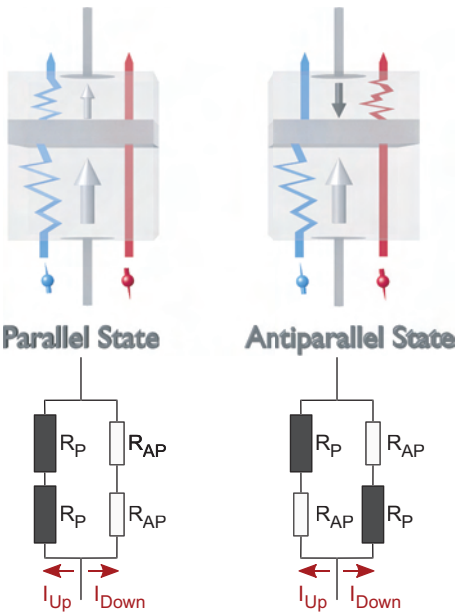

FIGURE 4.2
The GMR effect can be explained by assuming that the charge current can be split into two spin currents (I_{Up} and I_{Down}), which experience different scattering rates during their travel through the magnetic layers.

channel experiences only little scattering) than for antiparallel (both "Up" and "Down" channels exhibit a zone with increased scattering) [30].

This effect opened up the path for the development of today's hard disk drive read heads and encouraged research in GMR-based MRAM [31].

4.2.1.2 Tunnel Magnetoresistance

Another important effect that has great significance in current MRAM applications is the TMR. It was discovered by Julliere et al. [32] in a Fe/Ge/Co junction at temperatures below 4.2K in 1975. Similar to the GMR effect, TMR can be observed, where two magnetic layers sandwich a nonmagnetic insulating layer and the measured resistance depends on the magnetization orientation of the two magnetic layers with respect to each other. However, in this case the separating nonmagnetic layer is a thin metal-oxide (e.g., Al_2O_3 or MgO) and forms a MTJ in contrast to the GMR, where the nonmagnetic layer is composed of a metal (e.g., Cu) and forms a spin valve.

The TMR effect is quantified as the relative ratio between the parallel and antiparallel resistance states of the stack [33,34]:

$$TMR = \frac{R_{AP} - R_P}{R_P} \tag{4.3}$$

Analog to before, R_{AP} and R_P denote the high (antiparallel) and low (parallel) resistance states of the stack.

The source of this effect can be attributed to the difference in tunneling probabilities for the electrons with certain orientation (e.g., "Up" or "Down") from one ferromagnetic layer (reference layer) to the other ferromagnetic layer (free layer) through the oxide for a given magnetization state. Figure 4.3 depicts the energy bands and their respective occupation for the parallel (left) and the antiparallel (right) magnetization state. If the magnetizations of both layers are parallel (e.g., both point "Up"), the majority of the electrons occupies "Up" states and the minority "Down" states in the reference layer as well as in the free layer. Therefore, the bands and their occupation match, which makes it easier for the electrons to tunnel through the thin nonconducting layer. This state has a higher conductance (lower resistivity). In the case of antiparallel magnetization orientations (e.g., reference layer→"Up" and free layer→"Down"), the majority of the electrons in the free layer are in "Down" states and the minority of the electrons in "Up" states. Therefore, there are far more electrons in the reference layer with "Up" than matching states available in the free layer, which leads to a strongly reduced tunneling probability. Even though the spin "Down" electrons from the reference layer find plenty of available states in the reference layer, their total number is much smaller than the amount of "Up" electrons. Thus, they can only contribute little to the total conductance of the stack. In summary, the overall conductance is strongly decreased and an increase in the stack resistance is observed.

Although the TMR effect was found earlier than the GMR effect, its practical use was limited due to poor TMR values, until the advent of stacks with amorphous Al_2O_3 as tunnel barrier. Moodera et al. [35] and Miyazaki et al. [36] where the first who developed independently such structures. The largest TMR ratio for an MTJ with amorphous Al_2O_3 tunnel barrier at room temperature so far was demonstrated by Wang et al. [37] in 2004 and amounts to 70.4%.

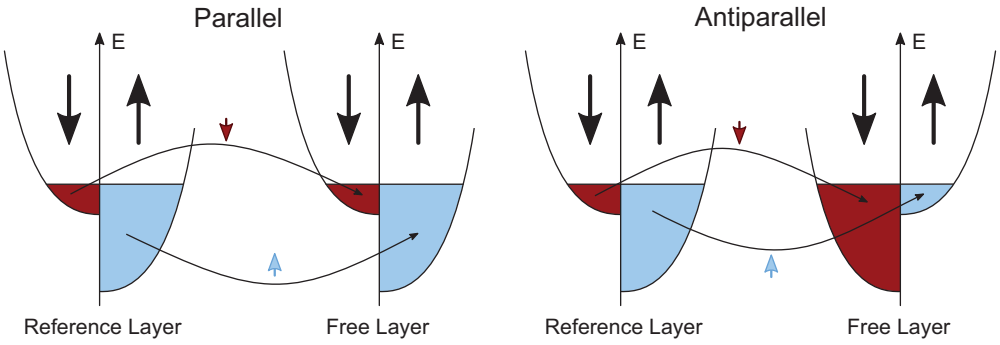

FIGURE 4.3
The energy bands and their respective occupation is different for parallel (left) and antiparallel (right) magnetization orientations. For parallel magnetization, the available states in the free layer match with the reference layer. Therefore, the electrons with "Up" and "Down" orientation are able to tunnel into matching states. For antiparallel orientation, there are far more electrons with spin "Up" than states available in the free layer. This reduces the tunneling probability considerably and causes an increase in resistance.

The next leap towards the realization of MRAM exploiting the TMR effect was the discovery of a giant TMR in an MTJ with an epitaxially grown MgO barrier. Again two scientists, Butler et al. [38] and Mathon et al. [39], predicted independently a giant TMR in MTJs with MgO tunnel barrier in 2001. Furthermore, Mathon predicted a TMR ratio >1000% for an MgO barrier [39].

This exceedingly large TMR ratio can be explained by a symmetry-based spin filtering that occurs in the MgO tunnel barrier [34]. Bowen et al. [40] were the first to measure TMR in Fe/MgO/FeCo (001) single-crystal epitaxial junctions. These measurements showed a much smaller TMR (27% at 300 K, 60% at 30 K) than predicted previously. In 2004, it was possible to increase the TMR ratio considerably in single-crystal Fe/MgO/Fe/MTJs, to a level of 220% [41] and 180% [42] at room temperature. Thanks to the rapid progress in the epitaxially growth techniques of MTJ stacks, the TMR increased swiftly [33]. By 2006, TMR values up to 410% could be demonstrated [43], followed by 604% at room temperature and 1144% at 4.2 K in Ta/$Co_{20}Fe_{60}B_{20}$/MgO $Co_{20}Fe_{60}B_{20}$/Ta junctions [44] in 2008.

4.2.2 Spin-Transfer Torque

Before the discovery of the spin-transfer torque (STT), the free layers of MRAMs were switched by the application of magnetic fields (cf. Figure 4.4). The magnetic fields were created by passing currents through adjacent wires. In order to protect the free layers from accidental switching, the memory cells must be designed in a way that two magnetic fields generated by two physically separated wires add up to switch the memory cells without unintentional switching events. The field-based switching method has the disadvantage of increasing current densities, when the structures are scaled down. This stems from the fact that the current must not change to ensure sufficient switching field strength, while at the same time the cross section of the wires decreases, when the structures are shrunk. This counteracting prerequisites made the shrinking of field-based MRAM below 90 nm unfeasible [45].

This field related limit was circumvented, when Slonczewski's [46] and Berger's [47] theoretical work predicted the existence of the STT effect in 1996. The exploitation of the STT effect represents a technological breakthrough, which allows the direct manipulation

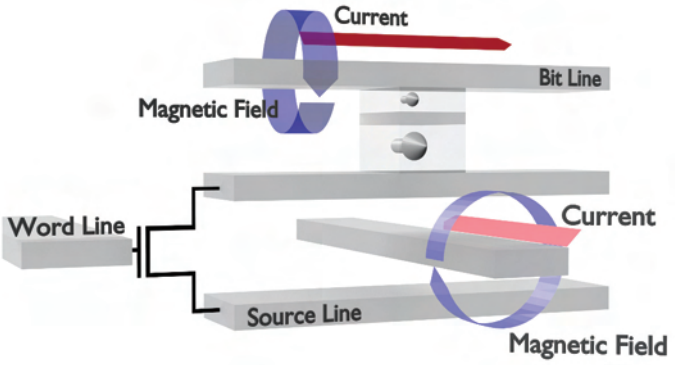

FIGURE 4.4
Field-based MRAM requires two wires for the generation of the writing field. Only when the magnetic fields created by both wires add up, the free layer will switch its magnetization. This design is deliberate to protect neighboring memory cells from accidental switching.

of the magnetization of a layer through a spin polarized current and renders the previously employed indirect switching via Ørsted fields superfluous.

When electrons move through a (thick) fixed reference layer, their magnetic moment aligns with the local magnetization (see Figure 4.5). If these spin-polarized electrons subsequently enter the free layer, they align again to the local magnetization orientation within a few Ångström. During the relaxation of the electrons to the local magnetization, not only the electrons experience a torque, but also the local magnetic moments (total sum of torques must be zero). This STT is able to excite precessions in the free layer and, if strong enough to overcome the damping, eventually switches the whole free layer. The precessions are carried out around the effective field H_{eff}. Changing the polarity of the

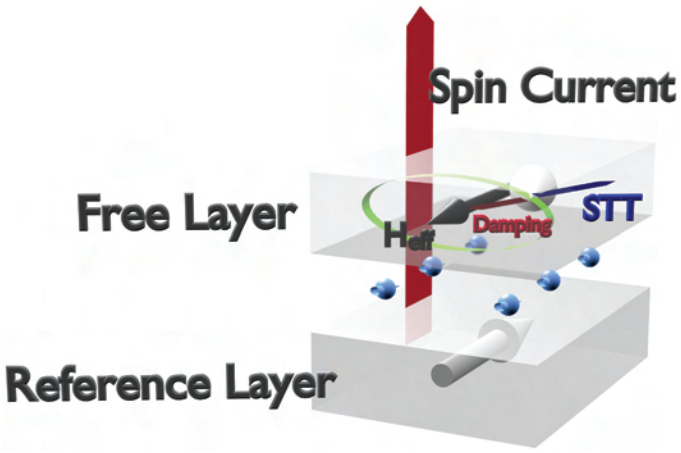

FIGURE 4.5
The electrons traversing through the stack, first pass the reference layer, where they align parallel to the reference layers' magnetization orientation (bottom). Then they pass the nonmagnetic layer (transparent gap) and finally enter the free layer, where they relax to the free layers magnetization orientation. This relaxation creates a spin-transfer torque that drives magnetization precessions. If the torque is strong enough to overcome the damping, the free layer is switched.

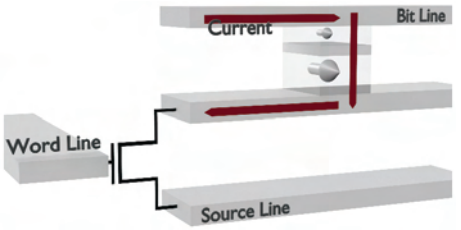

FIGURE 4.6
In contrast to the field-based MRAM (cf. Figure 4.4) STT-MRAM does not require an extra wire to prevent switching failures. Instead the magnetization is manipulated by a spin polarized current, which allows a considerably simplified memory cell design.

applied current flips the orientation of the exerted STT and, thus, allows to repeatably switch the free layer between antiparallel and parallel orientation with respect to the reference layer (see Figure 4.6).

Nevertheless, it took years until STT-induced switching could be demonstrated experimentally on all-metallic stacks [45]. Co/Cu/Co was the first GMR-based stack to proof the concept of STT-induced switching [48–52]. The first working STT-switched MTJ memory cells based on AlO_x were shown in 2004 [53] and based on MgO in 2005 [54].

4.2.3 Spin Hall/Spin-Orbit Effect

Another effect that has attracted a lot of attention, is the Spin Hall effect (SHE). It also generates a spin current capable of switching the magnetization of a layer and was predictedby D'yakonov and Perel in 1971 [55]. Driving a charge current through a metal line with strong spin orbit interaction generates a spin current perpendicular to the current's flow direction (see Figure 4.7). Vorob'ev et al. were the first to confirm the spin Hall effect experimentally in 1979 by observing a change in the rotation rate of the polarization plane for light propagating through a Te crystal [56]. Kato et al. [57] were able to demonstrate and confirm the same effect in 2004. The first direct electronic measurements were carried out

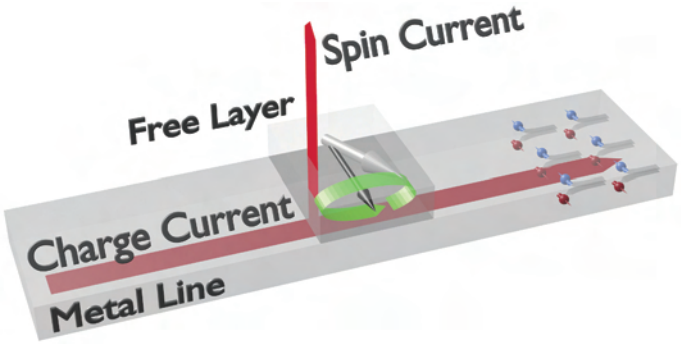

FIGURE 4.7
When a charge current flows through a metal line with strong spin-orbit interaction, a spin current perpendicular to the current flow is generated. The spin polarized electrons accumulate at the wire's surface and diffuse into the neighboring free layer, where they relax to the local magnetization and exert a spin torque on the free layer's magnetic moments.

by Valenzuela and Tinkham [58]. As it turned out later, they actually observed the inverse spin Hall effect (ISHE), since in their case they created a spin current, which generated a perpendicular charge current that accumulated at the edges of the sample exploited for electrical measurement [59]. For their work, they used a ferromagnetic electrode to generate a spin current and subsequently injected it into a nonmagnetic metal strip, where they took advantage of the ISHE as well as the nonlocal spin valve effect with the aid of a ferromagnetic probe electrode for the spin signal detection.

Further work regarding the SHE and the ISHE effect was carried out by Kimura et al. [60,61] and is based on NiFe/Cu/Pt structures. The spin current was measured by exploiting a nonlocal spin signal and the ISHE. Their work paved the way for the exploitation of the SHE and the ISHE as spin injection and detection tools.

4.2.4 Magnetoelectric Effect

Analog to the initially employed current controlled bipolar junction transistors, also the STT-based spintronic devices always require some kind of charge flow and thus also exhibit Joule heating as an energy dissipation mechanism during switching. This problem drove the transition from bipolar junction transistors to first N/P-MOS devices and eventually to the state-of-the-art CMOS technology. Therefore, ideally one could switch in spintronics from current-based to voltage-based magnetization dynamics manipulation in order to benefit the same way from the significant reduction in power dissipation [62].

Weisheit et al. [63] showed that the magnetocrystalline anisotropies of FePt and FePd compounds can be reversibly switched by an externally applied electric field. It was also demonstrated that a relatively small electric field can induce a large ∼40% change in the magnetic anisotropy of a bcc Fe(001)/MgO(001) junction [64]. Furthermore, it was demonstrated that the magnetocrystalline anisotropy of $Fe_{80}Co_{20}$(001)/MgO(001) cannot only be changed by an electric field, but actually voltage-assisted switched [65]. Nozaki et al. [66] showed high-frequency voltage-assisted magnetization reversal in MgO-MTJs in 2014. They could demonstrate a switching field reduction of >80% at a radio frequency of 3 dBm. Recently, Li et al. [67] could show that the introduction of a thin Mg layer at the CoFeB/MgO interface causes a 3× increase in the voltage controlled anisotropy coefficient (from commonly ∼30 fJ/Vm to ∼100 fJ/Vm). This is very encouraging, because it allows to reduce the write voltage below 0.6 V, which allows to employ advanced CMOS transistors.

The drastic change in the magnetocrystalline anisotropy strength of ultra-thin layers under the application of an electric field can be attributed to a change in the occupation of the atomic orbitals at the CoFeB/MgO interface, which together with the spin-orbit interaction, alters the anisotropy [62,67,68]. However, it can be also explained by the interfacial Rashba effect [62,69].

4.3 Materials and Their Processing

Since the peculiarities of the employed materials and their processing are essential to understand the current limits for designing and manufacturing spintronic devices, this section is dedicated to these aspects. A recurring theme of discussion is the integration with advanced CMOS process nodes, since a complete MRAM cell features a controlling transistor in combination with the MTJ element. MRAM technology has a few distinct

reliability issues and the large interest for MRAM technology has prompted tool vendors to develop dedicated tools. Acceptance of MRAM technology is manifested by its adoption into foundry process lines.

4.3.1 Back End of Line Integration

In integrated circuits the back end of line (BEOL) process refers to the fabrication of metal interconnects and the intermetal dielectrics (IMD) layers. Using successive deposition of metal (Cu), patterning of metal lines, IMD deposition, and planarization of the IMD layers, more than 10 layers of interconnecting Cu-lines can be realized. This is sufficient for the routing of signal and power supply lines in very complex circuits, with 100 millions of integrated transistors. All BEOL process steps are performed at low temperature, typically in the range 350°C–400°C. Therefore, the integration of spintronic memory and logic based on multilayer ferromagnetic metallic stacks with thin metal-oxide tunneling barriers is feasible. The MTJ stacks will not suffer from interdiffusion and the integrity of the tunneling barrier can be maintained [2,44]. Specifically the MgO barrier must be annealed under controlled conditions to obtain a proper crystallographic reorientation epitaxially along the (001) direction. More importantly, annealing is also necessary to induce the interfacial perpendicular magnetic anisotropy (PMA) effect for stacks based on CoFeB, which is intrinsically an in-plane material [70]. A comprehensive review of the PMA and its applications in [71]. The PMA can also be strengthened by using, for example, multilayer Co/Pt with inherent PMA or synthetic antiferromagnetic (SAF) layers in the MTJ stack [72]. Capping layers (e.g., silicon nitride) are used to protect the MTJ from unintentional reoxidation during later stages of processing. The MTJs are typically inserted close to the top metal layers. The MTJ bottom electrode is connected to an already available Cu-line in, for example, metal level 5 (M5), [1]. Subsequent MTJ layers are deposited without breaking the vacuum, patterned by lithography and etching and then embedded in the subsequent IMD layer. The IMD thickness depends on the layer and is chosen to minimize the interconnect capacitances. The MTJ stack total thickness is less than the IMD thickness so that the MTJ becomes fully embedded. For an illustration of production near embedded MRAM, see Figure 4.8.

To implement MTJs in the BEOL process flow the minimum additional lithographic mask count is three or four. To put this into perspective, a 14 nm advanced CMOS process node uses close to 70 mask steps. Also for comparison it is interesting to note that embedded flash nonvolatile memory has an added mask count as high as a dozen. Embedded static random-access memory (SRAM) has a significantly larger footprint or cell area, while embedded dynamic random-access memory (DRAM) is a quite complex process module, including high aspect ratio etching and filling steps for the storage capacitors.

4.3.1.1 MRAM Cell Density

The metal pitch in advanced technology nodes is compatible with the size of an MTJ element and the area of the complete MRAM cell, including one controlling CMOS transistor, follows the standard CMOS design rules. The width of the CMOS transistor must be chosen so that enough drive current can be supplied in order to reach the critical current density for STT switching. This has led some researchers to pursue devices that are voltage controlled (VC) MRAM and consume less current, allowing smaller transistors to be used [73]. A 4Gbit MRAM density has been demonstrated with 90 nm pitch [74]. The minimum pitch is used in the lower metal layer while the metal pitch increases for higher layers [75].

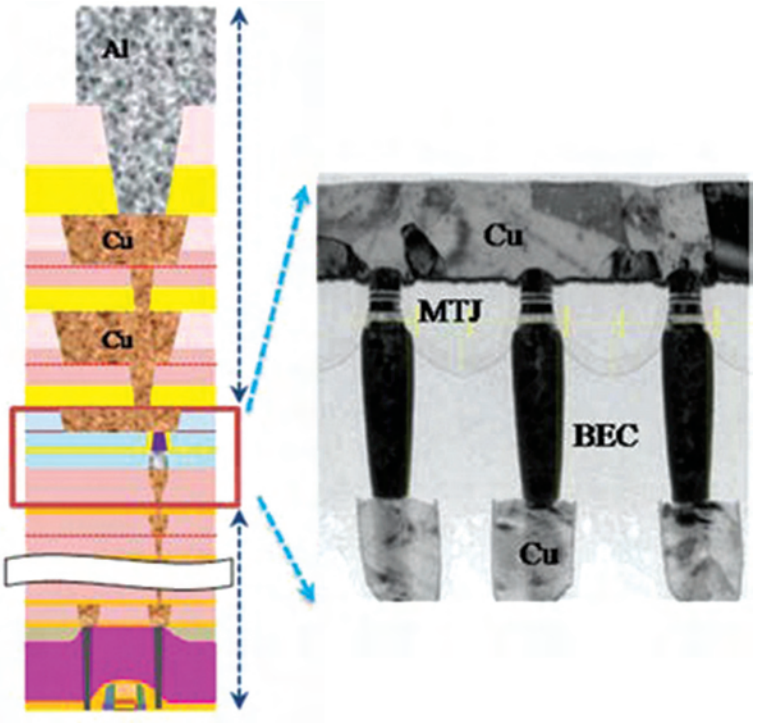

FIGURE 4.8
Example of production-near embedded MRAM [1]. Left panel showing schematic vertical structure of 8 Mb STT-MRAM cell array embedded in 28 nm logic process. Right panel showing transmission electron microscopy (TEM) picture of MTJ module inserted between Cu BEOL lines.

A via needs to be opened in the IMD and aligned to the MTJ top contact area. There are several methods to achieve this, including self-aligned process schemes [76]. A combination of chemical mechanical polishing (CMP) and deposition of sacrificial or etch stop layer on top of the actual MTJ are examples for such self-alignment solutions.

4.3.1.2 MTJ Multilayer Stack Deposition

Metal layers in the BEOL flow are deposited by sputtering tools, also known as physical vapor deposition (PVD) tools. The particular requirements for MTJ stacks include the possibility to deposit a large number of elements, for example, Ta, Ru, Co, Ni, Fe, Cu, Pt, B, Mg, and Al to name the most common. The tools operate under ultra-high-vacuum conditions (UHV) corresponding to 10^{-8} Torr or better and feature in-situ annealing capability. The UHV condition is a key requirement, for growing sub-nm atomically abrupt layers. In research, molecular beam epitaxy is sometimes used for abrupt layers, but for production purposes PVD tools are the only choice in terms of throughput, wafer scale uniformity and metal targets available. Dedicated PVD tools for MRAM fabrication are offered in multi-cathode configuration, able to handle the large number of elements. Examples of deposition and etching tool vendors include Applied Materials, Singulus, Canon Anelva, Oxford Instruments, and LAM. It should be noted that several of these companies already have a strong presence in microelectronics fabrication.

4.3.1.3 Two-Dimensional Materials in the MTJ Stack

Using emerging two-dimensional (2D) materials either graphene, boron-nitride (BN), MoS_2, or WS_2 offers an interesting path to improve the MTJ stack [77]. There have been successful demonstrations of using graphene as a tunneling barrier [78]. However, in this case the TMR is too low to consider applications. On the other hand, graphene and other monolayer materials are excellent diffusion barriers and can be used in combination with oxide tunneling barriers, since they alleviate interdiffusion issues during high temperature process steps [79].

4.3.1.4 MTJ Shape, Patterning, and Etching

MTJs are patterned and etched into pillars with their material stack sandwiched in between nonmagnetic top and bottom metal contacts. First and second generation MRAM cells relied on in-plane magnetization and shape anisotropy to stabilize the magnetization of the fixed or reference layer. Therefore, elliptic shapes were mandatory. This requirement put very stringent boundaries on the pattering process since variability in shape could be detrimental to the switching energy barrier. Basically, elliptic shapes are not optimal from a patterning perspective. In standard CMOS foundry design rules, circular contacts are patterned at minimum lithographic dimensions. In current generation MRAM, the use of materials with perpendicular anisotropy removed this constraint of having elliptically shaped MTJ elements and hence significantly eased the process integration. As discussed above, the MTJs are comparable to the pitches used in the BEOL and deep-UV optical lithography provides the necessary resolution and alignment. It should be mentioned that the scientific community relies almost exclusively on electron beam lithography, which has nanometer resolution but suffers from long writing times, and is impractical to use for alignment of multiple layers with critical dimensions.

Regardless of the patterning technique, the etching of MTJ stacks is known to be challenging, because the etching residues are not very volatile. This becomes an issue in reactive ion etching (RIE), where the substrate temperature must be raised to achieve enough etching rate for the removal of residues and to avoid redeposition. The temperature the metal stack can tolerate is limited, so other solutions must be considered. The main technique is physical etching by sputtering with low energy Ar ion beams. For this technique, there are also redeposition issues. Furthermore, since the etch is typically performed at glancing angles, the area of the patterned element will be reduced by lateral etching of the pillar sidewalls [80]. It could be advantageous to shrink the lithographic pattern size [81], but it is generally considered as a drawback of these etching tools. Many ion beam tools are equipped with in-situ analysis capabilities of the etching residues, which is highly useful for controlled etching of monolayers. Alternative methods include atomic layer deposition (ALD)/atomic layer etching (ALE), where the volatility of the etching residues is increased by controlled deposition of selected elements on the metallic surfaces [82]. For etching of multilayer stacks, the chemical reactions provide a degree of selectivity to the different materials being etched. In contrast, ion beam etching has virtually no selectivity due to its purely physical nature of material removal.

4.3.1.5 Nonvolatile Logic

Processing of nonvolatile logic based on MRAM cells is a straightforward adaption of the standard MRAM blocks (also known as macros). While these highly regular memory matrices are based on a 1T/1MTJ configuration, the relative number of transistors as

compared to MTJs increases in the hybrid realization of nonvolatile logic [83]. As an example, one would use at least six transistors and two MTJs in a flip-flop. To reduce this area and computational energy overhead, it would be preferable to move all computation to the spin domain and to use electronics only for interfacing purposes (see Section 4.5).

4.3.1.6 Access to Foundry Process Flow

All main foundry-based actors in the semiconductor business, such as TSMC, UMC, Global Foundries, and Samsung, have announced embedded MRAM (eMRAM) options by end of 2017 (see [84]). The intellectual property (IP) needed to get started in the MRAM field has been transferred to the foundry partners from start up companies, closely connected to academia. Some companies have entered manufacturing agreements and continue to develop their own IP. Finally, there are some companies with strong in-house activities, notably Toshiba.

4.3.2 Reliability and Yield Issues

During qualification, all memory devices are subjected to thorough cycling at various operating conditions, including elevated temperatures and increased humidity. Typical specifications require that a nonvolatile cell retains its state over a specified time (10 years) [84] and that a cell can be cycled (10^7 times) without any penalty in read or write voltage margin [85]. In fact, current MRAM offering surpass this significantly. In particular, the number of cycles is often given as close to unlimited [86].

4.3.2.1 Time Dependent Dielectric Breakdown

For MTJs one can identify several reliability issues. The main one is the relatively high current density passing through the MgO tunneling barrier during switching. This might lead to time dependent dielectric breakdown (TDDB), which is a well known issue in advanced CMOS with thin gate oxides. The TDDB is strongly affected by the temperature, as discussed further below.

4.3.2.2 Electromigration and Self-Heating

The relatively high critical current densities posed a serious threat due to possible electromigration in early generation spintronic devices [87]. For MTJ devices based on STT, the current densities are orders of magnitude lower. Since MTJs are embedded in isolating material with relatively low thermal conductance, there might be a significant temperature increase during switching. Increased temperature is known to accelerate electromigration by a power law [88].

4.3.2.3 Shorting of the Tunnel Junction and Etch Damage

During ion beam etching of the MTJ pillars, redeposition of metal can potentially cause an electrical short along the pillar sidewall and hence short the tunneling barrier [84]. This type of defect must be avoided since a parallel resistive path forms and effectively eliminates the difference between high and low resistance states of the MRAM cell. Careful tailoring of etch process, including good control of the sidewall slope is key to obtain high yield. In practice, the MTJs in production-near MRAM cells feature a small intentional sidewall slope (see Figure 4.9).

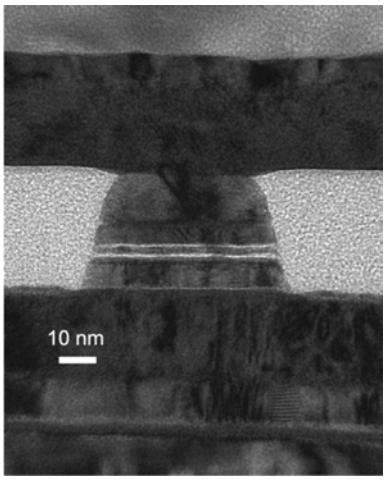

FIGURE 4.9
Cross-sectional transmission electron microscopy image of a fully functional device integrated on 90 nm CMOS [2]. The diameter of this device is about 50 nm.

Vertical sidewalls cannot be controlled with sufficient accuracy in wafer scale production. In case of RIE tools, redeposition on the MTJ sidewalls also occurs, but in this case of polymer residues. These can be removed by proper post-etch cleaning steps. The chemical species used in RIE tools are very corrosive and could damage the sensitive MgO tunneling barrier. Again, post process cleaning is essential to hinder any further corrosion due to remaining etchant species.

4.3.2.4 Voids/Open Failures

The MTJs are sputter deposited on bottom electrodes, which are part of the standard BEOL process flow. As in any contact opening the surface should be free of residues of such polymers, which remain from previous process steps [84]. Good via filling is essential particularly for the top contact, so that all of the MTJ area is contacted. Having a partial void at either the bottom or top contact will degrade the relative changes in resistance during switching and increase the absolute value of the MTJ resistance, so that the voltage drop becomes too high.

4.3.2.5 Disturbance by Internal and External Fields

Both read and write operations of MRAM can be disturbed by external fields. As the first generation MRAM cells were field-switched, current generations rely on spin transfer torque or voltage controlled anisotropy (cf. Sections 4.2.2 and 4.2.4). As an example of the field sensitivity, data sheets for commercial products give a limit of 8000 A/m. In addition, in a scenario where MRAM cells are placed at minimum design rules in advanced CMOS technology nodes, neighboring cells could affect each other due to their internal stray fields.

4.4 Spintronic Memory

Memory can be distinguished into two categories: volatile and nonvolatile. The volatile memories, such as SRAM and DRAM, retain their data as long as they are supplied with power. The nonvolatile memories, such as EEPROM and Flash, retain the data when powered off.

Conventional computers are organized in a memory hierarchy to improve their performance and optimize the cost [89]. The hierarchy is illustrated in Figure 4.10. The fastest, highest performance memory technology is placed at the top of the pyramid. The high performance memory is expensive so its size is kept small. At the top of the hierarchy is the so called Level 1 cache (L1), which is typically a small volume memory placed on the same chip as the microprocessor. L1 cache is realized through SRAM and fabricated with the same CMOS technology as the microprocessor. Further levels of cache (L2 and L3) are also SRAM, but typically on dedicated stand-alone chips. Below the cache is the main or primary memory, with considerably larger size than the cache. DRAM is employed for the main memory and its size is a tradeoff between cost and required performance. All data in the cache is also present in the main memory in order to avoid accessing the relatively slow main memory as much as possible. Below the main memory is the nonvolatile storage or secondary memory, where volume is more important than performance. The storage memory was for a long time occupied by HDDs, but now faces competition from the

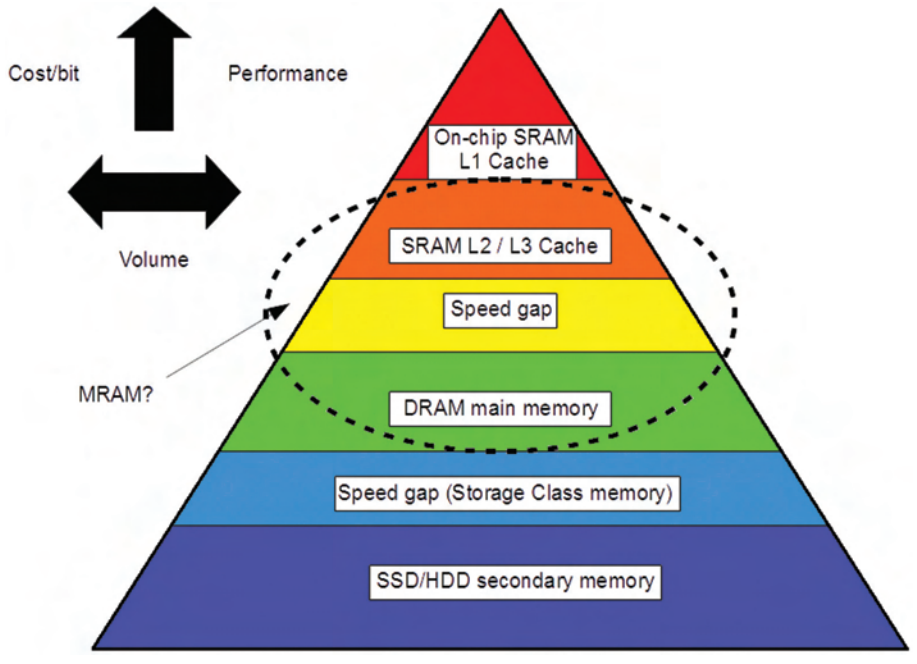

FIGURE 4.10
Pyramidal representation of the memory hierarchy. MRAM is a suitable candidate for L2/L3 cache and main memory.

NAND-flash-based solid state drives (SSD). The main memory mirrors the data from the comparatively very slow storage memory in order to speed up the access times.

Currently, there are two speed-gaps in the hierarchy: Between the cache and the primary memory and between the primary memory and the secondary memory [90,91]. For the gap between the primary memory and the high volume secondary memory, a new hierarchy level—the storage class memory (SCM)—has been proposed. To fill the gap the employed memory must exhibit, a density higher than DRAM, an access time shorter than NAND-Flash, and nonvolatility. Right now there is a competition between several nonvolatile random access memory (NVRAM) types that have potential for SCM applications, such as phase change memory, conductive bridge memory, resistive memory, and MRAM.

MRAM is a high performance NVRAM suitable for SCM applications, but currently not used in the SRAM, DRAM and HDD/SSD dominated memory hierarchy. MRAM has been proposed as a universal memory that can fill all levels of the memory hierarchy. However, the up to now rather low density prohibits any serious competition with the well established HDD/SSD technology. Due to the demand of a high density for an SCM, other NVRAMs are better suitable [90,91]. Especially, a three-dimensional monolithic integration of cross-bar memory arrays is more likely to succeed. These require memory cells that use a 1D-1R memory cell architecture (see Section 4.4.3). A more realistic application for MRAM is to replace SRAM and DRAM in L2/L3 cache and primary memory, respectively. It can bridge the speed gap between the cache and the primary memory. The required high endurance has been successfully demonstrated [92] and Kitagawa et al. [93] showed that a simulated mobile CPU would use less power, if it employs MRAM instead of SRAM as L2 cache. Other examples of MRAM for cache-applications can be found in [94]. MRAM is available on the market for main memory applications (DDR3 DRAM compatible) [95]. The major benefit of replacing DRAM with a NVRAM is the removal of the refresh action, the reduction of the overall power consumption and the simplification of the circuit design.

In this section, the MTJ, the core of the spintronic memory, will be discussed in depth. Its properties and trade-offs will be presented. The different varieties of spintronic memories and their peculiarities will be shown and the different memory cell architectures compared.

4.4.1 Magnetic Layer Design

4.4.1.1 Free and Reference Layer

A basic MTJ is composed of three elements: The reference layer, the tunneling barrier, and the storage layer. The tunneling barrier was covered in Section 4.2.1.2.

Storage layer: The storage layer, or free layer, is the layer that stores information as magnetization direction. A necessary requirement is that the free-layer material possess an energetically favorable nonzero magnetization in the absence of an external magnetic field or a remanent magnetization. There are elemental ferromagnetic materials (e.g., Fe, Co, Ni), ferrimagnetic half-metal oxides (Fe_3O_4, $La_{1-x}Sr_xMnO_3$), and various ferromagnetic alloys ($Ni_xFe_yCo_z$, Heusler alloys). Today, CoFeB ($Co_{0.20}Fe_{0.60}B_{0.20}$) is the material of choice as it has low damping [96] and provides high TMR in combination with MgO as tunneling barrier [44,97]. The free layer is a planar thin-film and can be further differentiated in films with in-plane and perpendicular magnetization direction. In order to achieve a free layer with in-plane direction, the free layer commonly exhibits an elongated shape (such as elliptic or rectangular). This form creates a shape

anisotropy with two well-defined stable magnetization states along the major axis. The effective anisotropy field H_k for in-plane design is given by [96,98]:

$$H_k = 2(M_s d_F) \times \left(\frac{l_F - w_F}{w_F \times l_F} \right) = 2(M_s d_F) \times \left(\frac{AR - 1}{w_F AR} \right) \tag{4.4}$$

l_F and w_F is the length and width of the free layer ($l_F > w_F$), respectively. AR denotes the aspect ratio ($= l_F / w_F > 1$), d_F the layer thickness, and M_s the magnetization saturation. The largest value the effective anisotropy field can reach is $2(M_s d_F)/w_F$. The magnetic moment $m = M_s A_F \times d_F$ is accessible through measurements with a vibrating sample magnetometer (VSM), and, if the area $A_F = l_F \times w_F$ is known, $M_s d_F$ can be determined ($= m/A_F = M_s d_F$). A typical ferromagnet (Co, Fe, Ni) exhibits an M_s of $\sim 10^6$ A/m. The two stable states of the magnetization are separated by an energy barrier that prevents the magnetization from freely switching the direction. The energy barrier determines the retention and switching properties, as will be discussed in Section 4.4.1.2. The general model for the energy barrier is found in [96,99]:

$$E_b = \mu_0 M_s H_k V_F / 2 = \mu_0 (M_s d_F) H_k A_F / 2 = K_u V_F \tag{4.5}$$

μ_0 describes the vacuum permeability, V_F the volume of the free layer ($= A_F \times d_F$), and K_u is the magnetic anisotropy energy density. The model for the energy barrier can with the aid of Equation 4.4 be further refined to analyze implications for in-plane designs:

$$E_b = \frac{\mu_0 (M_s d_F) H_k A_F}{2} \sim \mu_0 (M_s d_F)^2 w_F \times (AR - 1) \tag{4.6}$$

Assuming a constant aspect ratio, one can see from Equation 4.6 that the barrier depends quadratically on the layer thickness and linearly on the layer width.

In contrast, for the perpendicular design, the effective anisotropy field H_k is governed by three terms [96]:

$$H_k = \frac{2M_s}{\mu_0} K_b + \frac{2}{\mu_0 d_F} \sigma - \frac{1}{2} M_s \tag{4.7}$$

The first term corresponds to the perpendicular bulk anisotropy (given by K_b, J/m^3), the second term to the perpendicular surface anisotropy (given by σ_i, J/m^2), and the third term to the demagnetization energy. The perpendicular design becomes unstable, if the demagnetization energy dominates. Ferromagnetic materials behave differently in different nonequivalent crystal directions, which manifests in the magnetocrystalline anisotropy. As an example, Co, which has hexagonal symmetry, prefers a magnetization along *c*-axis instead of lying in the *a*-plane, and has an anisotropy energy of 4.5×10^5 J/m^3, or 2.8×10^{-3} eV/nm^3 [100]. The magnetocrystalline anisotropy can be used as source for bulk anisotropy. If this bulk term dominates, the anisotropy field is independent of the film thickness and the energy barrier is given as

$$E_b = \frac{\mu_0 (M_s d_F) H_k A_F}{2} \sim \left(K_b - \frac{1}{2} \mu_0 M_s^2 \right) d_F \times A_F \tag{4.8}$$

In this case, the energy barrier increases with increasing volume. Both magnetocrystalline anisotropy and damping are correlated functions of spin-orbit coupling [100,101]; thus, systems using intentionally high magnetocrystalline anisotropy (Pt/Pd systems, FePt [102], or Co/Pt-multilayers [101]) exhibit large damping, which will be discussed in relation with switching current in Section 4.4.1.2.

If the interface term dominates, the barrier is given as

$$E_b = \frac{\mu_0 (M_s d_F) H_k A_F}{2} \sim \left(\sigma_i - \frac{1}{2} \mu_0 \frac{(M_s d_F)^2}{d_F} \right) \times A_F. \tag{4.9}$$

The barrier increases with increasing area, but decreases with increasing thickness. The demagnetization term dominates, if the thickness is larger than a critical value, $d_C = 2\sigma_i / \mu_0 M_s^2$. The interface anisotropy for a CoFeB film sandwiched between Ta (bottom layer) and MgO (top layer) is $\sim 1.8 \times 10^{-3}\,\mathrm{J/m^2}$ and has a critical thickness of 1.1 nm [103].

Reference layer: Unlike the storage layer, the magnetization of the reference layer is not supposed to switch. For in-plane and bulk anisotropy designs, a simple solution is to have a relatively thick film in comparison to the storage layer. For interface anisotropy designs, it is the opposite. High anisotropy is achieved by having a relatively thin film [104]. A more sophisticated solution is to couple the ferromagnet to an antiferromagnetic material (AFM). For an AFM, it is energetically more favorable to be in a state with net-zero magnetization. This is achieved by arranging the magnetic moments in a regular pattern with neighboring moments (on different sublattices) pointing in opposite directions. At the interface between a ferromagnet and an AFM, the moments can align across the interface and couple the two layers. Reversing the magnetization of the coupled ferromagnet requires that the coupling energy is overcome, as the AFM will resist reversal. Thus, the ferromagnetic layer is pinned into a magnetic state. This exchange bias acts like an additional anisotropy field that forces the magnetization of the ferromagnetic layer into a specific state [105]. PtMn is an example for an antiferromagnetic material used in devices, with an interface anisotropy energy of $3.2 \times 10^{-4}\,\mathrm{J/m^2}$ [105].

If the reference layer comprises only one ferromagnetic layer, the reference layer exerts a fringe field on the free layer. This fringe field biases the free layer towards the antiparallel state. A remedy is to use a synthetic antiferromagnet (SAF). The SAF has two ferromagnetic layers forced into antiparallel state with net-zero magnetization. The two ferromagnetic layers are coupled through a very thin (typically less than 1 nm) nonmagnetic metal (like Ru or Cu). Depending on the thickness of the spacer, it may be favorable to have ferromagnetic coupling (both align) or antiferromagnetic coupling (anti-parallel). The interlayer exchange coupling can be described by the Ruderman-Kittel-Kasuya-Yosida (RKKY) model [106–108].

State-of-the-art MTJs are complex multilayer devices. Examples of MTJs include (from bottom to top): seed layer/PtMn/CoFeB/Ru/CoFeB/MgO/CoFeB/capping layer (an in-plane design with AFM and SAF) [109], Si wafer /Ta/Ru/Ta/CoFeB/MgO/CoFeB/ Ta/Ru (an in-plane design without AFM or SAF) [44] and Ta/Ru/Ta/CoFeB/MgO/CoFeB/ Ta/CoFeB/Ta/CoFeB/ MgO/Ta/Ru (interface perpendicular design, the MgO/CoFeB/Ta/ CoFeB/ MgO cleverly doubles the energy barrier by doubling the interface anisotropy without increasing the switching current) [110]. The various designs are illustrated in Figure 4.11.

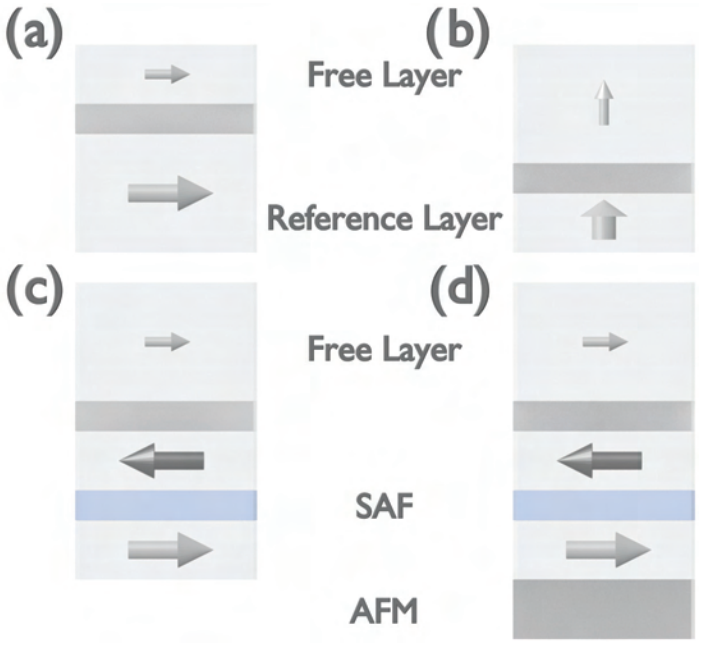

FIGURE 4.11
MTJ designs, where the reference layers are represented by big arrows and the free layers by small arrows. (a) An in-plane design, with the reference layer thicker than the free layer. (b) An interface perpendicular design, with the reference layer thinner than the free layer. (c) An in-plane design with a SAF. (d) An in-plane design with both a SAF and an AFM.

4.4.1.2 MTJ Properties

Memory devices are characterized by several key characteristics, such as endurance, retention, power consumption, read/write time, and density.

4.4.1.2.1 Endurance

Assuming an access interval of 1 ns to 10 ns for a high performance memory, the memory will experience about 3×10^{16} operations for an expected operational lifetime of 10 years. Assuming further a 256 kiB memory density/64 B cache line (L2 cache [92]), an individual memory cell is accessed about 10^{13} times. The number of times the memory is read is usually not a problem, but changing the state of a memory device can degrade the storage mechanism. As such, memories can wear out by repeated writing, and a cache memory should, therefore, withstand 10^{13} write operations. The endurance describes how many times a memory can be rewritten before the memory states become indistinguishable, which is a special reliability concern of memory devices. In a magnetic memory, the storage mechanism is the direction of magnetization in a ferromagnetic metal. There is no known degradation mechanism for the magnetization—the direction can be switched an infinite number of times. Of more concern is the degradation of the tunneling barrier in MTJs, which can be degraded by current injection during writing. However, for MRAM it has been demonstrated that it has "practically" unlimited endurance ($>10^{12}$) [86,92,111].

4.4.1.2.2 Retention, Volatility, and Thermal Stability

The distinction between a volatile and a nonvolatile memory is that the retention time, the time which the data is retained after power off, for nonvolatile memories is more than 10 years. MRAM belongs to the thermodynamically stable nonvolatile memory category, which means that the two possible states are approximately equally stable. Nevertheless, the memory is still susceptible to thermal fluctuations. The failure mechanism is modeled as [99]

$$\frac{1}{\tau} = \frac{1}{\tau_0} \exp(-E_b / k_B T). \tag{4.10}$$

τ is the mean time, τ_0 the attempt period (approximately equal to the gyromagnetic resonance period [112], 10^{-10}–10^{-9} s), E_b the energy barrier (cf. Section 4.4.1.1), k_B the Boltzmann constant, and T the absolute temperature. The ratio $\Delta_H = E_b / k_B T$ is called the thermal stability factor and dimensionless. The thermally activated process is stochastic and the probability is modeled by the cumulative exponential distribution function:

$$p(t) = 1 - \exp(-t / \tau) \tag{4.11}$$

Nonvolatile memories require less than one bit-flip during 10 years (~ 10^8 s), or $p(t_{10a}) < 1 / N$, where N is the number of bits in the memory. The required thermal stability factor can be estimated as

$$\Delta = \ln\left(\frac{t_{10a}}{\tau_0} \times \frac{1}{\ln(N / (N-1))} \right). \tag{4.12}$$

For 64 MebiByte memory and an attempt period of 1 ns, the thermal stability factor must be larger than 60 to qualify as a nonvolatile memory. The thermal energy at room temperature is approximately 26 meV; thus, the energy barrier must be larger than 1.56 eV. In practice, the minimum energy barrier is taken at the maximum expected working temperature (~80°C), in this case the energy barrier must be larger than 1.84 eV, or the thermal stability factor $\Delta > 71$ at room temperature.

4.4.1.2.3 Writing and Critical Current

MRAM dissipates energy during writing in the form of Joule heating,

$$P_J = RI^2. \tag{4.13}$$

P_J describes the dissipated power, R the resistance of the MTJ, and I the current. For STT-MTJs, the major dissipation occurs during writing, when the current is large. Thermal stability is modified by the STT current [99,113,114]:

$$\Delta_I(I) = \Delta_I(I = 0) \times \left(1 - \frac{I}{I_c} \right) \tag{4.14}$$

I_c is the critical current density for switching. In microscopic models, it corresponds to the minimum spin torque required to reverse magnetization at absolute zero [113]. Δ_I is not necessarily identical with Δ_H; it has been shown experimentally that Δ_I is

smaller than Δ_H [109]. If the temperature is nonzero, the MTJ can switch by thermal fluctuations, even if $I < I_c$. Obviously, also reducing the barrier leads to an increase in switching probability. If one bit is written once every 100 ns for 10 years (3×10^{15} write operations), the probability of *not switching* must be below 3×10^{-16} ($=1/3\times10^{15}$). The necessary current as a function of pulse time can be estimated from

$$I(t_p) = I_c \times \left(1 - \frac{1}{\Delta_I(I=0)} \ln\left(\frac{t_p}{\tau_0} \times \frac{1}{\ln(1/p)}\right)\right). \tag{4.15}$$

Considering the assumptions from before, I / I_c must be larger than 0.986 ($\Delta_I = 71$). The above formular is valid for thermally activated switching regimes (a few ns upwards). For shorter switching times, there is not sufficient time for thermal excitations to aid the switching process and the switching changes towards the purely STT driven precessional switching regime with a steeper current increase for shorter switching times [114]. Fast, reliable switching requires that the current is close to or larger than the critical current. The critical current depends on the layer design, such as in-plane or perpendicular. For in-plane design, the critical current [21,96] is given by:

$$I_{c_{\text{in-plane}}} = \left(\frac{2q}{\hbar}\right) \times \left(\frac{\alpha}{\eta}\right) \times (2E_b + \mu_0 M_s^2 V_F / 2). \tag{4.16}$$

q describes the elementary charge, $\hbar$ denotes the reduced Planck constant, α is the phenomenological Gilbert damping constant, and η the polarizing factor or spin-transfer efficiency. η depends on the spin polarization P and direction [115]:

$$\eta(P,\theta) = \frac{P}{2(1+P^2\cos(\theta))} \tag{4.17}$$

$\theta = 0$ describes the parallel and $\theta = \pi$ the anti-parallel state. η assumes its smallest value for the parallel state (large I_c). For the perpendicular design, the critical current is given by

$$I_{c_{\text{perpendicular}}} = \left(\frac{2q}{\hbar}\right) \times \left(\frac{\alpha}{\eta}\right) \times 2E_b. \tag{4.18}$$

Comparing the critical currents for in-plane and perpendicular designs shows that in-plane designs have an additional energy contribution that must be overcome. This term originates from the fact that the STT, which switches the in-plane magnetization, must move the magnetization out of the layer plane. The related energy barrier is $\mu_0 M_s^2 V_F / 2$ higher than the switching barrier E_b between the major and minor ellipses axis of the layer. Perpendicular designs do not need to overcome this extra energy barrier and, thus, exhibit lower critical currents.

Since both the retention time (Equation 4.10) and the critical current (Equations 4.16 and 4.18) depend on the energy barrier, there is a trade-off between high retention time and low critical current. A corresponding figure of merit for an MTJ design is Δ_H / I_c (the higher the better). The perpendicular design has a higher figure of merit than the in-plane design, if all parameters are the same, since the perpendicular design, unlike the in-plane design, does not have to overcome the demagnetization field.

For a perpendicular layer CoFeB with a damping of 0.005 [93,96], an assumed spin polarization of 60% [104] in parallel state and an energy barrier of 1.8 eV, the critical current is 40 μA and its figure of merit at room temperature (Δ_H / I_c) is 1.7 μA^{-1}. The resistance of an MTJ is on the order of 1–10 kΩ [93]; thus, the voltage and power dissipation when writing is ~100 mV and ~1 μW, respectively. Given the switching time (~10–100 ns), the energy consumed during writing is on the order of 10–100 fJ. Low energy operation (90 fJ write energy) has been experimentally demonstrated [93]. The most important material parameters are damping and polarization.

4.4.1.2.4 Reading and TMR

Reading involves determining if the state is in a LRS or a HRS. The relevant metric is the TMR, given by Equation 4.3. The TMR is microscopically connected to the spin polarization P through Julliere's model, which assumes that spin is conserved during tunneling [32].

$$\frac{\Delta G}{G_p} = \frac{2P^2}{1+P^2} \tag{4.19}$$

G is the conductance ($=1/R$). Using Equation 4.3, Equation 4.19, and some algebra, the polarization can be estimated from the device TMR as

$$P = \sqrt{TMR/(TMR+2)}. \tag{4.20}$$

An infinitely high TMR corresponds to an ideal polarization of 1; thus, high polarization is important for material consideration. Polarization also improves the writability, as previously discussed. The state is read by a sense current that develops a voltage drop across the MTJ. The magnitude of the voltage is used to determine the resistance state. Since a current passes through the MTJ during reading, power is dissipated and its magnetization is excited, which can lead to a read disturb error. A read disturb error is an accidental bit-flip of a memory during the read operation. If one bit is read every 100 ns for 10 years (3×10^{15} read operations), the probability of *switching* must be below 3×10^{-16} ($=1/3\times10^{15}$). The read disturb error is a switching event due to thermal activation over the current reduced barrier. The maximum allowed sense current can be estimated from

$$I(t_p) = I_c \times \left(1 - \frac{1}{\Delta_I(I=0)} \ln\left(\frac{t_p}{\tau_0} \times \frac{1}{\ln(1/(1-p))}\right)\right). \tag{4.21}$$

For a 10 ns read, I/I_c must be smaller than 0.47, for a 1 ns read 0.5 ($\Delta_I = 71$). Using the same values as for writing, the estimated sense voltage and dissipated power is on the order of 10–100 mV and 100 nW–1 μW. The time required to determine the state does not intrinsically depend on the MTJ but on the CMOS sense amplifier. A large difference in resistance between HRS and LRS (corresponds to high TMR) allows trading-off sense amplifier sensitivity to faster reading [96]. If the signal compared to noise is small, then the sense amplifier must be more sensitive and will be comparatively slow [116]. It should be noted that for the most common memory architecture (1T-1R, see Section 4.4.3), the transistor is connected in series with the MTJ when reading. For instance, assuming a transistor impedance of 1 kΩ, an LRS of 1 kΩ and an HRS of 7 kΩ (TMR = 600%), the resistance ratio of the memory cell is 300%.

The reading operation is unipolar for all spintronic designs—only the magnitude of the voltage/current matters, not the sign.

4.4.1.2.5 Density and Scaling

Memory density is arguably the most important metric for commercial products. The density is a measure of the number of bits per area, although it is often given by the number of bits per chip.

The density is not only determined by the size of the MTJ alone, but also by the size of the access device, typically a transistor (see Section 4.4.3). The size of the transistor is primarily determined by its drive current capability, which must be large enough to switch the MTJ (10–100 µA). The transistor width-normalized on-current for a low-power design transistor is about 600 µA/µm or A/m [116,117]. To provide 10–100 µA, the width has to be between 17 and 170 nm. For a hypothetical minimum sized memory cell (1T-1R) with a 20 nm memory half-pitch, the gate length would also be 20 nm (low-power logic transistor) [118]. The respective MTJ must be smaller than 20 nm and its switching current lower than 12 µA.

It is not trivial to take an MTJ design and scale it to smaller size. Looking at Equation 4.5 shows that decreasing the volume will cause a reduction in the energy barrier. To account for this decrease, the magnetic anisotropy strength has to be increased without degrading other parameters, for example like the damping by adding a second interface anisotropy [110]. The energy barrier and the switching current also depend on how the magnetization reversal takes place. Above a certain size (~40–70 nm [21,96]), it is easiest to reverse the magnetization by first nucleating a new domain and then having it grow. However, for decreasing size the magnetization reversal becomes nucleation dominated and the thermal stability factor almost independent of size. The figure of merit Δ_H / I_c improves with decreasing size. Below ~40–70 nm, the magnetic film prefers single-domain states and the entire domain switches instead of first growing a new domain. This is reflected by a saturation in Δ_H / I_c, as predicted by Equations 4.16 and 4.18 [96].

Most reports of MRAM circuits are on the order of Mib [94,95,109,119,120], and a few up to Gib [74,111].

4.4.1.2.6 Harsh Environment

There are applications where the electronics must be able to operate in harsh environments, such as military, vehicular, aerospace, space, and nuclear technology. The demands could be operation at low temperature (−40°C), high temperature (125°C), thermal cycling, and high radiation environment. Low temperature is not an issue for MTJ devices, as functional devices have been demonstrated to operate at liquid helium temperature (4 K). The spin-polarization through the tunneling layer is a function of temperature, and degrades with increasing temperature [121,122]. Nonvolatile operation at high temperature can be maintained as long as the thermal stability factor still exceeds about 60 at operation temperature. Or in other words the energy barrier must be about 30% larger as compared to room temperature (≈2eV or $\Delta_H \approx 78$). MTJs are exceptionally radiation hard. Ionizing radiation cannot cause the magnetization to switch direction; thus, there are no single event upsets (SEU) [123] or loss of information. High enough radiation doses could cause displacement damage in the tunneling layer, which would degrade the overall memory cell. Nevertheless, the real radiation vulnerability lies in the CMOS circuit. CMOS electronics would break at doses below the doses necessary to damage the MTJs [120]. But an SEU can cause transient currents in the CMOS periphery during reading the MTJ, which can lead to bit-flip [124].

4.4.2 Magnetic Random Access Memory

This section covers different designs for spintronic memories. All of them share the same method of reading, the tunneling magnetoresistance effect. What distinguishes the designs is the way the memory state is switched. The designs covered here are thermally-assisted, STT, spin-Hall/spin-orbit, domain wall and finally voltage controlled magnetic anisotropy (VCMA).

4.4.2.1 Thermally-Assisted MRAM

Thermally-assisted (TA) MRAM adds temperature as a controllable variable. The principle is quite simple—the thermal stability factor is smaller at a higher temperature and, therefore, it is easier to switch the state. This allows to design very stable devices at room temperature, without any penalty for writing, because the energy barrier for writing and the energy barrier responsible for the stability are decoupled by temperature.

Taken to the extreme, the device can undergo phase-changes during the writing procedure. If the temperature is higher than the Curie temperature of the storage layer, it becomes paramagnetic. If the storage layer is cooled below the Curie temperature while biased into a state, it magnetizes easily into the biased state. Another design possibility is to couple the storage layer to an AFM. The storage layer can easily be switched, if the AFM is heated above its blocking temperature or Néel temperature (the AFM becomes paramagnetic), but is otherwise very difficult to switch [125]. Such devices are typically heated up to ~200°C.

The devices proposed in [125] are for field-written MRAM, but TA-writing has also been demonstrated for STT-MTJs. The Joule dissipation is used to heat the storage layer (above 150°C). The perpendicular anisotropy of the storage layer is reduced, allowing the STT to bias the storage layer into a state. The anisotropy recovers as it cools down and the storage layer settles into the state it was biased into by the STT [126].

4.4.2.2 Spin-Transfer Torque MRAM

STT-based MRAM is the most mainstream design and was extensively covered in Section 4.4.1. A typical scaled memory device uses a perpendicular CoFeB/MgO/CoFeB stack, thanks to its low damping, high spin polarization, high TMR and low switching current. Gib-density has been demonstrated [74,111] and STT-MRAM is commercially available in density of 32Mib × 8 [95].

4.4.2.3 Spin-Hall/Spin-Orbit MRAM

The two-terminal MTJ suffers from its shared read- and write-path. A large write current can cause degradation in the tunneling layer, while reading can cause read disturb errors. The three-terminal Spin-Hall or Spin-Orbit MRAM offers a way to decouple the writing and reading path. The major benefit is that the properties that determine reading and writing can be optimized independently of each other. The reading is still carried out by the TMR-effect, but the writing is performed by spin injection from a heavy-metal film by utilizing the SHE. The reference layer has one terminal, and the heavy-metal film has two terminals.

The SHE details have been explained in Section 4.2.3. Metals generating a spin-current are Ta [127,128], W [129], Ir-doped Cu [130], and several others [131]. There are differences

between the metals in SHE strength and polarization efficiency. The performance metric is given by the spin Hall angle Θ_{SH}, which is the ratio of spin-current density J_s to charge-current density J_q. For example, Ta has a value of 0.12 [127] and 0.33 for W [129].

Geometric effects can significantly amplify the SHE [131]. The spin-current I_s to charge-current I_q ratio is given by $\Theta_{SH} A_s / A_q$, where A_s is the cross-section of the MTJ ($w_F l_F$) and A_q is the cross-section of the metal film ($d_{Metal} l_F$). Thus, $\Theta_{SH} A_s / A_q = \Theta_{SH} w_F / d_{Metal}$. The metal thickness d_{Metal} is usually several times thinner than the MTJs width w_F. Functional memory devices have been demonstrated in [127–130].

4.4.2.4 Domain Wall MRAM

Like the SHE-MRAM, domain wall MRAM is a three-terminal MRAM device that decouples the writing and reading paths. The reference layer has also one terminal, like SHE-MRAM, but the other two terminals are not connected to a metal film under the MTJ. Instead, they are connected to the storage layer that extends laterally out of the MTJ stack (see Figure 4.12). The storage layer is connected to spin-polarizers at each end. The spin-polarizers comprise ferromagnetic films pinned into opposite spin-states by AFMs. Since the two spin-polarizers have fixed spin-states, two domains form in the magnetic film, which are separated by a DW. When current is injected from a polarizer into the storage layer, the domain grows and the DW moves towards the other end of the layer. Depending on the current direction through the storage layer, the DW can be moved repeatedly back and forth, allowing to deliberately set the magnetization orientation below the MTJ stack either in a parallel or antiparallel orientation with respect to the reference layer [132].

The formation and design of domain walls is a complex topic, depends on the material parameters as well as on the geometry, and is the result of the energy minimization of the magnetic film, where several energy contributions compete with each other (e.g., exchange energy, anisotropy energy, and demagnetization energy). For DW-MRAM, the storage layer's material properties and geometry have been chosen so that the layer sustains stable domain walls. Memory devices based on DWs have been demonstrated [133,134] and there are also designs with more than three terminals [135,136].

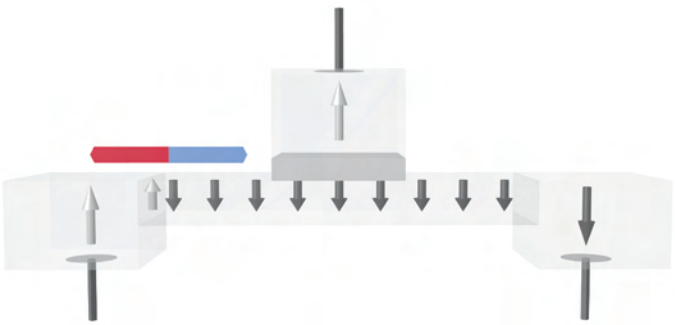

FIGURE 4.12
The DW memory has three leads, one connected to the MTJ reference layer (spin-up) and one to each polarizer. The DW is at the left hand side of the ferromagnetic layer. The spin-down domain encompasses both the right hand side polarizer and the storage layer. The memory is in antiparallel state. If a spin current is injected from the left hand side polarizer into the storage layer, the DW moves to the right and changes the state of the memory.

4.4.2.5 Voltage Controlled Magnetic Anisotropy MRAM

The voltage controlled magnetic anisotropy was discussed in Section 4.2.4, and it offers a new way to control an MTJ. As the free layer thickness scales down, the interface dominates over the bulk. Thin enough films can exhibit a perpendicular net magnetization due to interface effects, as describe in Section 4.4.1. The VCMA is controlled by the application of a voltage or an electric field. It can be described as [62]

$$\sigma_i(V) = \sigma_i(V = 0) - \xi V / d. \tag{4.22}$$

ξ describes the VCMA coefficient, V the applied voltage, and d the thickness of the tunneling barrier. The ξ values for the CoFeB/MgO systems range from 30–100 fJ/Vm [62,67]. The VCMA effect can be used either in conjunction with STT, where it reduces the energy barrier and thus the switching current, or by pure voltage switching by removing the barrier. When the barrier is removed, the magnetization freely precesses between the states, allowing STT-free switching at the physically fastest switching rate [62]. The precessional switching, while extremely fast and energy efficient, is circuit-wise complicated by the nondeterministic end-state (it keeps precessing between the states as long as the voltage pulse is on). The pulse must be very precise to ensure that it toggles into the desired state. Since there is no force driving it into a certain state, the memory must be read after writing to determine if the writing was successful or must be performed again.

4.4.3 Memory Cell Architecture

Memory matrices are typically active matrices, where the memory cell is composed of a selector device and a memory functional device [90]. The selector is a non-linear device that decouples the bit line from the memory functional device, unless selected (cf. Figure 4.13).

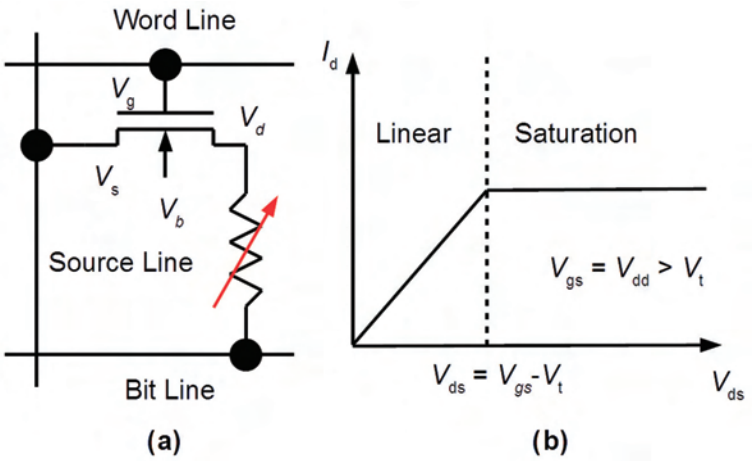

FIGURE 4.13
(a) A 1T-1R memory cell. V_g, V_s, and V_d are connected to the word line, source line, and an MTJ, respectively. The body connection V_b is not connected in this figure, but is usually tied to ground. (b) The simplified transistor output current characteristics. For small V_{ds}, the transistor behaves as a resistor, and, for large V_{ds}, it sinks the maximum amount of current.

Examples of selector devices are diodes (PN, Schottky) and transistors (NPN, NMOS, and PMOS). Diodes are preferred for their smaller size over transistors, but their rectifying property limits the memory functional device to the unipolar class. NMOS and PMOS transistors are used for bipolar class memories. NMOS transistors are preferred over PMOS transistors because they deliver larger currents for a given size due to their higher charge carrier mobility.

The access transistor is a four terminal (gate, source, drain, and body) device for a bulk CMOS process and a three terminal device for a silicon on insulator (SOI) process (gate, source, and drain). The body of the bulk transistor is connected to the lowest potential for an NMOS device (typically ground) and the highest potential for a PMOS device (typically V_{dd}). The transistor is characterized by its threshold voltage V_t. The NMOS transistor is on, when the source-gate voltage $V_{gs} = V_g - V_s$ is larger than V_t and off if smaller than V_t (for the PMOS it is the opposite, and V_t is negative). The maximum current through a long-channel transistor occurs, when the transistor is on ($V_{gs} - V_t = V_{ov} > 0$) and the source-drain voltage $V_{ds} = V_d - V_s$ is larger than the overdrive voltage V_{ov}. The transistor operates in saturation and is approximately independent of V_{ds} as long as the saturation condition is met. Since STT-switched MTJs require large currents, the transistor may operate in saturation during programming. For small V_{ds}, the transistor operates in the linear region and behaves as a resistor with an impedance on the order 100 Ω–1 kΩ. The transistor is operated in the linear region during reading. Figure 4.13 shows the transistor connected to an MTJ and the transistor output current characteristics.

The most basic CMOS circuit has only two potentials, ground and V_{dd}. The power supply depends on the CMOS technology and its intended application, but is in the range of 1.2–3.3 V for submicron transistors. A necessary but not sufficient condition for turning the NMOS transistor on is that the gate potential is V_{dd}. The NMOS transistor can still be off, if the source potential is larger than $V_{dd} - V_t$, since $V_{gs} = V_g - V_s < V_{dd} - (V_{dd} - V_t) = V_t$. This condition can occur for the access NMOS transistor, if it tries to source a large current to a large resistor, such as in the case of programming an MTJ with high resistance. The equivalent case for a PMOS transistor solution is when it tries to sink a current. This condition is known as source degeneration. There are several ways to avoid this. A charge pump can boost the gate voltage to $V_{dd} + V_t$, in such case, a full V_{dd} voltage-drop can be applied to the MTJ. But the charge pump solution is less preferably, as it consumes extra overhead area, power, and adds circuit complexity [99]. The largest current occurs during writing P→AP, when the current is sourced through the reference layer. For this case, it is best to connect the highest potential to the reference layer, or in other words, to connect the reference layer to the bit line. Consequently, the free layer is then connected to the drain of the NMOS transistor, which sinks current to the source line during the P→AP transition. Another solution is to use a PMOS transistor [91], where the drain is connected to the reference layer. The PMOS transistor will not have any source degeneration, when it sources the current during the P→AP transition, since the source is connected to the highest potential.

MRAM devices can be separated into devices with unipolar and bipolar switching. Most, but not all, MRAM devices are two-terminal devices. If there are multiple terminals, they are typically connected to different transistors. As such, MRAM can be realized by several memory cell architectures, such as 1D-1R, 1T-1R, 2T-1R, or 2T-2R (D = Diode, T = Transistor, R = Resistor, sometimes referred to as MTJ in literature). There are even more memory cell architectures, like 6T-2R, which will be briefly covered in Section 4.7.

1D-1R: This is the smallest memory cell for spin-based memories, with a minimum cell size of $4F^2$. F refers to the half-pitch in DRAM memory (2F = width + spacing = pitch), and is connected to the minimum lithographic feature size. It requires that the MTJ itself is not larger than $4F^2$ and can be placed on-top of the diode. A requirement of this memory cell is that the MTJ allows unipolar switching, which is possible for the orthogonal MTJ design (cf. [137,138]) and devices using VCMA [62]. The cell is selected (selector in low-impedance state), when there is a voltage drop across the diode (about 0.2 V for a Schottky and 0.7 V for a PN).

1T-1R: This is the standard memory cell for spin-based memories, shown in Figure 4.13. The 1T-1R is superficially similar to the 1T-1C of the DRAM. The densest DRAM cell uses an open architecture with a transistor size of $6F^2$. The size is minimized by having one contact shared between two transistors. It has been argued that the 1T-1R cell can be as small as $6F^2$ at the 90 nm node by [99], $9F^2$ at 45 nm feature size [74], and $22F^2$ was demonstrated at 28 nm feature size [111].

2T-1R: This cell design is used for three-terminal spintronic devices, like SHE-MRAM (Section 4.4.2.3) and DW-MRAM (Section 4.4.2.4). The size is larger or equal to $12F^2$, as transistors cannot share their contacts [134]. These devices target SRAM replacement instead of DRAM replacement [135].

2T-2R: This cell should be interpreted as 2×1T-1R. It dedicates "two" 1T-1R cells to store the data and their complement. The minimum size is larger or equal to $12F^2$. The memory density is about half of designs with1T-1R cells. This is a major disadvantage, but the design offers some performance advantages. The storing of both the data and its complement effectively doubles the read signal and allows to trade sensitivity for fast differential reading (see Section 4.4.1.2). It is also very robust to process variations. The performance of individual MTJs is strongly correlated to their locality, because MTJs near each other are more likely to show the same performance compared to MTJs further apart. As such, the R_P and R_{AP} of the two MTJs are very likely a close match, which almost guarantees correct reading. For example, it is highly unlikely that the R_P of one MTJ is as high as the R_{AP} of the adjacent MTJ, or conversely that the R_{AP} is as low as the R_P of the adjacent MTJ. For large arrays, the spread of values of R_P and R_{AP} in 1T-1R designs must be very small (i.e., $20\sigma < \bar{R}_{AP} - \bar{R}_P$ [96,99]) to ensure that $\min(R_{AP})$ of the array can never be misinterpreted as parallel state, and that $\max(R_P)$ of the array is not misinterpreted as antiparallel state. An example of a 2T-2R design can be found in [94], using a 90 nm CMOS process.

4.5 Spintronic Logic

As explained in the previous sections spintronic devices, in particular MTJs, are very promising for memory applications due to their nonvolatility, CMOS-compatibility, fast operation, and (nearly) unlimited endurance. But they are by no means limited to pure memory applications, which is reflected in the ITRS [118], where it is suggested to exploit nonvolatile devices to circumvent current limits of state-of-the-art logic circuits. Among

the many challenges in current CMOS technology development, the introduction of nonvolatile elements into logic circuits, allows to tackle the issue of the exponentially growing standby power dissipation [139]. Within the smorgasbord of available memory technologies STT-switched devices are especially appealing for logic applications [25,140–151].

4.5.1 Logic-in-Memory

Logic-in-Memory supplements the logic circuit plane by adding nonvolatile elements [152–155]. This way instant-on and more importantly an energy efficient transition between the shut down state and the active state are possible, but at the same time also the circuit complexity and the layout footprint increases. Typical application scenarios are in microprocessors and field programmable gate arrays [156]. Microprocessors are already incorporating various power reducing technologies and operation schemes (e.g., reduced operation voltage, clock gating, and power gating), but the power reduction commonly comes at the price of reduced performance. The more energy is saved, the longer it takes to enter into and to exit from the power saving mode. Introducing nonvolatile flip flops [157], or STT-MRAM [158], speeds up this transitions considerably and allows more frequent transitions into the power saving states as well as into deeper sleep states, resulting in a reduction of the total system power without degrading performance [159,160]. The second application area are field programmable gate arrays (FPGAs). They belong to the most popular reconfigurable hardware platforms and are employed for rapid prototyping and as a generic hardware for mapping arbitrary applications [161]. Commonly, they consist of elementary logic functions (lookup tables), which are connected through wire segments and programmable switches. The content of the lookup tables and the states of the programmable switches are fully defined by the bits stored in the configuration memory. Currently, there are two main groups of FPGAs, SRAM-based that store the configuration in SRAM memory cells and flash or anti-fuse FPGAs that employ nonvolatile memory for storing the configuration [162]. SRAM-based FPGAs are very fast, but need an additional nonvolatile off-chip storage for storing the configuration. Therefore, their startup is rather slow and takes around 100 ms. Additionally, SRAM cells have a big footprint in comparison to other memroy cells. In contrast, anti-fuse and flash-based FPGAs have a smaller footprint and startup faster, but anti-fuse FPGAs can only be programmed once and flash-based FPGAs have a very slow and energy consuming writing. MTJ/CMOS hybrid FPGA designs combine the advantageous features of both technologies without their drawbacks. They make the off-chip nonvolatile memory superfluous, which allows a very fast boot process and reduces the design complexity at the chip level, while featuring at the same time the speed of SRAM-based FPGAs and (partial) run-time reconfigurability. Another benefit of the transition to MTJs is the improved single event upset reliability of the resulting FPGAs. Especially for the deep-submicron technology nodes, this has become a concern [163]. Since the first proposal to use 100 nm thermally-assisted MTJs in combination with 130 nm CMOs technology to build a nonvolatile FPGA by Bruchon et al. [164] in 2006, a wide variety of publications picking up the idea and trying to enhance FPGAs from circuits up to the architectural level has followed [165–170]. The naive approach to simply replace the SRAM cells and flip flops in the FPGAs with nonvolatile counter parts suffers under area and leakage current increase due to the additional required components to read and write the MTJs [171,172]. Therefore, Suzuki et al. [170,173,174] proposed a six-input lookup table circuit with shared write driver and sense amplifiers in combination with redundant MTJs to decrease the influence of resistance variations and

improve the programmability. In the remainder of this section, we focus on the spintronic logic proposals that use the spin-based device as the main logic element and replace a CMOS-based logic block rather than acting as a complement. This paves the way for realizing intrinsic logic-in-memory architectures.

4.5.2 Spin-Transfer Logic

The dissipated power and the interconnection delay are central issues that have far-reaching implications throughout the digital ecosystem [118,175]. Nowadays, the static power consumption is minimized by shutting down unused circuit parts. Even though this strategy is simple and effective, it bears the disadvantage of loosing all the information stored in the circuit through dissipation. Therefore, it must be copied back into the circuit when it is brought online again, which adds delay and power consumption. A way to avoid this, is to use nonvolatile elements in the circuits. Spintronics exhibits a number of features that make it very attractive for such nonvolatile elements and circuits. Among the currently available multitude of ideas the technology readiness level for commercialization strongly varies [25,176] and despite the availability of many candidates for potential CMOS successors, CMOS will be around forever. Even more the upcoming generation of widespread commercially available products within the next few years will be nonvolatile CMOS MTJ hybrids [25,177–180]. In fact, STT-MRAM is already available on the market and many more applications will very likely follow soon [95,181]. Even though the CMOS MTJ hybrid solutions progress fast and that they are already competitive with respect to speed and power consumption in comparison to pure CMOS, at one of the essential features that guaranteed CMOS success, its integration density, the current solutions are still inferior. In principle, STT-MRAM is suited for high integration density and it is already three-dimensionally integrated at the BEOL, but it still suffers under relatively high switching currents for the MTJs, which limits the minimum useable transistor size. This led to the investigation of alternative switching mechanisms, such as the spin Hall effect, to surpass this limit [182,183]. The exploitation of STT-MRAMs for Compute-in-Memory (see Section 4.5.7) applications is very appealing due to their potential for high integration densities as well as the exploration of novel computation concepts, but they all remain limited by the same boundaries as the state-of-the-art STT-MRAM. To overcome these obstacles, researchers are also investigating alternatives to push the achievable integration densities beyond todays limits, i.g. [25].

A way to increase density is to put as much as possible of the CMOS functionality into the spintronic devices. The result of such efforts are the proposal of a nonvolatile magnetic flip flop (NVMFF) and a nonvolatile magnetic shift register [184]. The nonvolatile flip flop exploits spin-transfer torques and magnetic exchange coupling within its free layer to perform the actual computation instead of relying on external CMOS transistors. Thereby it is possible to reduce the number of required transistors, reduce the structural complexity, and take advantage of the resulting very dense layout footprint. Rigorous simulation studies were carried out to explore the capabilities as well as the limits of the NVMFF [185–189]. Additionally, the NVMFF can be combined with a STT majority gate in order to create a novel nonvolatile buffered magnetic gate grid.

4.5.2.1 Nonvolatile Magnetic Flip Flop

Flip flops belong to the group of sequential logic circuits and are an essential part of modern digital electronics [190]. Thus, the nonvolatile magnetic flip flop is a fundamental building block required in the creation of a nonvolatile STT computation environment.

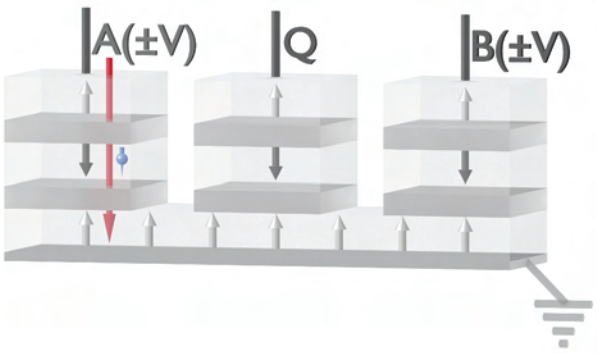

FIGURE 4.14
The nonvolatile magnetic flip flop comprises three MTJ or spin valve stacks that share a common magnetic free layer. It is operated by two simultaneously applied current pulses at its inputs *A* and *B*. Logic "0" and "1" are encoded via the pulse polarity and the result of each operation is stored in the common free layer as the layer's magnetization orientation. The information stored in the flip flop is accessible through its output *Q* as a high or low resistance state by exploiting either the GMR or the TMR effect.

Therefore, we will first explain how a single NVMFF works and use this knowledge later as basis for more complex applications, such as a nonvolatile shift register or a nonvolatile buffered gate grid. The NVMFF comprises three antiferromagnetically coupled polarizer stacks with perpendicular magnetization orientation (see Figure 4.14). The polarizer stacks are connected with each other through nonmagnetic interconnection layers (e.g., MgO, Al_2O_3 or Cu) and a common free layer with perpendicular magnetization orientation. One of the stacks is used for readout Q and the remaining two are dedicated to input *A* and *B*. Due to the anti-ferromagnetic nature of the polarizer stacks it is assumed that their stray field is negligible. The information is stored as magnetization orientation of the shared free layer and accessible via GMR or TMR effect. Depending on the relative orientation between the magnetization orientation of the shared free layer and the readout stack Q a high resistance state HRS (antiparallel) or a low resistance state LRS (parallel) is measured. The respective HRS and LRS are assigned to logic "0" and logic "1," respectively. For the operation of a single NVMFF, the polarity of the input pulses is mapped to logic "0" and "1." If now, a negative voltage is applied to one of the inputs (i.e., *A*), then electrons will flow from the leads through the polarizer stack, where they align with the local magnetization orientation, and eventually enter the common free layer before they get absorbed by the grounded bottom contact. During their time in the common free layer, the electrons relax to the free layers magnetization orientation. This creates a localized torque in the region where the electrons traverse, which depends on the pulse polarity and the relative orientation between the layers. Depending on the electrons polarization orientation the exerted torque either tries to push the magnetization into its other stable position or damps the magnetization precessions and stabilizes its current orientation. For the operation of the flip flop, two synchronous input pulses are applied to the two inputs *A* and *B*. Both pulses exert an STT on the common free layer. For fixed parallel magnetization orientations of the two input stacks and two input pulse polarities, four input combinations are feasible. Depending on the input pulse polarities the two created STTs either add up and accelerate the switching (same polarity) or counter act each other and damp the switching (opposing polarities). Translating this behavior to a logic table shows that the device can be SET/RESET (same polarity) as well as HOLD its current

FIGURE 4.15
A shift register consists of flip flops that are connected in series in order to pass the information stored in one flip flop to its subsequent neighbor. To create this kind of functionality, the nonvolatile flip flops are arranged in two rows in two distinct levels. The free layer of every flip flop overlaps at its boundaries with its neighbor flip flops on the respective other level. The polarizer stack in the middle of the flip flops is exploited for the generation of an auxiliary (clocked) STT.

state, which is exactly required for sequential logic as flip flops and latches [190]. In comparison to other ideas in this field, the key advantage of the nonvolatile magnetic flip flops is its very small footprint. But, in general, a single flip flop by itself is of limited use. Only when it is seamlessly integratable into bigger circuits without compromising the overall integration density, it is of practical value. Therefore, it was investigated how one can build bigger structures like a shift register out of the flip flops without degrading the overall integration density. It is essential to keep as much as possible of the required functionality in the spintronic domain in order to sustain the achieved integration density and the key to this is to directly copy the information from one flip flop's free layer into a subsequent free layer (see Figure 4.15).

4.5.2.2 Nonvolatile Magnetic Shift Register

The copy operation is achieved by first traversing an unpolarized current through the layer that is read (cf. Figure 4.16, Free Layer 2 overlapping region) and exploit the afterwards orientation encoded spin polarized electrons in the subsequent layer (Free Layer 1) to exert a spin-transfer torque on the local magnetization in the region where they enter. This way it is possible to pass directly the information from one device to the next without complex external CMOS blocks. As explained in Section 4.5.3, there are always two torques when the electrons interact with the local magnetization. One acts on the electrons while the other acts on the magnetization. Therefore, when the electrons are polarized in the read layer (i.e., Free Layer 2), there is always a torque that destabilizes the magnetization of the free layer and might cause a read error. The solution for this problem is to speed up the

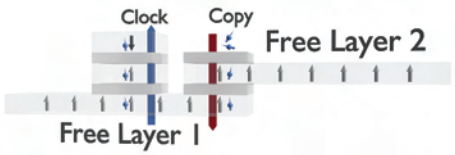

FIGURE 4.16
The n-Bit shift register from Figure 4.15 has been reduced to a 2-Bit shift register, in order to reduce the computational effort. During the copy operation, an unpolarized current is pushed through Free Layer 2. The with the orientation of Free Layer 2 encoded electrons enter Free Layer 1, where they exert a spin-transfer torque on the magnetization of the layer. The auxiliary pulse through the clock stack creates a second spin-transfer torque that speeds up the copy operation by either damping or enforcing the switching of the magnetization in Free Layer 1.

switching of the written layer (i.e., Free Layer 1) by adding a second auxiliary STT. Thereby, the copy operation will require less time than it takes to cause a read disturbance. The concept was tested by an extensive set of simulations. To keep the computational effort on a manageable level, the n-Bit shift register was reduced to a 2-Bit shift register and rigorous simulation studies were carried out to at first test the idea [191] and later check its limits with respect to manufacturing related misalignment [192,193]. It was not only found that the concept works, but that the structures are even capable of tolerating moderate in-plane as well as out-of-plane misalignment.

4.5.2.3 Nonvolatile Buffered Magnetic Gate Grid

A further example for the possible application of the flip flop is its use in a nonvolatile buffered gate grid [189], which, like the shift register, takes advantage of passing directly the stored information from one free layer to the next. To create the nonvolatile buffered gate grid, one needs an extra ingredient, the STT majority gate. The majority gate employs the same material stack for the free layer and the polarizers as the flip flop and is also based on the same information encoding principle via input polarity [185,194]. Therefore, the flip flop and the majority gate can be synergetically combined into bigger circuits. Since both devices are similar, the focus will be on explaining the differences between these two and how they interact. First of all the STT majority gate belongs to the class of combinational logic devices, while the flip flop belongs to the class of sequential logic devices. Both types are essential for building a computing environment and complement each other with their functionalities. The most obvious structural difference between them is that the free layer of the STT majority gate is cross shaped and features four instead of three polarizer stacks (cf. Figure 4.17). Three of the polarizer stacks *A*, *B*, and *C* are used as inputs and one polarizer stack *Q* is used for readout. The STT majority gate is operated via three synchronous polarity encoded input pulses and the final orientation of the free layer is defined by the majority of the input signals. One must mention that it is crucial that the number of applied inputs is odd. Otherwise, it can happen that the number of "0" and "1" input signals are equal, and the created torques perfectly balance each other (assuming equal input currents and equal torque strength), which leads to an undefined state after the operation. Only when an odd number of inputs is applied, there is one uncompensated torque during

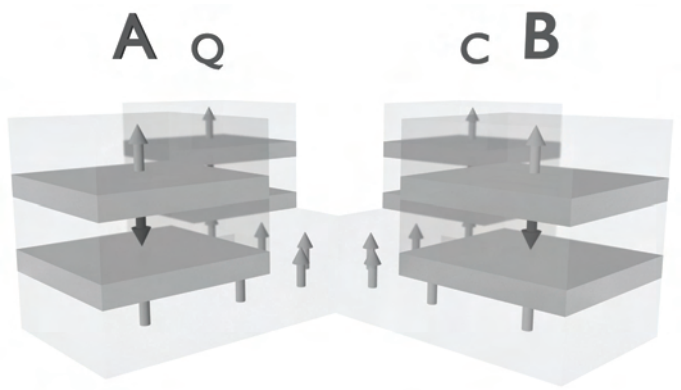

FIGURE 4.17
The STT majority gate comprises four equidistantly spaced legs. Each of the legs exhibits a polarizer stack and is connected through an interconnection layer to a common cross shaped free layer. One of the stacks is dedicated to readout *Q* and the remaining three *A*, *B*, and *C* are employed as inputs.

operation left, which will decide the final state. Another important feature for building arbitrary logic functions is functional completeness. In CMOS logic circuits, the NAND and NOR gates are widely employed due to their functional completeness. Looking at the truth table of the majority function shows that it consists of a two-input AND and a two-input OR gate, when one of the inputs is fixed to logic "0" and "1," respectively. Therefore, the NOT operation must be added in order to reach functional completeness. The easiest way to introduce the NOT operation is to invert the acting torque by inverting the polarity of the input signal.

By combining the STT majority gates and the nonvolatile flip flops into a buffered gate grid, the resulting circuit is not only CMOS compatible and able to complement CMOS logic, but also one achieves much more. Namely, the communication between the (external) memory and the logic is significantly decreased and the auxiliary CMOS circuits for the signal conversion between the CMOS and the spintronic domain become redundant, which in turn greatly improves the omnipresent leakage power and interconnection delay problems [10,139,176]. The devices are periodically distributed over the die plane and positioned in two separate levels with zones where they overlap with their neighbor devices in the respective other level (see Figure 4.18). Adding contacts at the top and the bottom of the overlapping regions allows to directly copy the stored information from one free layer to the next, the same way as for the shift register explained before. The resulting structure is highly regular, allows parallel execution of operations, and brings the advantage of a shared buffered between adjacent logic gates. The synergetic combination of all the features allows to keep the integration density high, while at the same time the energy and time spent for the information transport are minimized. Even more, it also enables the investigation of computing alternatives to the nowadays performance limiting Von Neumann architecture, where the computation units and the memory are physically separated and the information is continuously pushed back and forth between them. Furthermore, this structure gives considerable freedom in allocating the employed resources and it is very easy to reconfigure its logic; that is, the number of operating gates and buffers can be adjusted on the fly depending on the current computing task. To give an idea of how this nonvolatile buffered gate grid can be exploited in practice, the example of an easily concatenable one-bit full adder (cf. Figure 4.19) will be discussed in the following.

FIGURE 4.18
The nonvolatile buffered gate grid is formed by a periodic continuation of the STT majority gates and nonvolatile flip flops. The nonvolatile flip flops (rectangles) act as shared buffers and the STT majority gates (crosses) perform the calculations.

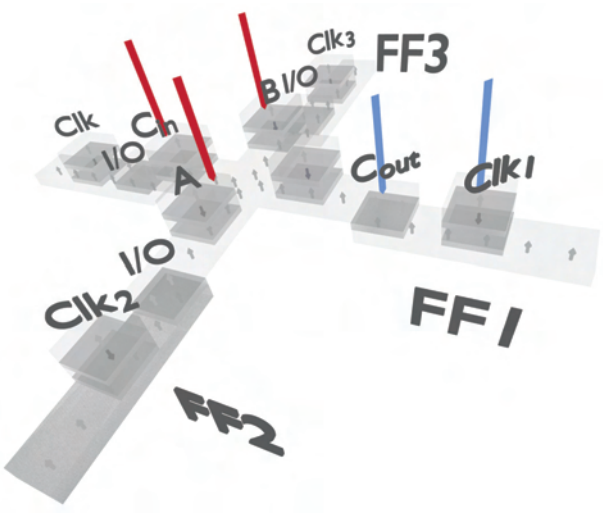

FIGURE 4.19
A single node of the buffered magnetic gate grid comprising a single majority gate and three flip flops is already capable to perform the calculations of a concatenable one-bit full adder. As for the shift register, the key for this is the exploitation of the devices' free layers as polarizers.

For the one-bit full adder three inputs, A, B, and C_{in} (carry in from a previous adder stage) and two outputs Sum and C_{out} are assumed. Sum is given by [190]:

$$\begin{aligned}\text{Sum} &= A\ XOR\ B\ XOR\ C_{\text{in}} \\ &= A\cdot B\cdot C_{\text{in}} + A\cdot \overline{B}\cdot \overline{C}_{\text{in}} + \overline{A}\cdot B\cdot \overline{C}_{\text{in}} + \overline{A}\cdot \overline{B}\cdot C_{\text{in}}\end{aligned} \tag{4.23}$$

C_{out} denotes the carry out and takes care of the overflow into the next digit for a multi-bit addition:

$$\begin{aligned}C_{\text{out}} &= MAJORITY(A,B,C_{\text{in}}) \\ &= A\cdot B + A\cdot C_{\text{in}} + B\cdot C_{\text{in}}\end{aligned} \tag{4.24}$$

In order to perform both calculations on a single majority gate one has to translate them into a sequence of *MAJORITY*, *NOT*, and copy operations. Since the *MAJORITY* function and the *NOT* form a functional complete basis, there is a well-defined sequence that achieves the calculation of SUM and C_{out}. For instance, as first step $MAJORITY(A,B,C_{\text{in}})$ is performed and the result is copied into the first buffer *FF*1 (see Figure 4.19). Then $MAJORITY(A,B,NOT(C_{\text{in}}))$ is performed and its result is stored in the second buffer *FF*2. Now, in the final step, the information contained in *FF*1 and *FF*2 is combined through $MAJORITY(NOT(FF1),FF2,C_{\text{in}})$ to calculate the Sum and to copy it into *FF*3. At the end of this sequence, Sum is stored in *FF*3 and C_{out} is contained in *FF*1. Since the results are safely stored in the buffers *FF*1 and *FF*3, they can be exploited for further calculations in their neighbor gates. For example, the C_{out} stored in *FF*1 can be used as carry in the next one-bit adder stage (e.g., majority gate at the right side of the central gate), even before the Sum calculation in the initial stage has been finished. This illustrates the parallelization potential of the structure and how the expensive information transport over a common bus can be minimized.

Straightforwardly, one can build a one-bit full adder without the proposed buffering [195]. However, without the buffers, it is much harder to generalize the layout and fit it into large scale integration schemes and it suffers under further drawbacks, which led to the proposal of an alternative solution with in-plane magnetization [196]. This alterative approach employs an all-spin logic inspired hybrid shift register and a stacking scheme that is similar to a previously proposed shift register [184,186]. Their exploitation of in-plane instead of out-of-plane magnetization also requires a redesign of the majority gate, which was realized by a ring structure.

4.5.3 All-Spin Logic

The direction of the spin transport is often tied to the direction of the charge transport, but by nature spin and charge transport are independent. Behin-Aein et al. proposed a type of spintronic logic that takes advantage of this fact and coined the term "All-Spin Logic" (ASL) [141,197,198]. This type of logic employs magnets to store logic information and to create spin polarized signals. The magnets are connected via nonmagnetic conducting channels in order to propagate spin signals between them (see Figure 4.20). These structures feature pure spin signal transport and can be exploited for sequential as well as combinational logic [141,199–201].

The proposal of this very interesting idea triggered a broad spectrum of activities to explore the different aspects of the concept. For example, ways to create and operate sequential logic, like a shift register and a ring oscillator, have been investigated in [200]. The scaling properties and the energy delay of ASL devices are investigated in [198,202]. The optimization of the device structure including interconnect materials and their respective advantages and disadvantages has been studied in [203–211]. A further important step for the progress in the field was the development of a generalized framework for modeling spintronic devices on the circuit level [212]. One of the key features that makes ASL attractive is the consequent avoidance of charge transport and by that a significant reduction in the dissipated power.

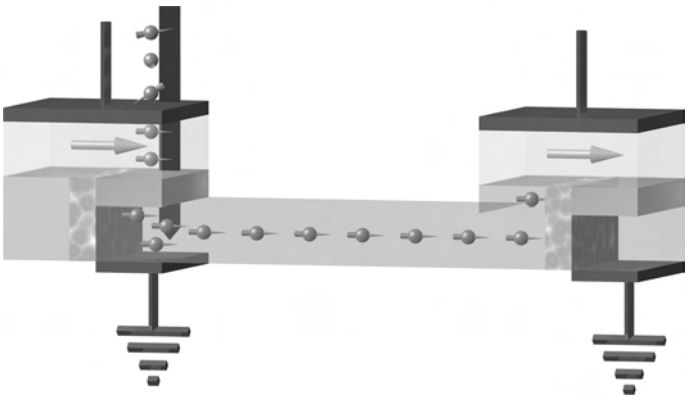

FIGURE 4.20
The magnets (boxes with white arrows) are used to store logic information (magnetization orientation) and to create spin polarized signals. Electrons, entering from the top electrode, are polarized when they move through the magnet and create a spin accumulation at the bottom electrode after they passed an oxide layer. This accumulation drives a spin diffusive current that reaches the neighbor magnet, where it relaxes and creates a spin-transfer torque able to switch the magnetization. This way a pure spin signal, encoded with the magnetization orientation of the magnet, is created and exploited to copy information from one magnet to another (left to right).

However, current estimates for the power consumption are worse than for state-of-the-art CMOS circuits [10,176,208]. This is not specific to ASL and shared by many other spintronic technologies, which can be easily explained by the head start of many decades for CMOS technology in research and development. Nevertheless, we feel confident that over time with growing knowledge and experience in the field of spintronics the gap will not only be diminished, but that spintronics will even substitute CMOS electronics for certain applications. In order to be able to study and explore ASL circuits larger than a few gates, one has to simplify their description and translate the device behavior into compact models. Many of these compact models employ the assumption that the magnets can be described by a single macro-spin [207,210,212–214]. It is obvious that the quality of the gained results on the circuit level crucially depends on the physical accuracy of the employed compact models. The findings of Verma et al. [215] show that the macro-spin assumption, which relies on a uniform precession and switching of the magnetization, is not valid. It has been further demonstrated that the current flow through the magnet and the related STT is strongly nonuniform. This translates into a significant influence on the overall switching behavior of the magnet and therefore must be incorporated in the compact models. An additional effect commonly ignored is the pairwise occurrence of the spin-transfer torques. If one pushes electrons through a magnetic layer to polarize them, not only the electrons experience a torque that aligns them to the local magnetization. There is always a simultaneously acting back torque that acts on the magnetic layer and destabilizes the magnet, thus causing a read error [216]. Therefore, the influence of these effects must be quantified and considered in the compact model description to gain meaningful ASL circuit modeling and analysis.

4.5.4 Domain Wall Logic

The creation and manipulation of magnetic domain walls via spin polarized currents for storing information and realizing logic has been a very hot topic for many years [134,217–227]. Since many of the domain wall related logic ideas are similar, we pick All-Metallic Logic (mLogic) [225,226] as a representative for this class of logic and discuss its basic features in the following. The basic mLogic device is shown in Figure 4.21 and comprises a free layer holding a domain wall sandwiched between two fixed oppositely magnetized polarizers (bottom of structure). The free layer is coupled to an adjacent free magnetic layer through a coupling layer (mottled layer) and its state can be accessed through the GMR stacks on the left and right side, which connect it to the leads R and R'. If one applies a current through the W^+ and W^-, the electrons will first pass a polarizer stack and subsequently exert a spin-transfer torque that pushes the domain wall along the layer. By changing the polarity of the applied current, the domain wall can be reversibly moved back and forth through the free layer. Due to the coupling between the upper and the lower free layer, the magnetization orientation of the upper layer follows accordingly. The logic state of the device is accessible through the GMR stacks, which are connected to the upper free layer, and their respective low and high resistance states depend on the free layers' orientation. The advantage of this gate is that it mimics CMOS behavior (n- and p-type by swapping input ports), allowing for the reuse of CMOS circuit design and replacing the n-type and p-type transistors by corresponding mLogic gates. The all-metallic structure also enables very small supply voltages. However, it also can cause high leakage currents and lead to degraded energy efficiency. Of course, it is also possible to create domain wall logic with simpler structures by cascading, for example DW memory cells (cf. Section 4.4.2.4), but it comes at the price of coupling the read and write paths of the devices. Thus, the control currents must pass the tunneling oxides, which has implications on wear and supply voltage [221,222,224].

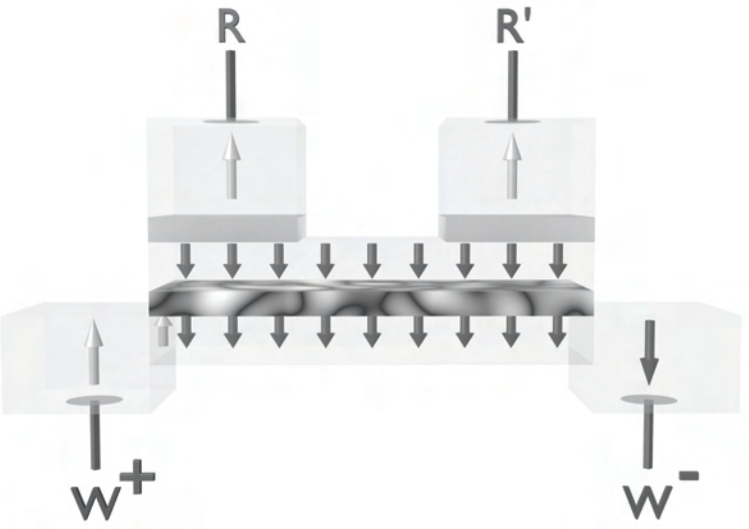

FIGURE 4.21
The mLogic device exhibits separate read and write paths. The writing path is formed by the free layer at the bottom of the structure and its two adjacent polarizers. Pushing a current through W^+ and W^- moves the domain wall (left corner) through the free layer. The read path is formed by the upper free layer and the two polarizer stacks at its ends. Upper and lower free layer interact through an insulating coupling layer (mottled layer).

4.5.5 Reprogrammable Logic

To exploit magnetic devices as computing elements and provide logic-in-memory, it has been shown that the use of direct communication between STT-MTJs can realize the basic Boolean logic operations. The experimental demonstration of two-input and three-input reprogrammable logic gates (Figure 4.22) to implement AND, OR, NAND, NOR, and the Majority operations is reported in [142] and [143]. A Boolean logic operation is executed

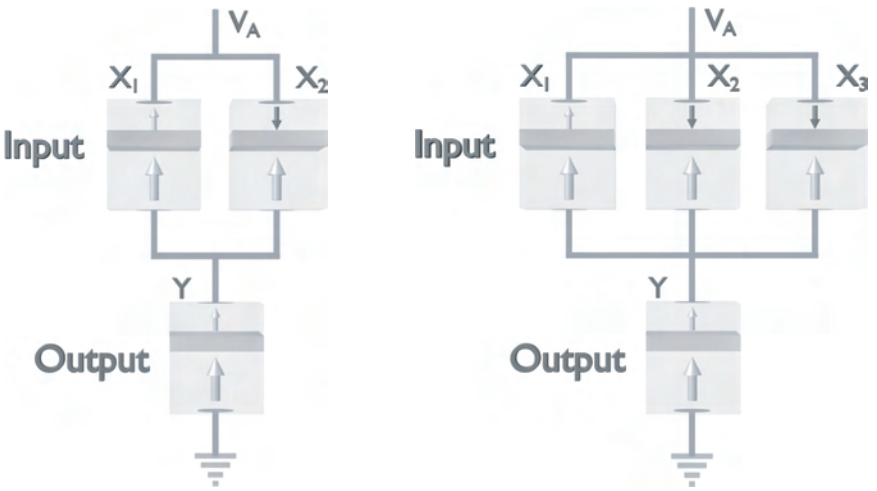

FIGURE 4.22
STT-MTJ-based two-input (left) and three-input (right) reprogrammable logic gates. X_i (Y) shows an input (output) MTJ.

in two sequential steps. These steps comprise an appropriate preset operation (parallel or antiparallel state) in the output MTJ. Then a voltage pulse (V_A) with a proper amplitude is applied to the gate. Depending on the logic states of the input MTJs (X_i), the preset in the output MTJ (Y), and the voltage level applied to the gate, a conditional switching behavior in the output MTJ is provided, which corresponds to a particular logic operation.

Tables 4.1 and 4.2 illustrate how the AND and OR operation and NAND and NOR operation, respectively, are performed using the two-input reprogrammable gate in two steps. The HRS and the LRS correspond to logical 0 and 1, respectively and the variable x_i and y represent the logic state of the input (X_i) and output (Y) MTJs. In order to perform a logic operation, first a preset of $y = 1$ or $y = 0$ is performed in the output MTJ and then in the following step a proper voltage level ($V_A < 0$ or $V_A > 0$ is applied to the gate to enforce the desired (high-to-low or low-to-high) resistance switching event in the output MTJ, which corresponds to a logic operation (i.e., AND/OR or NAND/NOR). The value of the voltage V_A has to be optimized to ensure a reliable conditional switching behavior of the output MTJ for any possible input pattern [228]. In fact, this optimization is required for any logic operation to maximize (minimize) the switching probability in the output MTJ ($P \to 1$ or $P \to 0$), when it is a desired (an undesired) switching event in Step 2. One should note that the switching probability of any input MTJ is negligible as the current flowing through the output MTJ splits between the input MTJs, and their currents are below the critical current required for the STT switching. Therefore, the logic state of the input MTJs is left unchanged.

TABLE 4.1

The realized conditional switching behavior is equivalent to the AND and OR operations with a preset of $y = 1$. Using the two-input reprogrammable gate.

			$y' \leftarrow x_1$ AND x_2		$y' \leftarrow x_1$ OR x_2	
Input Patterns			**Step 1**	**Step 2**	**Step 1**	**Step 2**
State	x_1	x_2	y	y'	y	y'
1	LRS (0)	LRS (0)	HRS (1)	**LRS (0)**	HRS (1)	**LRS (0)**
2	LRS (0)	HRS (1)	HRS (1)	**LRS (0)**	HRS (1)	HRS (1)
3	HRS (1)	LRS (0)	HRS (1)	**LRS (0)**	HRS (1)	HRS (1)
4	HRS (1)	HRS (1)	HRS (1)	HRS (1)	HRS (1)	HRS (1)

Desired switching events in the output (y′) are indicated by boldface type.

TABLE 4.2

The realized conditional switching behavior is equivalent to the NAND and NOR operations with a preset of $y = 0$. Using the two-input reprogrammable gate.

			$y' \leftarrow x_1$ NAND x_2		$y' \leftarrow x_1$ NOR x_2	
Input Patterns			**Step 1**	**Step 2**	**Step 1**	**Step 2**
State	x_1	x_2	y	y'	y	y'
1	LRS (0)	LRS (0)	LRS (0)	**HRS (1)**	LRS (0)	**HRS (1)**
2	LRS (0)	HRS (1)	LRS (0)	**HRS (1)**	LRS (0)	LRS (0)
3	HRS (1)	LRS (0)	LRS (0)	**HRS (1)**	LRS (0)	LRS (0)
4	HRS (1)	HRS (1)	LRS (0)	LRS (0)	LRS (0)	LRS (0)

Desired switching events in the output (y′) are indicated by boldface type.

Because of the easy integration with CMOS, the reprogrammable gates are generalizable to provide stateful logic arrays for large-scale logic circuit applications. In fact, unlike the ASL, which is based on spin-current in a spin-coherent channel, reprogrammable logic is based on an electric current to apply conditional switching at the output and, therefore, the logic operation is not limited to physically adjacent magnetic elements. This is an important feature for complex logic applications as discussed later.

4.5.6 Implication Logic

Material implication (IMP) is a fundamental two-input (e.g., s and t) Boolean logic operation ($s \rightarrow t$), which reads "s implies t" or "if s, then t," and is equivalent to "(NOT s) OR t." The IMP operation has been classified as one of the four basic logic operations by Whitehead and Russell [229], but has been ignored in digital electronics as Shannon founded modern digital electronics based on AND, OR, and NOT operations [230]. Only recently has it received renewed attention, when it was demonstrated that memristive switches intrinsically enable the IMP operation in a crossbar array of TiO_2 memristive switches [231]. Table 4.3 shows the truth tables of the basic implication operations, IMP and negated IMP (NIMP).

The MTJ-based realization of the IMP operation was demonstrated in [145] and it has been shown that the MTJ-based implication logic gate (Figure 4.23) significantly improves

TABLE 4.3

Truth table of IMP and NIMP operations.

State	$s\ t$	$s \rightarrow t$	$\overline{t \rightarrow s}$
1	0 0	1	0
2	0 1	1	1
3	1 0	0	0
4	1 1	1	0

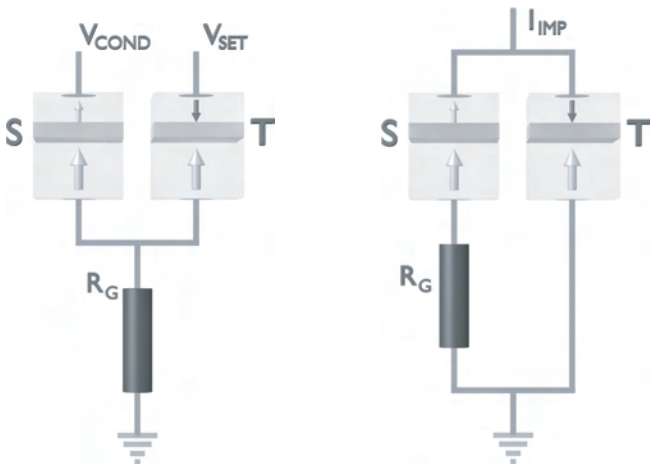

FIGURE 4.23
Voltage-controlled (left) and current-controlled (right) STT-MTJ-based implication logic gates.

the reliability of the MTJ-based logic as compared to the reprogrammable gates [145]. It has been shown that all three-input as well as two-input OR and NOR reprogrammable gates suffer from high error probability and, therefore, cannot provide reliable logic operation [228]. In fact, as reliability is an essential prerequisite to realize spin-based logic, the implication logic is a promising alternative.

Figure 4.23 shows the circuit topologies of the implication gates [145]. In both gates, two STT-MTJs are combined with a simple resistor R_G, where the initial resistance states of the source (S) and target (T) MTJs (logic variable s and t) act as the logic inputs of the gate. The final resistance state of T (t') is the logic output of the gate. The logic operation ($t' = s \rightarrow t$) is performed by simultaneous application of two voltage pulses (V_{SET} and V_{COND}) in the voltage-controlled gate or the application of the current I_{imp} in the current-controlled gate. When these voltage or current pulses are applied, a conditional switching behavior in T is provided, depending on the resistance state of the MTJs S and T (Table 4.4). Such a switching behavior corresponds to the IMP or NIMP (negated IMP) operation (Table 4.3). If we define HRS ≡ 1 and LRS ≡ 0 (the convention of Shannon), the logic output of the implication gate corresponds to the NIMP operation.

$$\{t' = t \text{ NIMP } s\} \equiv \overline{t \rightarrow s} \equiv \{t' = t.\bar{s} = t \text{ AND } \bar{s}\} \tag{4.25}$$

t' is the final state of the variable t after the operation. In combination with the TRUE operation (here low-to-high resistance switching), the NIMP operation forms a complete logic basis to compute any Boolean function. Therefore, stateful logic is enabled as MTJs are simultaneously used as nonvolatile memory and logic elements. The universal NOR and NAND operations, for example, can be performed in three and five sequential steps, respectively.

$$\begin{aligned}
&\text{Step 1 (TRUE):} && a = 1 \\
&\text{Step 2 (NIMP):} && \overline{a \rightarrow b} \equiv \{a' = a.\bar{b} = \bar{b}\} \\
&\text{Step 3 (NIMP):} && \overline{a \rightarrow c} \equiv \{a' = a.\bar{c} = \bar{b}.\bar{c} = \overline{b + c} = b \text{ NOR } c\}
\end{aligned} \tag{4.26}$$

TABLE 4.4

The realized conditional switching behavior is equivalent to the operation IMP or NIMP. Depending on the definitions for the HRS and LRS as logical "0" and "1".

	Implication Operation (Conditional Switching)		**HRS ≡ 0, LRS ≡ 1**			**HRS ≡ 1, LRS ≡ 0**		
			$t' = s \rightarrow t$			$t' = \overline{t \rightarrow s}$		
State	$s\ t$	$s'\ t'$	s	t	t'	s	t	t'
1	HRS HRS	HRS **LRS**	0	0	**1**	1	1	**0**
2	HRS LRS	HRS LRS	0	1	1	1	0	0
3	LRS HRS	LRS HRS	1	0	0	0	1	1
4	LRS LRS	LRS LRS	1	1	1	0	0	0

$$\begin{aligned}
&\text{Step 1 (TRUE):} \quad a = 1 \\
&\text{Step 2 (NIMP):} \quad \overline{a \rightarrow b} \equiv \{a' = a.\bar{b} = \bar{b}\} \\
&\text{Step 3 (NIMP):} \quad \overline{c \rightarrow a} \equiv \{c' = c.\bar{a} = c.b\} \\
&\text{Step 4 (TRUE):} \quad a = 1 \\
&\text{Step 5 (NIMP):} \quad \overline{a \rightarrow c} \equiv \{a' = a.\bar{c} = \overline{c.b} = b \text{ NAND } c\}
\end{aligned} \tag{4.27}$$

Here, a (a') indicates the initial (final) variable equivalent to the resistance state of an auxiliary MTJ storing the logic result of intermediary steps and the final result of stateful NAND and NOR operations.

It has been shown that the implication logic outperforms the conventional Boolean logic based on reprogrammable gates from both reliability and power consumption point of views [232]. In addition, a combination of implication logic and the reprogrammable logic reduces the number of required logic steps implementing complex logic functions [233]. Therefore, the total time and the energy consumption can be decreased at the cost of higher error probability [233].

4.5.7 Compute-in-Memory

An important issue of nonvolatile logic, the fan-out, needs to be addressed to generalize the intrinsic logic-in-memory proposals in order to perform complex logic functions and for large-scale logic circuits. When the input and output of memory elements are physically connected to form a logic gate, additional connection elements could disturb the correct logic operation (e.g., conditional switching behavior in MTJ gates). Therefore, the extension of the logic gates to provide more complex functions is problematic. In fact, highly localized computations limit the possibility of performing logic operations among data located in arbitrary parts of the circuit. Therefore, intermediate circuitry is usually required to perform additional read/write operations increasing the complexity, energy consumption, and delay. There is a lot of effort to offer compute-in-memory capabilities in large-scale implementing complex functions [234–239].

This issue appears unsolvable in all-spin logic as it is based on spin-current. However, the reprogrammable and implication gates are based on electric current and, therefore, extendable to stateful arrays without being limited to physically adjacent elements [234,235]. This makes MTJ-based logic very promising, especially when MTJs with high TMR are available to guarantee reliable operation with negligible error probabilities.

In previous sections, it has been described how direct communication between STT-MTJs via reprogrammable and implication logic gates realizes intrinsic logic-in-memory architectures and extends the functionality of nonvolatile memory circuits to incorporate logic computations.

It has been shown that by replacing the MTJ devices with one-transistor/one-MTJ cells (see Figure 4.6), the reprogrammable and implication logic gates can be realized in MRAM arrays [234,235]. Since the 1T/1MTJ cell is the basic building block for STT-MRAM structures [24,240], an STT-MRAM array can be used not only as memory, but also as magnetic logic circuit for the development of innovative nonvolatile large-scale logic architectures [234,235]. The realization of the MTJ gates in STT-MRAM arrays

enables the extension of nonvolatile MRAM from memory to logical computing applications and eliminates the need for sensing amplifiers and intermediate circuitry as compared to other hybrid CMOS/MTJ nonvolatile logic proposals, where the MTJs are used only for nonvolatile storage.

4.6 Spin-Torque Oscillator

Oscillators are important devices ubiquitously needed for many applications [190] and the STT-effect can be exploited to build oscillators. Commonly a spin-torque oscillator (STO) is built as a GMR-pillar or an MTJ. Thus, the GMR or the TMR effect can be used to detect the magnetization oscillation as a high frequency voltage. The precession frequency of STOs is tunable over a wide range of frequencies 5–46 GHz by a DC current as well as by the application of an external magnetic field, which makes them very competitive in comparison to voltage controlled oscillators and Yttrium garnet oscillators [241–244]. They are also very small. STOs are over fifty times smaller than a standard LC-tank voltage controlled oscillator due to the very large required inductor footprint [245]. Their large operation frequency, small size, and low power consumption is very attractive for several microwave-based applications, like broadband oscillators [241–244], fast modulators [246–251], and sensitive field/current detectors [252].

There are several ways to categorize STOs. We focus here on their structure and distinguish between nano-contact oscillators, where the current enters though a nano-constriction into an extended magnetic structure and nano-pillar STT oscillators (spin valve or MTJ stack). Nano-contact STOs can be further differentiated by their number of contacts and have been demonstrated for different geometries [253–255]. The nano-pillar STOs can be subdivided into two categories, depending on the magnetization orientation of the free layer: "out-of-plane" with the magnetization perpendicular to the layer and "in-plane" with the magnetization parallel to the layer. Looking at STOs with nano-pillars and in-plane magnetization [256] reveals on one hand high frequency capabilities, but on the other hand the prerequisite of a large external magnetic field and low output power levels [257]. In contrast, oscillators with an out-of-plane magnetization of the free layer [258] are able to oscillate without an external magnetic field, but suffer under relatively low output power. Additionally, they typically feature lower operation frequencies ($\leq$2 GHz), which limits their potential application as tunable oscillators [257].

Makarov et al. [259,260] proposed a bias-field-free STT oscillator with in-plane MgO MTJ, elliptical cross-section, and nonperfect overlap between the free and the fixed layers. This structure exhibits the drawbacks of a weak frequency dependence on the current density and a narrow range of frequencies. A way around these limitations is to use an alternative structure, which employs two MTJ stacks that share a common free layer (cf. Figure 4.24; similar to the NVMFF). This structure allows stable high frequency oscillations without the need of an external magnetic field and its operation frequency is widely tunable by varying the current density through the MTJs [261,262]. In [263], it could be demonstrated that in such a structure oscillations up to $\approx$ 30 GHz are achievable. As further investigations have shown, the structure based on two MTJs with a common shared free layer also exhibits stable oscillations with an out-of-plane magnetization orientation of the free layer [264].

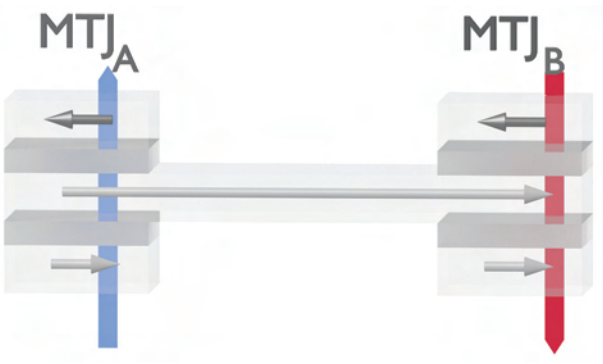

FIGURE 4.24
This structure exploits one MTJ for driving the oscillations, while the other prevents switching and relaxation into a stable state (opposite current direction). This way large stable oscillations of the common free layer can be not only sustained, but steered over a wide frequency range.

In general, the output power of current STOs is not sufficient for practical applications yet. Commonly the output power for GMR-based STOs lies in the sub-nW range. CoFeB/MgO/CoFeB based nano-pillar structures achieve higher output power, but still remain in the nW range [265–268]. In order to overcome this problem, the synchronization of several STOs has been proposed [248,254,269–276]. Another solution is to use an external microwave current or field to injection lock the synchronization [277–281]. Parametric synchronization with an external microwave field frequency close to twice the STO's free frequency has been reported, a bit more recently [281–284] and benefits from the advantage that the measurement is not interfered by the external signal. First experimental observation of parametric excitation in a nano-contact STO at cryogenic temperatures and an excitation frequency of twice the STO's free frequency was achieved by a separately manufactured strip line on top of the STO [285]. Bortolotti et al. [286] were able to parametrically excite vortex gyration by passing a microwave current through a vortex-based MTJ-STO with a sufficing Ørsted field strength at room temperature. A very encouraging result was shown by Sani et al. [254] in 2013. They were able to mutually synchronize three nano-contact STOs. Nevertheless, even under ideal conditions the parametric excitation only shows imperfect locking and the output power as well as the phase noise need further improvement [287].

The above mentioned STOs exploit magnetically hard layers to polarize the electrons before they interact with the free layer to drive precessions. But it is also possible to take advantage of the spin Hall effect for the polarization of the electrons to build spin Hall nano-oscillators (SHNOs). An SHNO comprises a nonmagnetic layer with a strong spin-orbit coupling adjacent to a magnetic layer. These devices are able to create microwave signals in the range of 2–10 GHz, which is appealing for applications in the telecommunication domain. These SHNOs work with pure spin signals (cf. Section 4.2.3), only require little power, operate in a wide range of frequencies, and are rather small ($\leq$5 µm) in comparison to state-of-the-art technologies. Several SHNO devices in a variety of geometries have been manufactured and their operation was properly demonstrated, such as a disk with triangular contacts (nano-gap) [288,289], a nano-wire [290], and a nano-constriction [291]. It has been demonstrated that relatively large power and small auto-oscillation linewidth are possible for a localized spin current injection at

cryogenic temperatures in 2013 [288]. Unfortunately, both features decrease considerably at elevated temperatures due to the availability of additional modes and the arising thermal mode hopping [291]. These problems can be avoided by deliberately exciting a single mode; that is, by adjusting the geometric area of the auto-oscillation zone. One would intuitively expect that the auto-oscillation area is correlated to the experimental setup, like the spin injection geometry, but as it turns out the control of the auto-oscillation characteristics is rather tricky [292]. The local injection of a spin signal into a continuous magnetic film causes the spontaneous excitation of the bullet auto-oscillation mode [293] and the dimensions of the "bullet" is governed by nonlinear self-localization effects and not the spin injection area [289,294].

4.7 Applications

In this final section we highlight a few showcases for spintronic computing, which are likely to be commercialized in the next few years.

4.7.1 Random Number Generator

Since the magnetization of MTJs experiences thermal excitations, their switching shows stochastic behavior and the switching probability of MTJs is governed by the applied current amplitude. This is commonly considered as an effect that has to be controlled by careful circuit design, but one can make a virtue out of necessity by exploiting it for the physical realization of a random number generator [295]. In 2013, a first spin-based random-number generator (spin dice) was built by employing a conventional in-plane MTJ and a current adjusted to achieve 50% switching probability [72]. Unfortunately, in-plane MTJs suffer of a rather small magnetic field range for bistable states and demand high switching current densities, which caused problems in the practical realization of the spin dice [296]. The next generation utilizes MTJs with perpendicular free layer and a perpendicular synthetic antiferromagnetic bottom reference layer [295,296]. Besides the well known random number generator applications, like Monte Carlo simulations and cryptography, they can also be used to improve analog-to-digital information conversion systems for low energy applications. Lee et al. [297] proposed a very interesting voltage-controlled stochastic oscillator for event-driven random sampling. Due to the exploitation of a VCMA and their deliberately reduced thermal barrier, they are able to reduce the power consumption by more than three times and improve the area efficiency even by a factor of 20 in comparison to the state-of-the-art.

4.7.2 Ternary Content-Addressable Memory

Content addressable memory (CAM) is the kind of technology that people use every day, but commonly are completely unaware of its existence. Even more, modern databases and search engines, like Google, could not offer high-speed access to data without them. In contrast to RAM, where the user sends an address to the RAM and gets a data word in return, CAMs get a data word from the user, search their entire memory for the data word and, if such entries exist, return a list of addresses where the data word is stored [298]. These memories are designed in a way that they can search their entire memory within

one operation, which makes them very fast but at the same time expensive. The added search capability is realized by additional comparison circuitry in each memory cell, which causes a high power consumption and a considerably increased memory cell footprint. A ternary CAM (TCAM) extends the functionality of binary CAMs (BCAMs) by adding a third search option "X"—do not care, which gives more freedom for search queries but adds additional complexity to the circuit design [299]. The combination of rising demand for (T)CAMs together with their high energy consumption and large layout footprint makes them very attractive candidates for spintronic complementation. For instance, Govindaraj et al. [300] proposed a 6T 2 STT-MTJ-based NOR-TCAM in 2015 and lately another 9T 2 STT-MTJ based NAND TCAM in 2017 [301]. Considering that a typical CMOS only TCAM cell exhibits 16 transistors, this is a big step forward with respect to integration density and dissipated power. There are TCAMs with smaller memory cell size, like 4T-2MTJ TCAM [302], 3T-2DW BCAM [303], or even 2T-2MTJs [304]. They all feature significantly smaller memory cells and offer zero standby power, but depending on the application scenario and the overhead complexity one is able to afford, one or another of these designs will prevail [300,301].

4.7.3 Spin-Transfer Torque Compute-in-Memory (STT-CiM)

One very recent and interesting proposal for a STT-based Compute-in-Memory design was presented by Jain et al. [305]. They suggest to take advantage of the resistive nature of the STT-MRAM cells to perform a range of arithmetic, bitwise, and complex vector operations. The trick is to enable multiple word lines simultaneously and sense the effective resistance of all enabled cells in each bit-line in order to directly perform logic functions dependent on the values stored in the cells. Such a scheme is not feasible in SRAMs, because it would cause short circuit paths, but, since the STT-MRAM cells are intrinsically resistors, this problem does not appear. This idea is not new (Section 4.5.7), but the implementation simultaneously addresses process variation issues and allows arithmetic and complex vector operations without modifying either the bit-cell or the data array. The bundle of adjustments on different levels (sensing scheme, error correction scheme, and extension of the instruction set) cumulates in an average 4× performance improvement and simultaneous memory system energy reduction.

4.8 Conclusion and Outlook

In this chapter, we tried to give an overview about the many facets of CMOS compatible spintronics and its importance for future beyond Von Neumann computing. Especially STT-switched MTJs have not only become so mature that off-the-shelf MRAM is already available, but the technology as a whole including the process know-how reached a level that we are confident that first CMOS MTJ hybrids for logic applications will be brought to market very soon. However, MTJs of course also have issues like the still rather high switching currents, reduction of damping, increased thermal stability, and device variability. There are ideas to circumvent (some of) these problems via the spin Hall effect, domain wall motion, or voltage controlled magnetic anisotropies. But domain wall-based MRAM and spin Hall MRAM are by nature three terminal devices and, therefore, require more space, while the voltage controlled magnetic anisotropy coefficient needs a boost

to make it compatible with advanced CMOS transistors. STT oscillators are an essential building block for digital electronics and show great potential due to their large operation frequencies, small size, and low power consumption. Currently, they suffer under too low output power for many applications, but there are niches where they already can shine like in STO-based random number generators and analog-to-digital information conversion systems for low energy applications.

Overall one can see a gradual evolution on all levels (materials, processing, devices, circuits, and architectures). This evolution drove the introduction of STT-MRAM into market and will also lead to first spintronic logic and later beyond Von Neumann products. Most likely, this will happen in high performance computing and database hardware, where reduced cooling power and less power consumption immediately brings a big advantage in operating expenses for high performance computation clusters and big server farms. TCAMs with their rather big and complex memory cells as well as their high power dissipation in combination with their crucial role in modern data base applications are perfect replacement candidates. Also FPGAs have a high potential to boost their performance with spintronic logic and will help to familiarize the current generation of developers and engineers with the next generations spintronic technology. FPGAs are very important due to their widespread application in aerospace, medical electronics, application-specific integratet circuit (ASIC) prototyping, digital signal processing, image processing, consumer electronics, high performance computing, scientific instruments, data mining, and many more. They also open up the next step towards the huge system-on-chip market. More disruptive approaches try to draw from the unique advantages of spintronics and break up the CMOS dominance. For example, ASL or STT logic will take off later, when the CMOS MTJ hybrid logic ecosystem has been established and the companies as well as the market are ready for the next more powerful technology generation. In summary, we can see that spintronics managed to become mature enough for first real products, like STT-MRAM, and we are confident that it will not stop there and a plethora of nonvolatile spin-based logic is going to appear within the next 5–10 years on the market.

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