Reliability and Thermal Stability of MoS_2 FETs with Ultrathin CaF_2 Insulators

Yu.Yu. Illarionov[1,2], A.G. Banshchikov[2], D.K. Polyushkin[1], S. Wachter[1], M.I. Vexler[2], N.S. Sokolov[2], T. Mueller[1], T. Grasser[1]
[1]TU Wien, Vienna , Austria [2]Ioffe Institute, St-Petersburg, Russia

Two-dimensional (2D) materials can potentially provide a route to overcome the limitations of Si technologies by enabling nanoscale more than Moore FETs. Fabrication of these devices requires *i*) 2D semiconductors with sizable bandgaps and high carrier mobilities and *ii*) competitive insulators to separate the channel from the gate. However, up to now attention has been mostly paid to the channel materials, while insulators fully suitable for 2D FETs have not been identified. For instance, native oxides of 2D semiconductors, which would go along with them as well as SiO_2 goes with Si, either do not exist or cannot be easily synthesized. As a result, 2D FETs currently face the same problems as many other emerging technologies (e.g. Ge, III-V or GaN FETs), and commercial devices do not yet exist.

The absence of native insulators for 2D FETs requires the use of other materials. The most obvious of them are oxides known from Si technologies (e.g. SiO_2, Al_2O_3, HfO_2), which have been used in most 2D FETs. However, despite a respectable performance of some devices, the typical thickness of the oxides used ranges from tens to even hundreds of nanometers. When being scaled down to the equivalent oxide thicknesses (EOT) below 1nm, as required for end-of-the-roadmap devices, these oxides become amorphous. Thus, their interfaces with 2D channels are of poor quality and contain numerous defects which degrade the performance and reliability of 2D FETs. Another solution is the use of 2D insulators which form well-defined van der Waals interfaces with 2D channels. The best known of them is hBN which indeed resulted in the improvement of 2D FETs. However, when scaled down to several nanometers thickness, hBN exhibits significant tunnel leakage currents. This is due to the moderate dielectric properties ($\varepsilon < 5$, $E_G = 6$ eV) of hBN, which appears to be unsuitable for scaling. As for other 2D insulators, such as mica or oxide nanosheets, their usability in devices has not been demonstrated.

As an alternative, we have recently suggested to use calcium fluoride (CaF_2) as an insulator for 2D devices [1]. Few-nanometers thin CaF_2 layers can be grown on Si(111) by molecular beam epitaxy (MBE) which forms an F-terminated inert surface with no dangling bonds [2]. This results in a quasi van der Waals interface with 2D materials (Fig.1a), similar to those formed by hBN. Furthermore, due to its good dielectric properties ($\varepsilon = 8.43$, $E_G = 12.1$eV), the tunnel currents through CaF_2 are lower than for most high-k oxides with equal EOT, not to mention SiO_2 and hBN.

We fabricated hundreds of CVD-grown MoS_2 FETs with epitaxial CaF_2 insulators of record-small thickness of only about 2 nm (EOT less than 1nm), see Fig.1b. The gate currents in our devices are small compared to the drain current (Fig.1c). Thus, already in the first bare channel prototypes we achieve competitive on/off current ratios of up to 10^7 and SS down to 90 mV/dec (Fig.2a). At the same time, the hysteresis in our devices is even smaller than in Al_2O_3 encapsulated SiO_2(25nm)/MoS_2 FETs [3] (Fig.2b). In Fig.2c we compare the hysteresis widths normalized by the insulator field factor $\Delta V_G/d_{ins}$, where ΔV_G is the width of the gate voltage sweep range and d_{ins} the insulator thickness. For CaF_2 the hysteresis is comparable to that in Si/high-k FETs.

In Fig.3 we show the results for bias-temperature instabilities (BTI) in our CaF_2(2nm)/MoS_2 FETs. The negative BTI (NBTI, Fig.3a) and positive BTI (PBTI, Fig.3b) at insulator fields which are typically used for 2D FETs (2.5 to 5MV/cm) are relatively weak. This is likely due to the lack of insulator defects in the crystalline CaF_2 insulator. However, PBTI stress at the insulator field of 7.5MV/cm leads to a negative drift of the threshold voltage (Fig.3c). This kind of degradation has never been observed for 2D FETs with thick insulators, which routinely operate at lower insulator fields. Recently we found that the negative V_{th} shift after PBTI stress observed in our CaF_2/MoS_2 FETs is very similar to that in MoS_2 FETs with 4nm thick hBN insulators [4]. Thus, we suggest that this is due to the activation of breakdown mechanisms in ultrathin insulators. However, we note that a reasonable on current in our CaF_2/MoS_2 FETs can be achieved already at a gate voltage of 1V (F_{ins} of 5MV/cm), allowing safe device operation.

We also analyzed the thermal stability of our devices and found that it strongly depends on the quality of the MoS_2 channel. If the CVD-grown MoS_2 film is formed by few nanometers sized grains (Process 1, Fig.4a), baking of the devices at 100°C introduces a strong hysteresis (Fig.4b). However, this hysteresis is observed only when using small sweep times t_{sw} and disappears for slow sweeps (Fig.4c). We suggest that the origin of this behavior is thermally enhanced creation of S vacancies in MoS_2. These S vacancies can cause a hysteresis when interacting with adsorbates [5], which can penetrate to the CaF_2/MoS_2 interface through the numerous grain boundaries in the small grain MoS_2. In contrast to charge trapping by slow insulator defects, which seems to be missing in CaF_2, interaction between S vacancies and adsorbates is a fast process. This explains the fast sweep hysteresis which we observe. In contrast, in the CaF_2/MoS_2 FETs with larger grains of the MoS_2 film (Process 2, Fig.5a) the hysteresis remains small even after baking at 165°C (Fig.5b), though a negative shift of V_{th} attributed to the creation of S vacancies is present. However, these S vacancies remain passive, since the number of grain boundaries in large grain MoS_2 is small and thus the penetration of adsorbates to the interface is less efficient. At the same time, the number of active defects in crystalline CaF_2 is small, independently of the MoS_2 quality. Thus, the hysteresis in our Process 2 devices remains small within the whole range of sweep times, while being smaller than in Al_2O_3 encapsulated SiO_2(25nm)/MoS_2 FETs (Fig.5c).

In summary, we examined the reliability and thermal stability of the MoS_2 FETs with CaF_2 insulators of record small 2nm thickness. We found that the virtually defect-free nature of CaF_2 insulators leads to a small hysteresis and BTI, while the thermal stability of our devices strongly depends on the quality of the MoS_2 channel.

[1] Yu.Yu. Illarionov *et al*, "Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors", Nature Electron., 2019.

[2] A. Koma *et al*, "Heteroepitaxy of a two-dimensional material on a threedimensional material", Appl. Surf. Sci., vol. 41, 451–456, 1990.

[3] Yu.Yu. Illarionov *et al*, "Improved Hysteresis and Reliability of MoS_2 Transistors with High-Quality CVD Growth and Al_2O_3 Encapsulation", IEEE Electron Device Lett., vol. 38, 1763–1766, 2017.

[4] Yu.Yu. Illarionov *et al*, "Reliability of scalable MoS_2 FETs with 2 nm Crystalline CaF_2 Insulators", 2D Mater. , 2019.

[5] A. Di Bartolomeo *et al*, "Hysteresis in the transfer characteristics of MoS_2 transistors", 2D Mater., vol. 5, 015014, 2017.

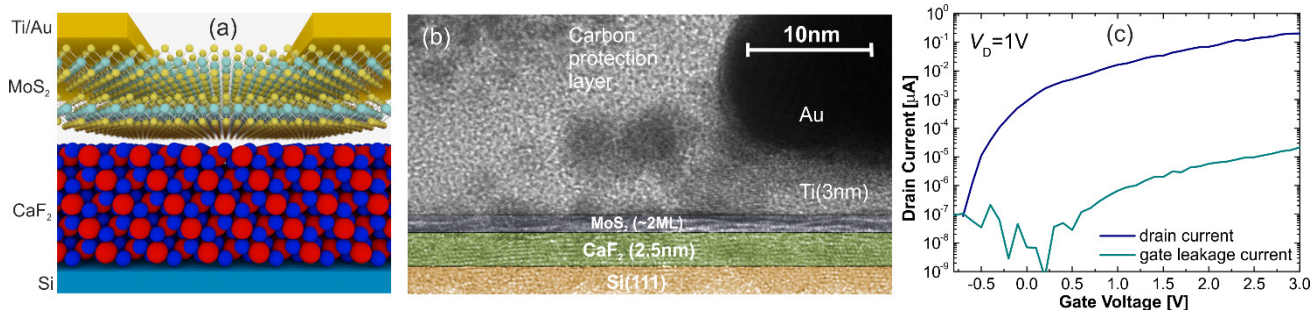

Fig.1. (a) Schematic device layout. (b) TEM image of the channel area. (c) Drain current and gate leakage current vs. gate voltage.

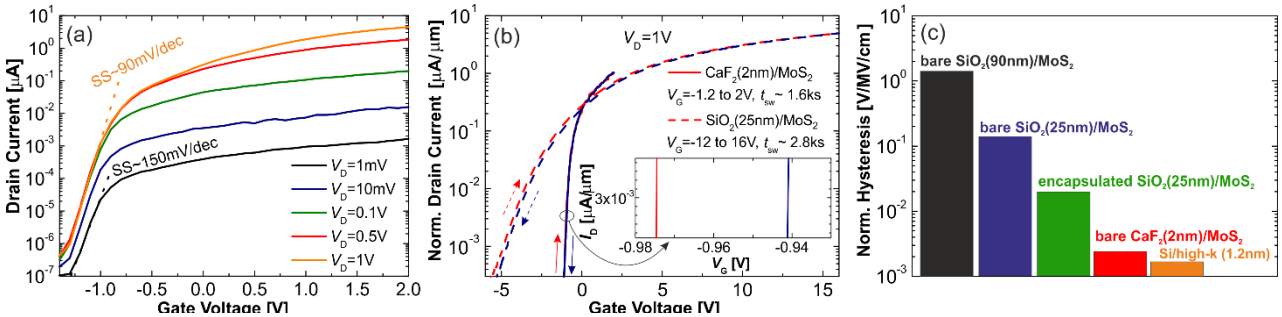

Fig.2. (a) The I_D-V_G characteristics of our CaF_2/MoS_2 FETs. (b) Slow sweep I_D-V_G characteristics of the CaF_2/MoS_2 and SiO_2/MoS_2 FETs. (c) Comparison of the hysteresis width normalized by the insulator field factor for different MoS_2 FETs and Si/high-k devices.

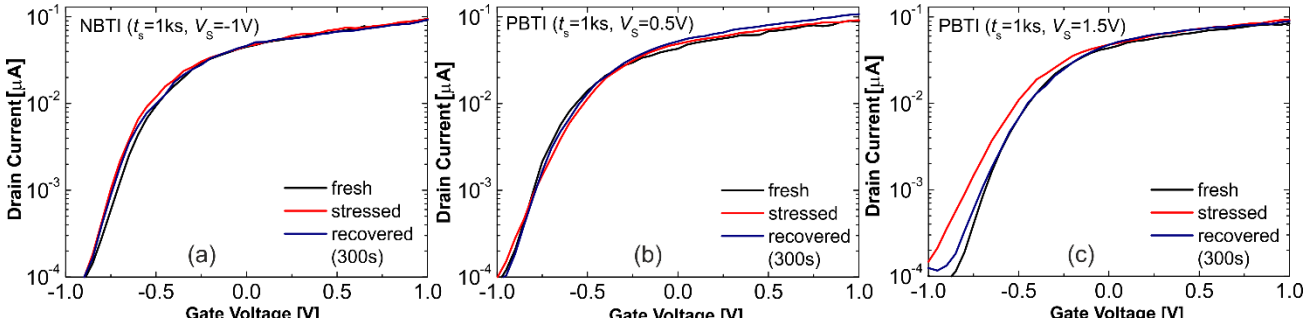

Fig.3. NBTI (a) and PBTI (b,c) in our CaF_2/MoS_2 FETs. A negative V_{th} shift (c) appears after PBTI stress at V_S=1.5V (F_{ins}=7.5MV/cm).

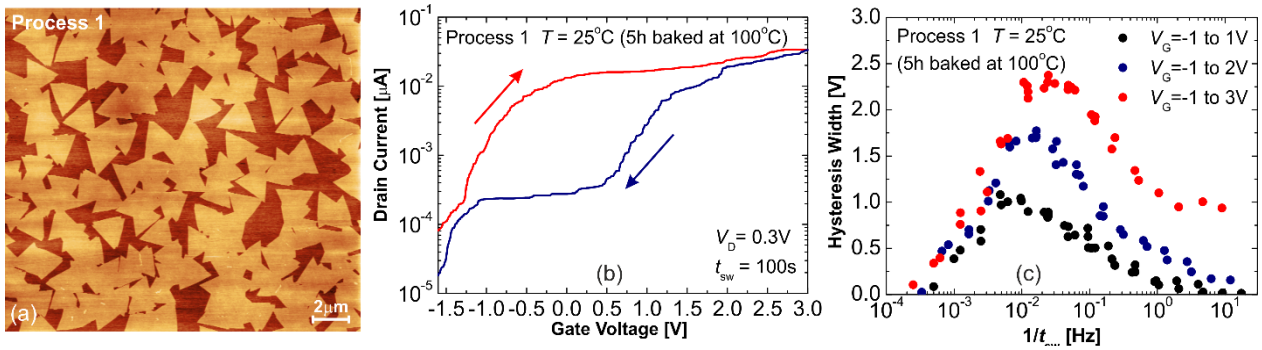

Fig.4. (a) AFM image of the Process 1 MoS_2 film. Fast sweep hysteresis (b) and $\Delta V_H(1/t_{sw})$ dependences (c) after baking at 100°C.

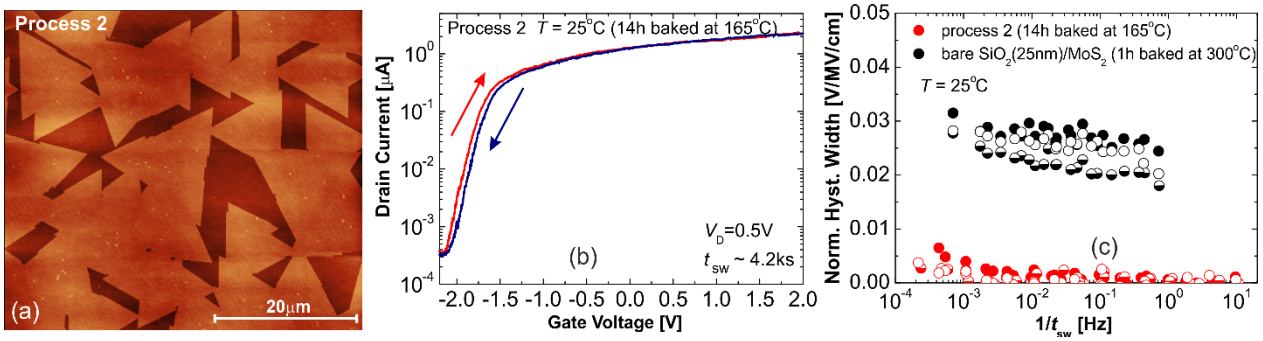

Fig.5. (a) AFM image of the Process 2 MoS_2 film. (b) Slow sweep hysteresis after baking at 165°C. $\Delta V_H(1/t_{sw})$ dependences for the Process 2 CaF_2/MoS_2 and bare channel SiO_2/MoS_2 FETs measured after baking (3 devices for each case).