Reliability of 2D Field-Effect Transistors: from First Prototypes to Scalable Devices

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***Abstract*—The rich and fascinating properties of two-dimensional (2D) materials have recently inspired various intriguing ideas for post-silicon nanoelectronics. One of the most far reaching of them is the possible substitution of Si with 2D materials in modern field-effect transistors (FETs). Ideally, this should suppress short-channel effects and thus extend Moore's law below 5 nm channel lengths, while maintaining and possibly even overcoming the high performance of commercial Si devices. However, despite recent progress at fabricating 2D FETs, there is still *no commercially competitive transistor technology*. One of the main reasons for this is the relatively poor reliability of typical 2D FET prototypes, which suffer from hysteresis and bias-temperature instabilities (BTI) of the transistor characteristics. Despite this, the attention paid to this serious problem is *impermissibly low*. Here we discuss the main achievements at understanding the reliability of various 2D FETs, from the first prototypes to recently reported scalable devices.**

I. Introduction

The recent discovery of the electric field effect in graphene [1] has unleashed a tremendous amount of research at creating atomically thin electronic devices using various two-dimensional (2D) materials [2]. Among all these studies, the most inspiring are those targeting the realization of field-effect transistors (FETs) with monolayer 2D channels [3]. This should allow to overcome short-channel effects and thus extend the life of Moore's law towards sub-5 nm channel dimensions. Recently, numerous prototype FETs built from graphene [4–6] and various beyond-graphene 2D semiconductors, such as MoS_2 [7–11], other transition metal dichalcogenides (TMDs, e.g. WSe_2 [12] and $MoTe_2$ [13]) and black phosphorus (BP) [14–16] have been reported. Furthermore, a considerable progress at addressing fabrication-related issues [17] and tuning electrical figures of merit (e.g. carrier mobility [11] and on/off current ratio [18, 19]) has been already achieved.

However, despite all the initial success and the enormous amount of funding invested into this field, there is still no commercial technology of 2D FETs. One of the main reasons for this is the comparably poor reliability of currently available 2D FETs. For instance, the hysteresis [7, 9, 16, 20] and bias-temperature instabilities (BTI) [5, 8, 16, 20, 21] of the gate transfer characteristics in these devices are typically much stronger than in Si technologies. Although commercialization of 2D devices prior to addressing these issues is impossible, we find that the attention paid in the literature to the reliability of 2D FETs is impermissibly low. As shown in Fig. 1, for the three most important 2D technologies, which are graphene, MoS_2 and BP FETs, the number of publications at least touching upon the reliability question is typically less than 10% of the total number of papers. As for the systematic studies of 2D FETs fully reserved to understanding their reliability, only a handful of papers for each technology have been published. As a result, the commercial potential of 2D FETs is currently debated by the research community [3], while the interest in these new technologies currently exhibits some signs of stagnation (Fig. 1). Nevertheless, we are confident that 2D FETs will have a huge commercialization potential if their reliability is considerable improved, for instance by using crystalline gate insulators with a low amount of defects [22].

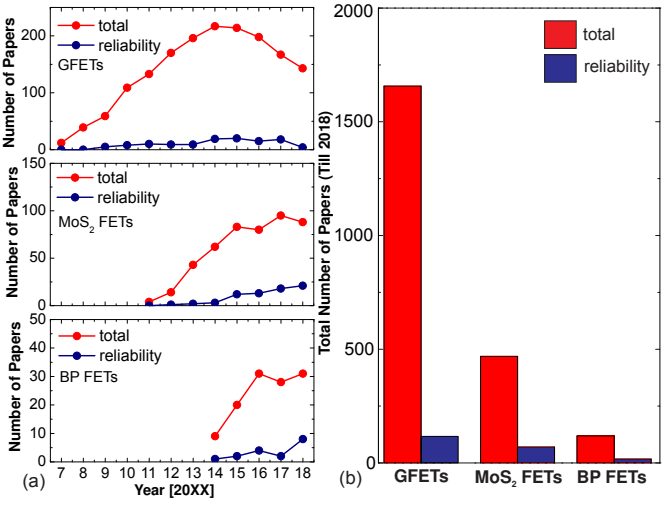

Fig. 1: (a) The number of papers per year on graphene, MoS_2 and BP transistors and the number of papers at least mentioning the reliability of these devices. (b) The total number of papers on these 2D technologies and their reliability (till 2018). The data are taken from Web of Science Core Collection.

Here we will discuss the recent progress at understanding the reliability of 2D FETs, starting from the first large-area prototypes and ending with more mature devices with scalable channel area and gate insulator thickness. By doing this, we will study the reliability of 2D FETs as an important benchmark of modern nanoscience.

II. Large-Area 2D FETs with Thick Insulators

Most of the currently available 2D FETs are large-area prototypes with several microns channel dimensions and tens of nanometers thick gate insulators. For example, we will discuss the reliability of graphene FETs (GFETs), MoS_2 FETs and black phosphorus FETs (BPFETs), which are currently the most frequently studied 2D FETs.

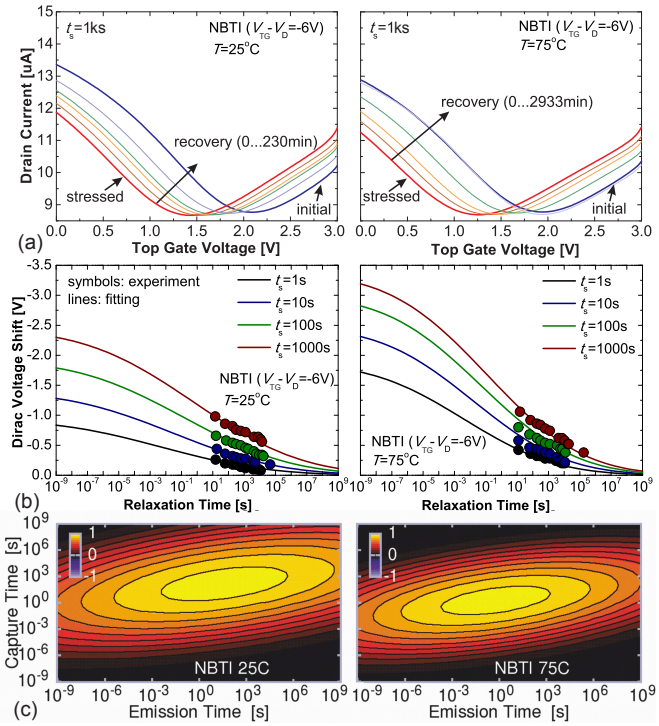

Fig. 2: (a) The top gate transfer characteristics of GFETs with 25 nm thick Al_2O_3 insulator [21] measured at different NBTI stress/recovery stages at two different temperatures. (b) Extracted $\Delta V_D(t_r)$ recovery traces fitted with the CET map model. (c) Underlying CET map distributions.

A. Graphene FETs

The first attempts at understanding the reliability of GFETs have been published in 2009, when the hysteresis of the gate transfer characteristics in GFETs with parylene and SiO_2 insulators was compared. It was observed that devices with parylene show a significant improvement in their reliability [23]. In the following studies the hysteresis [24–26] and BTI [5, 27, 28] in GFETs were typically attributed to carrier trapping by defects. However, owing to a lack of analysis using time-resolved measurement techniques and trustable physics-based models, no clear conclusions about the origin of these defects and the physical mechanisms underlying charge trapping have been made.

A better understanding of the reliability of GFETs was gained in our study on double-gated devices, where we examined BTI reliability of the top gate Al_2O_3 insulator [21]. There we measured BTI in GFETs using subsequent stress/recovery rounds with logarithmically increased stress times t_s, while doing full sweeps of the top gate transfer ($I_{DS} - V_{TG}$) characteristics at each stress/recovery stage (Fig. 2a). Thus, the BTI degradation/recovery dynamics can be expressed using the recovery of the Dirac point voltage shift (ΔV_D) versus the relaxation time (t_r) for different t_s. As shown in Fig. 2b, these recovery traces can be reasonably fitted using the capture-emission time (CET) map model previously developed for Si technologies [29]. In contrast to a very simplified stretched-exponential equation [30] used in most studies on 2D FETs, the CET map model provides a more physical description of the charge trapping processes. This model suggests that BTI is the collective response of independent oxide traps with widely distributed capture and emission times (Fig. 2c) which exchange charges with the channel following a first-order non-radiative multiphonon process. Thus, we concluded that BTI dynamics in GFETs are dominated by thermally activated oxide traps situated at a tunnel distance from the interface with the graphene channel. Furthermore, it has been found that under some conditions hot-carrier degradation (HCD) in GFETs is also strongly recoverable and can be nicely fitted using the CET map model [31]. This suggests that charge trapping by oxide traps also has a sizable contribution to HCD in GFETs.

However, we note that the zero bandgap of graphene makes accurate modeling of the reliability very challenging, since the technology computer aided design (TCAD) tools developed for Si MOSFETs cannot be reliably used for these devices. Furthermore, the hysteresis and BTI drifts in most of the previously reported GFETs are extremely large, which is mainly due to the huge amount of oxide defects in the insulators grown using non-optimized atomic-layer deposition (ALD) processes. Together with a very limited potential for digital applications of GFETs, this resulted in some decay of the research interest in these devices in recent years (Fig. 1a). Instead, the current trend in 2D research suggests switching to beyond graphene materials, such as MoS_2 and BP.

B. Black phosphorus FETs

Just like graphene, black phosphorus is an ambipolar semiconductor which is potentially interesting for both n- and p-FETs. An important advantage of this material over graphene is its sizable electronic bandgap which can exceed 1 eV in the single-layer limit. This makes BPFETs suitable for digital applications. However, initially the poor air-stability of BP made long-term reliability studies of BPFETs impossible. This problem was addressed by using conformal encapsulation schemes [15], which resulted in at least 17 months stability of BPFETs [16, 32].

Our studies of the hysteresis and BTI in highly-stable BPFETs with conformal Al_2O_3 encapsulation [16, 32] show that both issues are due to charge trapping by oxide defects in SiO_2 gate insulators. At room temperature the density of active defects contributing to charge trapping is relatively low [32]. However, thermal activation of more defects at higher temperatures results in sizable BTI drifts (Fig. 3a) and a huge hysteresis [16]. The recovery of the charge neutrality point shift ΔV_{NP} (Fig. 3b) can be well fitted using TCAD simulations considering that the defects in SiO_2 are energetically aligned within two distinct defect bands (Fig. 3c). Charge trapping is dominated by the upper defect band, which is energetically close to the conduction band of BP. Also, the positions of both defect bands are similar to those previously extracted for Si technologies [33–35]. This confirms that these defect bands are a fundamental property of an isulator and that the dynamics of BTI are similar in BPFETs and Si technologies.

While the dominant impact of insulator defects on the reliability of BPFETs has been demonstrated, typical BTI drifts are still orders of magnitude larger than in Si devices, especially at higher temperature. This suggests that the total

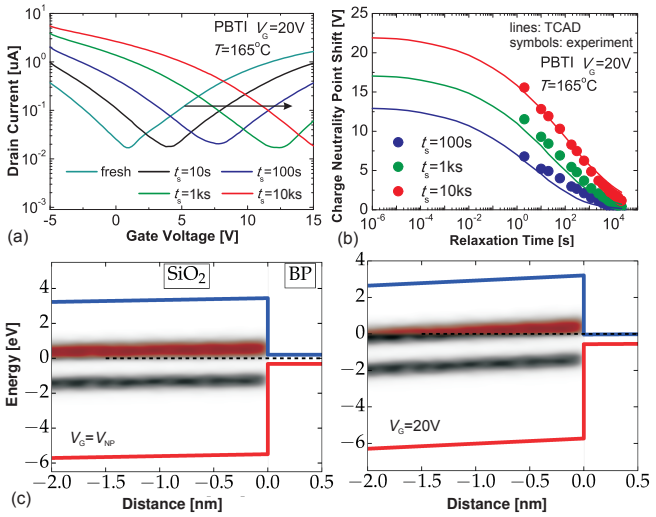

Fig. 3: (a) Evolution of the gate transfer characteristics of back-gated BPFETs with 80 nm thick SiO_2 insulator and Al_2O_3 encapsulation [16] after subsequent PBTI stresses at $T = 165°C$. (b) $\Delta V_{NP}(t_r)$ recovery traces fitted with TCAD. (c) Underlying band diagrams with the defect bands of SiO_2 for the case of equilibrium (left) and PBTI at $V_G = 20$ V (right).

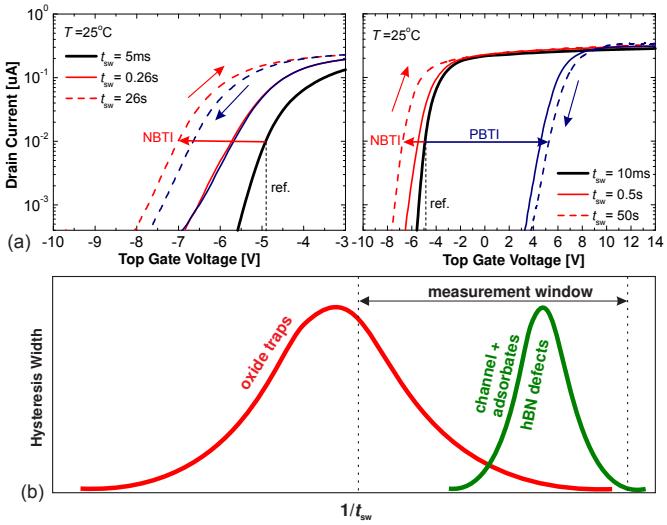

Fig. 4: (a) The top gate transfer characteristics of the MoS_2 FETs with 23 nm thick Al_2O_3 insulator [36]. For a narrow sweep range (left) the device is mostly under NBTI bias condition, and a small hysteresis is observed on the background of an NBTI shift which increases vs. t_{sw}. For a wider sweep range (right) the hysteresis is given as a superposition of NBTI and PBTI shifts, both increasing vs. t_{sw}. (b) Schematic $\Delta V_H(1/t_{sw})$ dependence. In experiments the maximum is typically observed if the hysteresis is dominated by fast defects rather than oxide traps.

density of defects inside the defect bands of thermally grown SiO_2, which is typically used in BPFETs and other 2D devices, is considerably larger than that in the SiO_2 films used in commercial Si technologies.

C. MoS_2 FETs

As of today, the most significant progress in fabrication of functional 2D FETs has been achieved with MoS_2, which is an air-stable 2D semiconductor with an electronic bandgap of up to 2.7 eV in the single-layer limit. However, the attention paid to the reliability of MoS_2 FETs is still low, and most studies were performed on bare channel back-gated devices of rather poor quality. Thus, the hysteresis and BTI in MoS_2 FETs are often attributed to the impact of adsorbates (e.g. water molecules), which agrees well with the activation of both issues in the ambient [7, 8]. At the same time, the adsorbates situated on top of the channel cannot have any contrubution to the hysteresis, since their occupancies are not able to follow the variations of the applied gate bias. Thus, the most likely mechanism appears to be the interaction between adsorbates which have diffused to the insulator/MoS_2 interface and the channel defects [10], such as S vacancies in MoS_2. This process is sensitive to the applied gate voltage, thus being able to contribute to the hysteresis and BTI.

However, the contribution coming from adsorbates can be reduced by placing bare channel devices into vacuum [7], not to mention more mature MoS_2 FETs with protected channels. In our recent studies [20, 36, 37] we have demonstrated that the most important mechanism of the hysteresis and BTI in MoS_2 FETs is charge trapping by insulator defects, similar to Si technologies and other 2D FETs. Furthermore, it could be demonstrated that the hysteresis arises from the gate bias dependence of the time constants of these defects [37] which results in a superposition of NBTI and PBTI drifts accumulated during forward and reverse sweeps (Fig. 4a) [36]. The magnitudes of these drifts depend on the total sweep time t_{sw} and V_G sweep range, which define the cumulative stress times at NBTI and PBTI bias conditions. Hence, the hysteresis and BTI are related phenomena which have the same origin and can be well described using the same defect bands (e.g. Fig. 3c). The energetic alignments of the defect bands are unique for each oxide and can be determined by fitting the measured hysteresis dynamics or BTI recovery with TCAD [35, 36].

We note that it is always important to consider that the hysteresis width ΔV_H depends on the sweep time t_{sw}. This aspect is often neglected in previous studies, which do not even mention the sweep rate used for the measurements. However, it has been demonstrated that the hysteresis dynamics can be well benchmarked using a range of $\Delta V_H(1/t_{sw})$ traces. According to our experimental observations and TCAD modeling [20], the dependence between ΔV_H and $1/t_{sw}$ has a universal shape with a maximum (Fig. 4b) which originates from different gate bias dependences of the capture and emission times. If the hysteresis is dominated by slow oxide defects with widely distributed time constants, this maximum is barely reachable when using reasonable sweep times. However, the maximum can be detected in bare channel devices if the key hysteresis mechanism is the interaction between adsorbates and channel defects [10], which is a comparably fast process. In that case the hysteresis can be suppressed by changing the measurement environment, since the number of both adsorbates and channel defects is sensitive to pressure and temperature. Also, the maximum can be sometimes visible in devices with hBN insulators [20], likely because hBN defects are faster than oxide traps. Although this behavior was for the first time observed in MoS_2 FETs, it is universal and expected to be similar for other 2D devices.

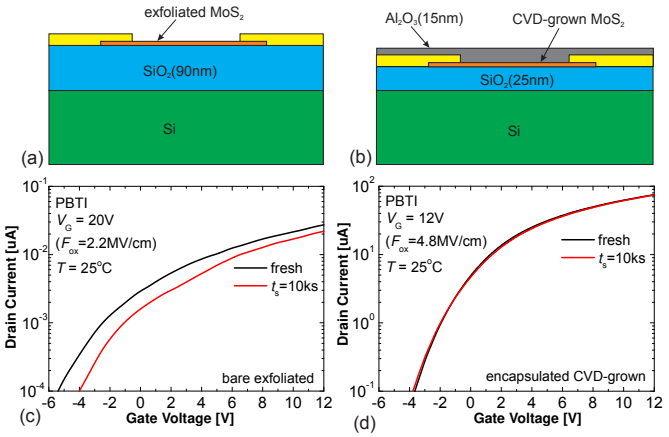

Fig. 5: Schematic cross-sections of bare exfoliated [20] (a) and encapsulated CVD-grown [38] (b) back-gated MoS_2 FETs. While bare exfoliated devices exhibit sizable PBTI drifts (c), in their encapsulated CVD-grown counterparts PBTI degradation is weak (d).

Understanding the origin of the hysteresis and BTI in MoS_2 FETs can be used to considerably suppress these issues. For now it is already known that the use of hBN insulators as an alternative to oxides leads to an improved reliability of MoS_2 FETs [20, 39]. This is because the density of electrically active defects in layered hBN is lower compared to amorphous oxides. However, in our recent work [38] we found that an improvement can be achieved even for MoS_2 FETs with SiO_2 insulators. For instance, a strong degradation observed in the first prototypes with bare exfoliated channels (Fig. 5a) was strongly reduced in more mature devices where the channels were grown by chemical vapour deposition (CVD) and protected with a high-quality Al_2O_3 encapsulation (Fig. 5b). The resulting improvement may be partially due to a higher quality of the thinner SiO_2 layer used in the latter case, which thus contained a lower number of defects. However, further improvement of the reliability would make sense mainly on scalable devices which are more close to the commercial requirements than prototypes with tens of nanometers thick insulators.

III. Scalable 2D FETs

Commercialization of 2D FETs requires scaling of the insulators down to the equivalent oxide thickness (EOT) of below 1 nm, which for most insulators corresponds to a physical thickness of several nanometers. Simultaneously, channel dimensions have to be scaled down to at least several tens of nanometers. So far only devices with either scaled insulator thickness or channel dimensions but not both have been reported. All these studies were performed on MoS_2 FETs. Below we will discuss the reliability aspects of these devices.

A. Devices with thin insulators

The oxides known from Si technologies, such as SiO_2 and Al_2O_3, are amorphous when grown in thin layers. Thus, their scaling down to sub-1 nm EOT while maintaining good interfaces with 2D materials is technologically difficult. On the other hand, hBN has a small bandgap of about 6 eV and a dielectric constant of about 5, which would lead to excessive gate leakage currents through the tunnel-thin hBN layers. While attempting to overcome these limitations, recently we reported bare channel back-gated MoS_2 FETs with crystalline CaF_2 as an insulator [22]. This material has a wide band gap of 12.1 eV, a high dielectric constant of 8.43 and a well-defined interface with 2D materials, which can be formed by the inert F-terminated $CaF_2(111)$ surface. The thickness of the epitaxially grown CaF_2 in our MoS_2 FETs was as low as 2 nm (EOT of about 0.9 nm), which has never been achieved for 2D FETs before.

We studied the hysteresis in CaF_2/MoS_2 FETs and found that this issue strongly depends on the quality of the MoS_2 channel grown by CVD. For the devices with small grain MoS_2 films having a large number of S vacancies we sometimes observed a maximum of $\Delta V_H(1/t_{sw})$ at moderate sweep times (Fig. 4b), indicating that an interaction between S vacancies and water adsorbates is the most likely mechanism of the hysteresis. However, for MoS_2 FETs with higher quality MoS_2 channels the hysteresis was even smaller than for Al_2O_3 encapsulated SiO_2(25 nm)/MoS_2 FETs (Fig. 6a) and close to Si/high-k FETs (Fig. 6b). Furthermore, the BTI drifts measured for our best devices with CaF_2 are the smallest ever reported for 2D FETs (Fig. 6c). The improved reliability of CaF_2/MoS_2 FETs is achieved due to a small number of electrically active defects in crystalline CaF_2 as compared to amorphous oxides. However, further improvement is necessary to achieve the level of commercial Si technologies. This requires a transition to more mature device configurations with protected channels and, finally, to top-gated devices which are suitable for circuit integration. A possible route for this is via the development of heteroepitaxy [40] of 2D materials on top of CaF_2 and CaF_2 on top of 2D materials and the production of CaF_2/2D/CaF_2 heterostructures.

Another important aspect for 2D FETs with tunnel-thin insulators is the comparably high insulator fields during device operation. For instance, the routinely achievable gate voltage of 2 V in MoS_2 FETs with 2 nm thick CaF_2 corresponds to an insulator field of 10 MV/cm, while 20 V in devices with 90 nm thick SiO_2 is only about 2.2 MV/cm. Thus, in devices with scalable insulators attention has to be paid to various breakdown issues, such as time-dependent dielectric breakdown (TDDB). Recent studies on multi-layer hBN films indicate a layer-by-layer breakdown of this insulator [41], though these experiments were not performed on complete transistors. Nevertheless, our recent experiments on CaF_2/MoS_2 FETs suggest that the breakdown mechanisms in CaF_2 are rather similar to hBN, though this requires a more detailed analysis.

B. Devices with small channel area

Fabrication of 2D FETs with sub-100 nm channel dimensions is still challenging. Thus, there are only few reliability studies on nanoscale MoS_2 FETs with thick SiO_2 insulators. In these devices there are only a few defects per channel, while the impact of each defect on the channel electrostatics is large. Charging and discharging of discrete defects leads to random shifts of V_{th} and, consequently, discrete fluctuations of the drain current measured versus time. This is known as

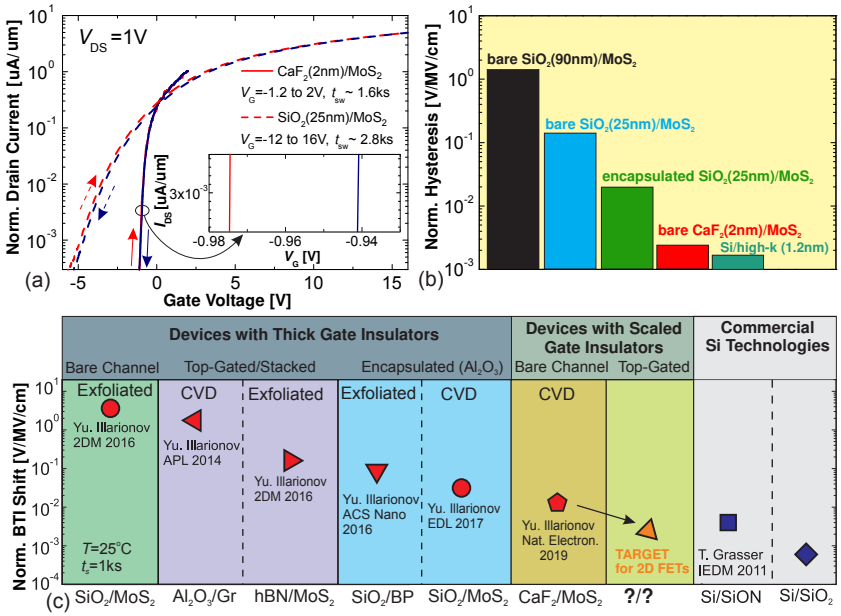

Fig. 6: (a) Ultra-slow sweep gate transfer characteristics measured for the Al_2O_3 encapsulated SiO_2(25 nm)/MoS_2 [38] and bare channel CaF_2(2 nm)/MoS_2 FETs [22]. The inset shows the hysteresis in the CaF_2(2 nm)/MoS_2 FETs near V_{th}. (b) Comparison of the hysteresis widths normalized by the insulator field factor $\Delta V_G/d_{ins}$, where ΔV_G is the gate voltage sweep range and d_{ins} is the insulator thickness. (c) Comparison of the BTI shifts normalized by the insulator field for devices from our previous studies [16, 20–22, 29, 38]. The best reliability is achieved for CaF_2(2 nm)/MoS_2 FETs, though some improvement is still required to achieve the level of commercial Si FETs.

random telegraph noise (RTN) which presents a very important reliability issue in nanoscale devices.

One recent study on nanoscale MoS_2 FETs [42] reports the presence of single-level, multi-level and correlated multi-level RTN, while suggesting a way to determine the positions of discrete defects along the channel. We performed similar RTN experiments on ∼50 nm sized bare channel MoS_2 FETs [43] and found that the origin of the defects can be understood from the measured RTN traces which contain information about the time constants. For instance, defects with a weak gate bias dependence of the capture and emission times are those situated on top of the channel. These can be adsorbates which are not able to follow the variations of V_G. On the other hand, defects with a strong bias dependence of the time constants can be identified as oxide traps in SiO_2. The energy levels of these defects and their depths in the insulator can be determined by fitting the measured results using TCAD [43]. Also, we found that some defects exhibit random periods of inactivity, which is known as anomalous RTN (aRTN) [44] or volatility [45].

However, in general the reliability of nanoscale 2D FETs is not well understood. In particular, a more detailed analysis of RTN is required. Also, a detailed analysis of the hysteresis and BTI recovery in nanoscale devices is required, as these issues are also expected to contain unique fingerprints of discrete defects. All these methods present a very powerful tool for microscopic characterization of the defect properties which cannot be performed on large-area devices.

IV. Conclusions

We have discussed the reliability of different 2D FETs, from the first prototypes to most recently reported devices with thin gate insulators and nanoscale channel dimensions. Independently of the device technology, reliability issues such as hysteresis, BTI and RTN in nanoscale devices, are mostly due to charge trapping by insulator defects which are energetically aligned within certain defect bands and have widely distributed time constants. The underlying physical processes can be well described using models known from Si technologies. At the same time, the reliability of 2D FETs can be strongly improved by using crystalline insulators, such as hBN and CaF_2, which contain less defects compared to amorphous oxides.

Despite the recent progress in understanding and addressing the reliability issues in 2D FETs, the overall amount of attention paid to this topic in the literature is rather low. Thus, we conclude by stating that the reliability of 2D FETs is an important roadblock of modern nanoscience which should get more attention from the research community.

Acknowlegements

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