Modeling the Effect of Random Dopants on Hot-Carrier Degradation in FinFETs

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Abstract—We present the first physics-based approach to modeling the effect of random dopants on hot-carrier degradation (HCD) in FinFETs, which is based on a statistical analysis of HCD performed over an ensemble of 200 transistors with different random dopant configurations. As a reference, the results obtained with the deterministic version of our HCD model are used. The statistical analysis shows that degradation traces and device lifetimes have quite broad distributions and that the deterministic model tends to overestimate HCD and makes pessimistic predictions on device lifetime. Moreover, lifetime distributions evaluated for high stress voltages and for biases close to the operating regimes have different shapes which makes backward lifetime extrapolation challenging, thereby demonstrating that full physics-based HCD treatment is of crucial importance.

Index Terms—hot-carrier degradation, stochastic modeling, random dopants, physics-based model, FinFET, interface traps.

I. INTRODUCTION

Hot-carrier degradation (HCD) is recognized as one of the most important and detrimental degradation modes together with bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), random telegraph noise (RTN), etc, that deteriorates performance of the field-effect transistor (FET) and hinders introduction of novel transistor nodes. With the rapid shrinking of device dimensions the detrimental effect of HCD becomes more pronounced. Recently HCD has been reported to be the main reliability issue in most advanced FinFET nodes fabricated by Intel [1,2]. This is because the very fast reduction of device dimensions is accompanied by a much slower (if any) scaling of the transistor operating (and hence stress) voltages. As a result, these miniaturized FETs are subjected to high electric fields which result in severe carrier heating, subsequently giving rise to HCD.

In addition to reliability problems, modern transistors can show quite broad sample-to-sample variability of their characteristics which also becomes an important issue. Such variability can be either of macroscopic nature (fluctuations in the dielectric thickness, continuous doping profiles, etc) [3–7] or stem from microscopic factors such as local perturbation of material properties (e.g. related to the amorphous nature of dielectric materials and hence corresponding dielectric/semiconductor interfaces) [8, 9], random dopants [10, 11],

etc. The latter aspect is especially pronounced in transistors with dimensions in the sub-decananometer range because these FETs contain just a handful of dopants which are randomly distributed over the device [11]. As a result, ultra-scaled transistors can have wide spreads of their parameters such as the drain current, threshold voltage, etc. This is the reason why the effect of random dopants on the characteristics of pristine devices was a subject of extensive research performed by several groups [6, 10, 12, 13].

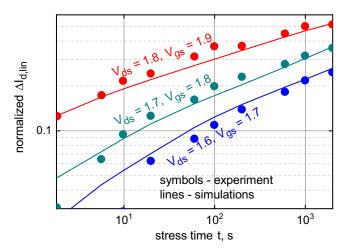


Fig. 1: Experimental and simulated with the deterministic version of our HCD model normalized changes of the linear drain current with time $\Delta I_{\rm d,lin}(t)$.

As we will demonstrate here, the situation becomes even more complicated when an analysis of degradation of short-channel devices is attempted. Indeed, degradation is related to the build-up of defects which proceeds in a stochastic manner, i.e. generated defects are also randomly distributed over the device, although following the macroscopic defect density, which can be used as a probability density for defect coordinates if one considers an extensive set of samples with different trap configurations. As a result, the reliability in modern FETs is considered as time dependent variability [14, 15]. This means that changes of device parameters during stress cannot be described by using a single degradation trace which results in a single device lifetime value. Instead, a set

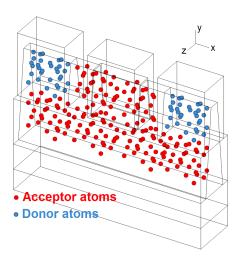


Fig. 2: A schematic representation of the FinFET with random dopants.

of degradation traces (each of them has a certain probability) should be considered, while the device life-time has to be described in terms of a probability density distribution. To summarize, comprehensive modeling of any of the reliability phenomena in nanoscale FETs should include a statistical analysis.

Such a statistical analysis has already been applied to the intimately related degradation issues BTI, RTN [16], and TDDB [17]. As for HCD, extensive experimental efforts focused on the statistical description of this effect were performed [18–22]. Moreover, some modeling approaches which study the impact of random positions of interface traps generated during HC stress have been recently published [23,24]. However, these approaches do not capture the effect of random dopants on HCD and perform simulations for a device with a fixed configuration.

The only paper which attempts to perform a comprehensive statistical description of HCD has recently been published by Bottini *et al.* [24]. This work presents an investigation of the impact of randomly distributed dopants and traps (created by hot-carrier stress) on the device characteristics. However, the bond-breakage process in this paper is described using phenomenological treatment of the defect generation kinetics. As a result, this approach does not consider the interplay between single- and multiple-carrier mechanisms of Si-H bond dissociation (see [25, 26]). An adjacent problem is that the effect of random dopants on carrier transport is also not addressed in [24]. We believe, however, that a physics-based description of these two aspects is of crucial importance for stochastic modeling of HCD.

Therefore, the goal of this work is to transform our deterministic HCD model [26, 27] (which can successfully represent HCD over a wide class of devices including planar FETs [27], FinFETs [28], and high-voltage transistors [29]) to a stochastic description of the effect of random dopants on HCD.

II. THE MODELING FRAMEWORK

Our deterministic model for HCD considers the single- and multiple-carrier (SC- and MC-) processes for Si-H bond breakage and all their superpositions [30,31]. Even at relatively low stress voltages, the single-carrier mechanism has been shown [26,32] to provide a significant contribution to the cumulative bond rupture rate. This is due to the coupling of these SC- and MC-mechanisms which has been recently reported to be the most probable path of bond dissociation [25,32–34]. Within this scenario, the bond is first being excited by several low-energetical carriers from the ground state to some intermediate level. The energy barrier which separates this level and the transport mode is reduced (compared to the bond-breakage energy from the ground state) and therefore the probability of a solitary carrier which can deliver this portion of energy and trigger an SC-mechanism is increased.

The rates of both mechanisms are calculated based on a thorough description of carrier transport [35]. To tackle this problem, we employ the deterministic Boltzmann transport equation solver ViennaSHE [35–38], which evaluates carrier energy distribution functions (DFs) at the Si/SiO₂ interface for given stress conditions and a specified device topology. To generate the device architecture we use the Sentaurus Process simulator [39] which is coupled to the device and circuit simulator MiniMOS-NT [40]. We perform calibration of these modeling tools in a manner to represent the current-voltage characteristics of the pristine device and ensure that the doping profiles (and other architectural features) are correctly captured. Note that this scheme creates a device with continuous doping profiles.

The distribution functions are then used to calculate the interface state generation rates for single- and multiple-carrier bond-breakage processes (and their superpositions) [30,31] and the interface state density $N_{\rm it}$. While calculating these quantities, we also consider the effect of the bond rupture

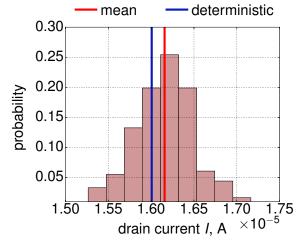


Fig. 3: The distribution of linear drain currents simulated for 200 different realizations of random dopant configurations. The linear drain current value for the parent device and the average linear drain current are also shown.

energy dispersion which can substantially affect the bond-breakage rates of both the mechanisms [26]. Note that these fluctuations of the dissociation energy stem from the structural disorder at the interface with an amorphous dielectric layer. In the model, this information is contained in the value of the standard deviation of the bond-breakage energy $\sigma_{\rm E}$ and this quantity is assumed to be fixed for all devices from the same technological node but varies if one switches from one technology to another. Together with the concentration of Si-H bonds in the pristine device N_0 (which is also determined by the technological process), $\sigma_{\rm E}$ is the main adjustable parameter of the model. The obtained $N_{\rm it}(x,y,z,t)$ profiles are then used as input for the device simulator MiniMOS-NT to calculate changes of the transistor characteristics over time.

The deterministic version of the model has already been validated for a wide class of transistors [26, 29]. However, in this paper we focus on the effect of random dopants on HCD in an n-channel FinFET with a gate length of $L_{\rm g} = 40\,{\rm nm}$ (the corresponding channel length is $L_{\rm ch} \sim 28\,{\rm nm}$) and the operating voltage of $V_{\rm dd}$ =0.9 V (the threshold voltage is $V_{\rm th} = 0.4\,{\rm V}$). The high-k gate stack contains an interfacial SiO₂ layer with a physical thickness of 0.4 nm and a 2.4 nm thick HfO₂ layer (the resulting equivalent oxide thickness is 1.2 nm). These devices were stressed for \sim 2 ks at room temperature under three different combinations of stress voltages $V_{\rm ds}$, $V_{\rm gs}$ ($V_{\rm ds}$ and $V_{\rm gs}$ are the drain and gate biases, respectively) corresponding to the worst-case conditions of HCD in short-channel devices [41]: $V_{\rm ds} = 1.6$, $V_{\rm gs} = 1.7$ V; $V_{
m ds}=1.7\,{
m V},\,V_{
m gs}=1.8\,{
m V};$ and $V_{
m ds}=1.8\,{
m V}$ and $V_{
m gs}=1.9\,{
m V}.$ To access hot-carrier degradation we recorded changes of the linear drain current (normalized to the drain current in the pristine device) $\Delta I_{\rm d,lin}$ as functions of stress time, see Fig. 1 and [28]. From Fig. 1 one can conclude that the model can represent degradation traces with good accuracy using a unique set of model parameters.

The device structure generated by the Sentaurus Process simulator was then used as a template to generate a set of 200 devices, where each of these devices is characterized by a unique distribution of random dopants (sketched in Fig. 2). The number of 200 samples was chosen to be a good trade-off between acquiring extensive statistics of various random dopant configurations and computational burden. Note that the transport simulator ViennaSHE requires substantial computational resources and therefore increasing the number of samples can dramatically increase computational time. To create transistors with different dopant configurations, for each mesh cell of the initial template device we multiplied the local concentration of doping impurities by the cell volume, thereby obtaining the number of discrete atoms in this cell. Then this number was a subject of randomization, i.e. for each cell a Poisson distributed (with the mean value determined by the macroscopic doping concentration) number of cell atoms was set. In these virtually generated samples, if the number of impurity atoms is transformed to a continuous concentration this quantity will be fluctuating from sample to sample. However, if one calculates the average over the device

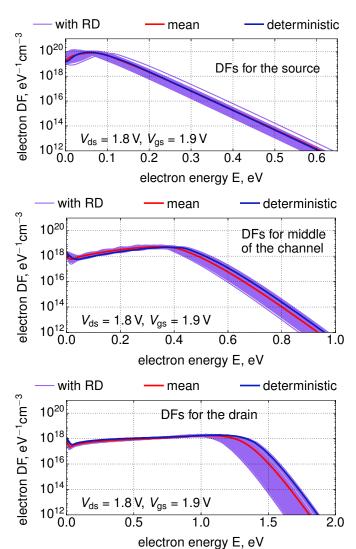


Fig. 4: Families of electron energy distribution functions calculated for $V_{\rm ds}=1.8\,\rm V$ and $V_{\rm gs}=1.9\,\rm V$ plotted for three sections in the device: in the source (upper panel), in the channel (middle panel), and in the drain (bottom panel). In addition, the DFs for the nominal device and the average DFs are shown.

ensemble, the resulting doping concentration will correspond to the concentration in the template device.

All further simulations (DFs, $N_{\rm it}$ profiles, $\Delta I_{\rm d,lin}(t)$ traces, and device lifetimes) are carried out using this ensemble of devices for two combinations of stress voltages of $V_{\rm ds}=1.7\,\rm V$, $V_{\rm gs}=1.8\,\rm V$, and $V_{\rm ds}=1.8\,\rm V$, $V_{\rm gs}=1.9\,\rm V$ and for biases which are quite close to the operating regime: $V_{\rm gs}=V_{\rm ds}=1.0\,\rm V$ ($V_{\rm dd}=0.9\,\rm V$). Note that for a reference we also calculated all these quantities for the original macroscopic device with non-fluctuating doping concentration. Since this device "integrates and averages" all doping profiles we label results obtained using this transistor as "deterministic".

III. RESULTS AND DISCUSSION

For each of the devices in the ensemble we calculated linear drain currents (at $V_{\rm ds}=0.05\,\rm V$ and $V_{\rm gs}=0.9\,\rm V$) and binned these values into a histogram presented in Fig. 3.

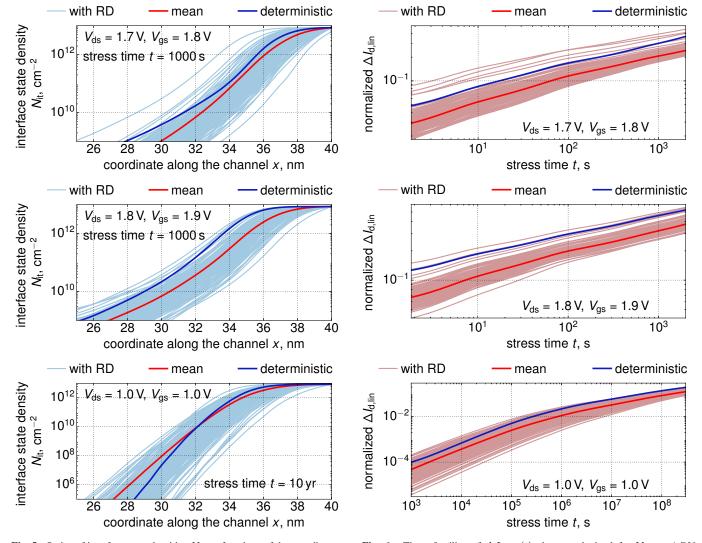


Fig. 5: Series of interface state densities $N_{\rm it}$ as functions of the coordinate x from the source to the drain plotted near the device drain (the cut is made close to the edge between the fin top and the sidewall) calculated for $V_{\rm ds}=1.7$ V, $V_{\rm gs}=1.8$ V; $V_{\rm ds}=1.8$ V, $V_{\rm gs}=1.9$ V; and $V_{\rm ds}=1.0$ V, $V_{\rm gs}=1.0$ V. For first two stress conditions stress time is t=1 ks, while for the latter one $t\sim10$ years. The $N_{\rm it}(x)$ profile obtained with the deterministic model and the average $N_{\rm it}(x)$ density are also depicted.

For comparison, we also show the $I_{\rm d,lin}$ value typical for the macroscopic device. From Fig. 3 one can see that the linear drain current probability density is close to a normal distribution with the mean value higher than the deterministic $I_{\rm d,lin}$ value.

Three series of electron DFs evaluated at $V_{\rm ds}=1.8\,{\rm V}$ and $V_{\rm gs}=1.9\,{\rm V}$ for the source, channel, and drain are shown in Fig. 4. One can see that each set of DFs is very broad and typically the deterministic DFs have higher values in the mid-high energy range, as compared to the mean DFs. This trend is especially pronounced in the drain section of the device (Fig. 4, bottom panel) where the $N_{\rm it}$ density has a peak which makes the most prominent contribution to HCD. In other words, based on the behavior of electron DFs, we expect that the deterministic version of the model should result in substantially stronger HCD than the average degradation

Fig. 6: Three families of $\Delta I_{\rm d,lin}(t)$ changes obtained for $V_{\rm ds}=1.7\,\rm V,$ $V_{\rm gs}=1.8\,\rm V;$ $V_{\rm ds}=1.8\,\rm V,$ $V_{\rm gs}=1.9\,\rm V;$ and $V_{\rm ds}=1.0\,\rm V,$ $V_{\rm gs}=1.0\,\rm V.$ Deterministic and average $\Delta I_{\rm d,lin}(t)$ traces are also plotted.

typical for the entire set of the devices.

The interface state density profiles $N_{\rm it}(x)$ (where x is the coordinate from the source to the drain; $x=40\,{\rm nm}$ corresponds to the drain and thus for the sake of visibility only the drain $N_{\rm it}$ peak is resolved) evaluated for three stress voltages and summarized in Fig. 5 confirm this idea. Thus, for all stress conditions the deterministic $N_{\rm it}$ values are much higher than the mean. Note that for $V_{\rm gs}=V_{\rm ds}=1.0\,{\rm V}$ the deterministic $N_{\rm it}$ values can be lower than the mean values but this trend is pronounced only for $N_{\rm it}\lesssim 10^{10}\,{\rm cm}^{-2}$ and such low $N_{\rm it}$ concentrations do not affect device performance.

Fig. 6 presents three series of normalized $\Delta I_{\rm d,lin}(t)$ traces which have substantially broad distributions. The trend that the deterministic model overestimates HCD is also visible in this figure. Using the changes of the linear drain currents we extracted lifetimes for each realization of the devices (determined as time at which $\Delta I_{\rm d,lin}=0.1$) and binned these

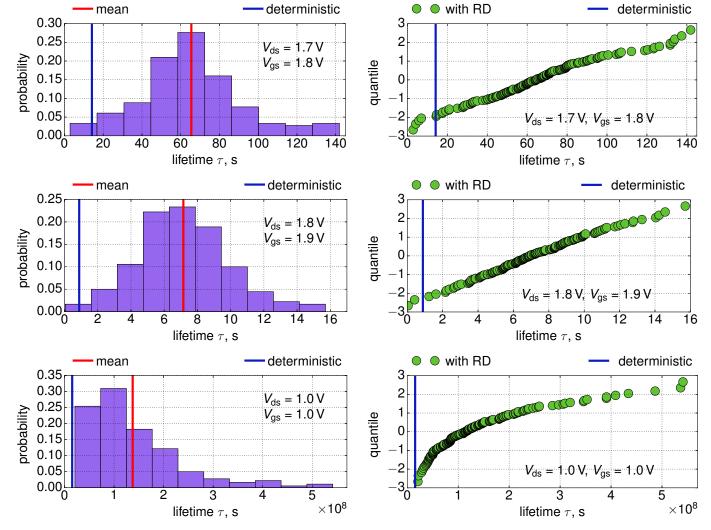


Fig. 7: Distributions of device lifetime extracted from $\Delta I_{\rm d,lin}(t)$ traces (Fig. 6) for $V_{\rm ds}=1.7$ V, $V_{\rm gs}=1.8$ V; $V_{\rm ds}=1.8$ V, $V_{\rm gs}=1.9$ V; and $V_{\rm ds}=1.0$ V, $V_{\rm gs}=1.0$ V. The deterministic and average lifetimes are also marked.

Fig. 8: Probit plots for device lifetimes under three stress conditions: $V_{\rm ds}=1.7\,\rm V,\ V_{\rm gs}=1.8\,\rm V;\ V_{\rm ds}=1.8\,\rm V,\ V_{\rm gs}=1.9\,\rm V;$ and $V_{\rm ds}=1.0\,\rm V,\ V_{\rm gs}=1.0\,\rm V.$ One can see that for higher stress voltages ($V_{\rm ds}=1.7\,\rm V$ and $V_{\rm ds}=1.8\,\rm V$) lifetime distributions are very close to the normal ones.

values into histograms. At a first glance, lifetime probability densities obtained for $V_{\rm ds}=1.7\,\rm V$, $V_{\rm gs}=1.8\,\rm V$, and $V_{\rm ds}=1.8\,\rm V$, $V_{\rm gs}=1.9\,\rm V$ are nearly normally distributed, while for stress conditions close to the operating regime the distributions are asymmetric. To check this in greater detail probit plots for the cumulative distribution functions for device lifetimes are employed (see Fig. 8). They confirm that the device lifetime for higher stress voltages can be described by a normal distribution, while at $V_{\rm gs}=V_{\rm ds}=1.0\,\rm V$ the probability density is clearly non-normal. Finally, we can see (Fig. 6) that for all stress regimes the deterministic lifetime is shorter than the mean.

One of our main results, namely that HCD in the device with the non-fluctuating doping concentration substantially differs from the average HCD, is consistent with findings by Asenov *et al.* for *pristine transistors* [42,43]. The authors of [42,43] showed that the drain current, threshold voltage, and

the mobility calculated for the deterministic version of the device significantly deviate from their mean/average values obtained for the ensemble of FETs. This behavior is due to a strong distortion of the channel potential by individual doping atoms which can dramatically perturb carrier transport and depopulate the high-energy fraction of the ensemble, thereby strongly affecting the carrier distribution functions (Fig. 4), interface state density profiles (Fig. 5), $\Delta I_{\rm d,lin}(t)$ degradation traces (Fig. 6), and device life-times (Figs. 7,8).

An important consequence from these trends is that an HCD model calibrated using a doping profile calculated e.g. with a process simulator will result in HCD stronger than that evaluated by averaging contributions given by all devices in the set. All these considerations mean that for a comprehensive HCD analysis one should perform a complete statistical treatment of the effect of random dopants.

IV. CONCLUSION

For the first time we have performed statistical modeling of the effect of random dopants on hot-carrier degradation. To achieve this goal, we used an ensemble of 200 FinFETs with different configurations of random dopants and calculated carrier energy distribution functions, interface state density profiles, linear drain current degradation traces, and lifetimes for each of these devices as well as for the device with the average doping profile (referred to as "deterministic"). We found that in all cases HCD (and related quantities) is overestimated if treated with the deterministic version of the model. In addition, device lifetimes have rather broad distributions. For higher stress voltages, their probability densities are nearly normally distributed, while for the regime similar to the operating conditions the lifetime distribution substantially deviates from the Gaussian. Therefore, full statistical treatment should be carried out to describe HCD in sufficient detail. Finally, we conclude that one cannot easily extrapolate back from accelerated stress to operating conditions because lifetime distributions in these regimes have substantially different shapes.

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REFERENCES

- [1] S. Novak, C. Parker, D. Becher, M. Liu, M. Agostinelli, M. Chahal, P. Packan, P. Nayak, S. Ramey, and S. Natarajan, "Transistor Aging and Reliability in 14nm Tri-gate Technology," in 2015 IEEE International Reliability Physics Symposium, April 2015, pp. 2F.2.1–2F.2.5.
- [2] A. Rahman, J. Dacuna, P. Nayak, G. Leatherman, and S. Ramey, "Reliability Studies of a 10nm High-performance and Low-power CMOS Technology Featuring 3rd Generation FinFET and 5th Generation HK/MG," in 2018 IEEE International Reliability Physics Symposium (IRPS), March 2018, pp. 6F.4–1–6F.4–6.
- [3] M. Koh, K. Iwamoto, W. Mizubayashi, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Yokoyama, S. Miyazaki, M. M. Miura, and M. Hirose, "Threshold Voltage Fluctuation Induced by Direct Tunnel Leakage Current through 1.2-2.8 nm Thick Gate Oxides for Scaled MOSFETs," in 1998 International Electron Devices Meeting, Dec 1998, pp. 919–922.
- [4] M. Koh, W. Mizubayashi, K. Iwamoto, H. Murakami, T. Ono, M. Tsuno, T. Mihara, K. Shibahara, S. Miyazaki, and M. Hirose, "Limit of Gate Oxide Thickness Scaling in MOSFETs due to Apparent Threshold Voltage Fluctuation Induced by Tunnel Leakage Current," *IEEE Transactions on Electron Devices*, vol. 48, no. 2, pp. 259–264, Feb 2001.
- [5] P. Andrei, "Analysis of Fluctuations in Semiconductor Devices," *PhD Thesis*, pp. i–180, 2004.
- [6] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic Threshold Voltage fluctuations in Decanano MOSFETs due to Local Oxide Thickness Variations," *IEEE Transactions on Electron Devices*, vol. 49, no. 1, pp. 112–119, Jan 2002.
- [7] S. Tyaginov, M. Vexler, A. Shulekin, and I. Grekhov, "Statistical Analysis of Tunnel Currents in Scaled MOS Structures with a Nonuniform Oxide Thickness Distribution," *Solid-State Electronics*, vol. 49, no. 7, pp. 1192–1197, 2005.
- [8] A. R. Brown, J. R. Watling, A. Asenov, G. Bersuker, and P. Zeitzoff, "Intrinsic Parameter Fluctuations in MOSFETs due to Structural Nonuniformity of High-κ Gate Stack Materials," in 2005 International Conference On Simulation of Semiconductor Processes and Devices, Sep. 2005, pp. 27–30.

- [9] A. R. Brown, J. R. Watling, and A. Asenov, "Intrinsic Parameter Fluctuations due to Random Grain Orientations in High-κ Gate Stacks," *Journal of Computational Electronics*, vol. 5, no. 4, pp. 333–336, Dec 2006.
- [10] D. J. Frank, Y. Taur, M. Ieong, and H.-P. Wong, "Monte Carlo Modeling of Threshold Variation due to Dopant Fluctuations," in 1999 Symposium on VLSI Circuits. Digest of Papers (IEEE Cat. No.99CH36326), June 1999, pp. 171–172.
- [11] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the Random Dopant Induced Threshold Fluctuations and Lowering in sub-100 nm MOSFETs due to Quantum Effects: a 3-D Density-gradient Simulation Study," *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 722–729, Apr 2001.
- [12] A. Asenov, "Random Dopant Induced Threshold Voltage Lowering and Fluctuations in sub-0.1 μm MOSFET's: A 3-D Atomistic Simulation Study," *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp. 2505–2513, Dec 1998.
- [13] Y. Li, S. Yu, J. Hwang, and F. Yang, "Discrete Dopant Fluctuations in 20-nm/15-nm-Gate Planar CMOS," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1449–1455, June 2008.
- [14] B. Kaczer, T. Grasser, P. J. Roussel, J. Franco, R. Degraeve, L. A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, "Origin of NBTI Variability in Deeply Scaled pFETs," in 2010 IEEE International Reliability Physics Symposium, May 2010, pp. 26–32.
- [15] B. Kaczer, J. Franco, P. Weckx, P. Roussel, V. Putcha, E. Bury, M. Simicic, A. Chasin, D. Linten, B. Parvais, F. Catthoor, G. Rzepa, M. Waltl, and T. Grasser, "A Brief Overview of Gate Oxide Defect Properties and Their Relation to MOSFET Instabilities and Device and Circuit Time-dependent Variability," *Microelectronics Reliability*, vol. 81, pp. 186–194, 2018.
- [16] T. Grasser, "Stochastic Charge Trapping in Oxides: From Random Telegraph Noise to Bias Temperature Instabilities," *Microelectronics Reliability (invited)*, vol. 52, no. 1, pp. 39–70, 2012.
- [17] A. Padovani, D. Z. Gao, A. L. Shluger, and L. Larcher, "A Microscopic Mechanism of Dielectric Breakdown in SiO₂ Films: An Insight from Multi-scale Modeling," *Journal of Applied Physics*, vol. 121, no. 15, p. 155101, 2017.
- [18] C. H. Tu, S. Y. Chen, A. E. Chuang, H. S. Huang, Z. W. Jhou, C. J. Chang, S. Chou, and J. Ko, "Transistor Variability after CHC and NBTI Stress in 90 nm pMOSFET Technology," *Electronics Letters*, vol. 45, no. 16, pp. 854–856, July 2009.
- [19] E. R. Hsieh, S. S. Chung, C. H. Tsai, R. M. Huang, C. T. Tsai, and C. W. Liang, "New Observations on the Physical Mechanism of Vthvariation in Nanoscale CMOS Devices after Long Term Stress," in 2011 International Reliability Physics Symposium, April 2011, pp. XT.9.1– XT.9.2.
- [20] P. Magnone, F. Crupi, N. Wils, H. P. Tuinhout, and C. Fiegna, "Characterization and Modeling of Hot Carrier-Induced Variability in Subthreshold Region," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2093–2099, Aug 2012.
- [21] S. S. Chung, "The Process and Stress-induced Variability Issues of Trigate CMOS Devices," in 2013 IEEE International Conference of Electron Devices and Solid-state Circuits, June 2013, pp. 1–2.
- [22] B. Kaczer, J. Franco, M. Cho, T. Grasser, P. J. Roussel, S. Tyaginov, M. Bina, Y. Wimmer, L. M. Procel, L. Trojman, F. Crupi, G. Pitner, V. Putcha, P. Weckx, E. Bury, Z. Ji, A. D. Keersgieter, T. Chiarella, N. Horiguchi, G. Groeseneken, and A. Thean, "Origins and Implications of Increased Channel hot Carrier Variability in nFinFETs," in 2015 IEEE International Reliability Physics Symposium, April 2015, pp. 3B.5.1–3B.5.6.
- [23] C. Liu, K. T. Lee, S. Pae, and J. Park, "New Observations on Hot Carrier Induced Dynamic Variation in Nano-scaled SiON/poly, HK/MG and FinFET Devices Based on On-the-fly HCI Technique: The Role of Single Trap Induced Degradation," in 2014 IEEE International Electron Devices Meeting, Dec 2014, pp. 34.6.1–34.6.4.
- [24] R. Bottini, A. Ghetti, S. Vigano, M. G. Valentini, P. Murali, and C. Mouli, "Non-Poissonian Behavior of Hot Carrier Degradation Induced Variability in MOSFETs," in 2018 IEEE International Reliability Physics Symposium (IRPS), March 2018, pp. 6E.7–1–6E.7–6.
- [25] Y. Randriamihaja, V. Huard, X. Federspiel, A. Zaka, P. Palestri, D. Rideau, and A. Bravaix, "Microscopic Scale Characterization and Modeling of Transistor Degradation Under HC Stress," *Microelectronics Reliability*, vol. 52, no. 11, pp. 2513–2520, 2012.

- [26] M. Bina, S. Tyaginov, J. Franco, Y. Wimmer, D. Osinstev, B. Kaczer, T. Grasser et al., "Predictive Hot-Carrier Modeling of n-channel MOS-FETs," *IEEE Transactions on Electron Devices*, vol. 61, no. 9, pp. 3103– 3110, 2014.
- [27] S. Tyaginov, M. Jech, J. Franco, P. Sharma, B. Kaczer, and T. Grasser, "Understanding and Modeling the Temperature Behavior of Hot-Carrier Degradation in SiON nMOSFETs," *IEEE Electron Device Letters*, vol. 37, no. 1, pp. 84–87, Jan 2016.
- [28] A. Makarov, S. E. Tyaginov, B. Kaczer, M. Jech, A. Chasin, A. Grill, G. Hellings, M. Vexler, D. Linten, and T. Grasser, "Hot-Carrier Degradation in FinFETs: Modeling, Peculiarities, and Impact of Device Topology," in *Proc. International Electron Devices Meeting (IEDM)*, 2017, pp. 13.1.1–13.1.4.
- [29] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.-M. Park, R. Minixhofer, H. Ceric, and T. Grasser, "Modeling of Hot-Carrier Degradation in nLDMOS Devices: Different Approaches to the Solution of the Boltzmann Transport Equation," *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1811–1818, 2015.
- [30] W. McMahon, K. Matsuda, J. Lee, K. Hess, and J. Lyding, "The Effects of a Multiple Carrier Model of Interface States Generation of Lifetime Extraction for MOSFETs," in *Proc. International Conference* on Modeling and Simulation of Microsystem, vol. 1, 2002, pp. 576–579.
- [31] A. Bravaix, C. Guerin, V. Huard, D. Roy, J. Roux, and E. Vincent, "Hot-carrier Acceleration Factors for Low Power Management in DC-AC Stressed 40nm NMOS Node at High Temperature," in *Proc. International Reliability Physics Symposium (IRPS)*, 2009, pp. 531–546.
- [32] S. Tyaginov, M. Bina, J. Franco, D. Osintsev, O. Triebl, B. Kaczer, and T. Grasser, "Physical Modeling of Hot-Carrier Degradation for Short- and Long-Channel MOSFETs," in *Proc. International Reliability Physics Symposium (IRPS)*, 2014, pp. XT.16–1–16–8.
- [33] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, D. Osintsev, B. Kaczer, and T. Grasser, "A Predictive Physical Model for Hot-Carrier Degradation in Ultra-Scaled MOSFETs," in *Proc. Simulation of Semiconductor Processes and Devices (SISPAD)*, 2014, pp. 89–92.
- [34] Y. Randriamihaja, X. Federspiel, V. Huard, A. Bravaix, and P. Palestri,

- "New Hot Carrier Degradation Modeling Reconsidering the Role of EES in Ultra Short n-channel MOSFETs," in *Proc. International Reliability Physics Symposium (IRPS)*, 2013, pp. 1–5.
- [35] M. Bina, K. Rupp, S. Tyaginov, O. Triebl, and T. Grasser, "Modeling of Hot Carrier Degradation Using a Spherical Harmonics Expansion of the Bipolar Boltzmann Transport Equation," in *Proc. International Electron Devices Meeting (IEDM)*, 2012, pp. 713–716.
- [36] http://viennashe.sourceforge.net/, 2014.
- [37] K. Rupp, T. Grasser, and A. Jüngel, "On the Feasibility of Spherical Harmonics Expansions of the Boltzmann Transport Equation for Three-Dimensional Device Geometries," in 2011 International Electron Devices Meeting, Dec 2011, pp. 34.1.1–34.1.4.
- [38] K. Rupp, C. Jungemann, M. Bina, A. Jüngel, and T. Grasser, "Bipolar Spherical Harmonics Expansions of the Boltzmann Transport Equation," in *Proc. International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2012, pp. 19–22.
- [39] Synopsis, Sentaurus Process, Advanced Simulator for Process Technologies.
- [40] T. B. Stockinger, K. Dragosits, T. Grasser, R. Klima, M. Knaipp, H. Kosina, R. Mlekus, V. Palankovski, M. Rottinger, G. Schrom, S. Selberherr, and M., MINIMOS-NT User's Guide, Institut für Mikroelektronik, 1998.
- [41] S. Tyaginov and T. Grasser, "Modeling of Hot-Carrier Degradation: Physics and Controversial Issues," in *Proc. International Integrated Reliability Workshop (IIRW)*, 2012, pp. 206–215.
- [42] A. Asenov, R. Balasubramaniam, A. R. Brown, J. H. Davies, and S. Saini, "Random Telegraph Signal Amplitudes in sub 100 nm (Decanano) MOSFETs: a 3D 'Atomistic' Simulation Study," in *Interna*tional Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138), Dec 2000, pp. 279–282.
- [43] A. Asenov, F. Adamu-Lema, X. Wang, and S. M. Amoroso, "Problems With the Continuous Doping TCAD Simulations of Decananometer CMOS Transistors," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2745–2751, Aug 2014.