On Correlation Between Hot-Carrier Stress Induced Device Parameter Degradation and Time-Zero Variability

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***Abstract*—We investigate correlation between linear drain currents ($I_{\mathrm{d,lin}}$) in unstressed n-channel FinFETs and relative $I_{\mathrm{d,lin}}$ changes ($\Delta I_{\mathrm{d,lin}}$) during hot-carrier degradation (HCD). For this analysis we simulate 200 different realizations of a FinFET where each of these devices has its own unique distribution of random dopants. Our study shows that devices with superior performance (with higher time-zero $I_{\mathrm{d,lin}}$ values) degrade faster than initially "worse" transistors (with lower initial $I_{\mathrm{d,lin}}$ currents) and, correspondingly, device lifetime also decreases with the time-zero $I_{\mathrm{d,lin}}$.**

***Index Terms*—Hot-carrier degradation, random dopants, variability, physical modeling, FinFETs, carrier transport, interface traps**

I. Introduction

In scaled field-effect transistors (FETs) the problem of device reliability has recently been reformulated in terms of time-dependent variability of device characteristics, as opposed to the deterministic picture typical for large-area transistors [1]. This paradigm shift is related to the stochastic nature of defect generation where a charged defect can be randomly placed in a device. Such a defect can impact transistor characteristics in different manners, depending on its position. Moreover, even pristine nanoscale FETs are not microscopically identical and sample-to-sample variability of transistor parameters at time-zero can be broad [2]. One can envisage that samples with superior properties degrade with a different rate compared to FETs of a poor quality.

Among these lines, Kerber and Nigam [3] showed experimental evidence that the threshold voltage values (V_{th}) in "virgin" FETs and their shifts ΔV_{th} during bias temperature instability (BTI) stress are correlated. In other words, transistors with better characteristics degrade faster and therefore have worse lifetimes as compared to initially "bad" devices. Quite to contrary, Hussin *et al.* [4] reported that $\{V_{\mathrm{th}}, \Delta V_{\mathrm{th}}\}$ pairs are uncorrelated. The same tendency was shown by Angot *et al.* [5]. In addition, variability induced by self-heating was studied by the group of Asenov [6]; the authors showed that self-heating reduces the ON-current fluctuations.

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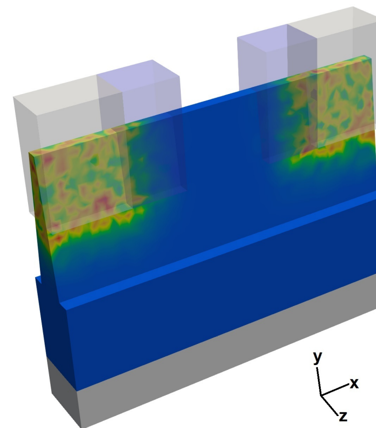

Fig. 1. A schematic representation of the FinFET with random dopants.

Finally, Gerrer and co-authors [7] discussed an increase in the defect generation rate in the vicinity of the percolation path and this behavior was attributed to a higher current density in the percolation path. Therefore, we conclude that there is correlation between time-zero and time-dependent variabilities of device characteristics during stress.

As for hot-carrier degradation (HCD) – which is reported to be the most detrimental reliability issue in modern MOSFETs [8] – Schlünder *et al.* [9] showed a strong correlation between

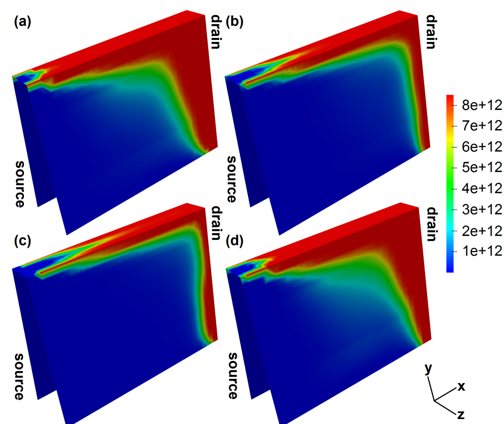

Fig. 2. N_{it} densities shown for four different realizations of RD configurations corresponding to the same continuous doping profile. Calculations were performed for $V_{\mathrm{ds}} = 1.8\,\mathrm{V}$, $V_{\mathrm{gs}} = 1.9\,\mathrm{V}$ and $t = 200\,\mathrm{s}$. The concentrations N_{it} can be substantially different in devices with different RD configurations.

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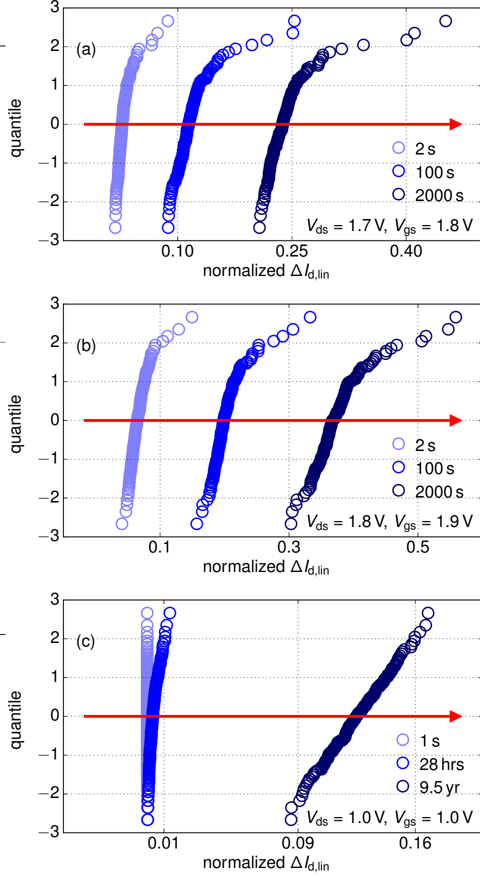

Fig. 3. Distributions of the normalized linear drain current change as probit plots calculated for three different combinations of $V_{\rm gs}$ and $V_{\rm ds}$. One can see that the distributions become wider at longer stress times.

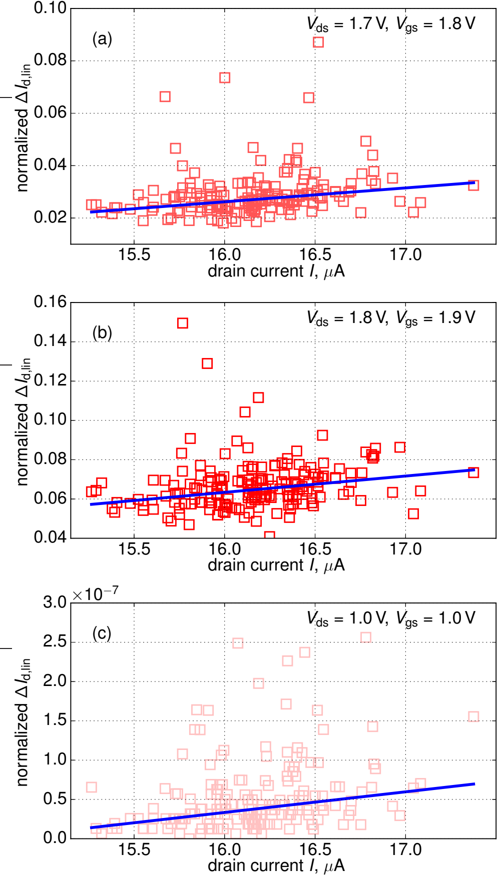

Fig. 4. Normalized changes in the linear drain current $\Delta I_{\rm d,lin}$ plotted against time-zero values of the drain current $I_{\rm d,lin}^{(0)}$. The linear fit obtained with the robust correlation test shows that the median $\Delta I_{\rm d,lin}$ increases with $I_{\rm d,lin}^{(0)}$. Data are shown at t = 2 s for $V_{\rm ds}$ = 1.7 V, $V_{\rm gs}$ = 1.8 V and $V_{\rm ds}$ = 1.8 V, $V_{\rm gs}$ = 1.9 V and at t = 1 s for $V_{\rm ds}$ = $V_{\rm gs}$ = 1.0 V.

parameters in virgin devices and changes of these parameters. These authors have also shown that devices with initially higher drain current degrade faster than worse transistors with lower currents. However, to the best of our knowledge, no simulation studies of this correlation have been performed so far.

Thus, the goal of this work is to investigate correlation between time-zero values ($I_{\rm d,lin}^{(0)}$) of the linear drain current ($I_{\rm d,lin}$) in n-channel FinFETs and relative changes of these currents ($\Delta I_{\rm d,lin}$) during hot-carrier stress and, further, HCD device lifetimes. For this, we use our recently developed stochastic model for HCD [10, 11].

II. The Modeling Framework

The framework for a stochastic description of HCD has been derived from the deterministic approach to hot-carrier degradation modeling [12–14], which was shown to represent HCD over a wide class of devices which includes high-voltage FETs (such as LDMOS transistors) [15], scaled planar FETs [13, 16] and ultra-scaled FETs of 3D architectures, i.e. FinFETs [17] and NWFETs [18]. Within this approach, HCD is considered to be driven by dissociation of Si-H bonds at the $\rm Si/SiO_2$ interface which can be triggered by the single- and multiple-carrier mechanisms of Si-H bond rupture, as well as by their superpositions. As suggested in our previous publications [13, 16], as well as by Randriamihaja *et al.* [19, 20], the most probable pathway of the Si-H bond dissociation reaction is related to preexcitation of the bond by several cold carriers followed by a hot carrier bombardment which breaks the bond. To compute the rates of these processes, we use the carrier energy distribution functions which are obtained from a solution of the Boltzmann transport equation with the deterministic transport simulator ViennaSHE [21]. For obtaining the device architecture the Sentaurus Process simulator [22] is employed. Note that Sentaurus Process generates device structures with continuous doping profiles. Since the Si/dielectric interface is a disordered system, the bond-breakage energy is a stochastically distributed quantity and our HCD model assumes that this energy follows the normal distribution.

Our statistical analysis considers the impact of random dopants (RDs) on HCD and was conducted using experimental data measured employing n-channel FinFETs (which are schematically depicted in Fig. 1). These devices have a

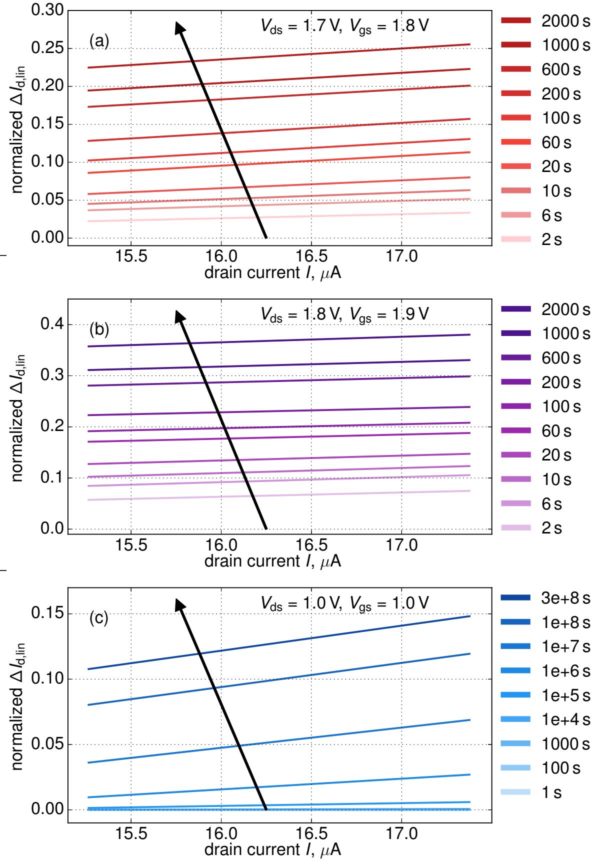

Fig. 5. Linear fits of $\Delta I_{\rm d,lin}$ vs. $I^{(0)}_{\rm d,lin}$ for all stress time steps extracted from the simulated data using the robust correlation test.

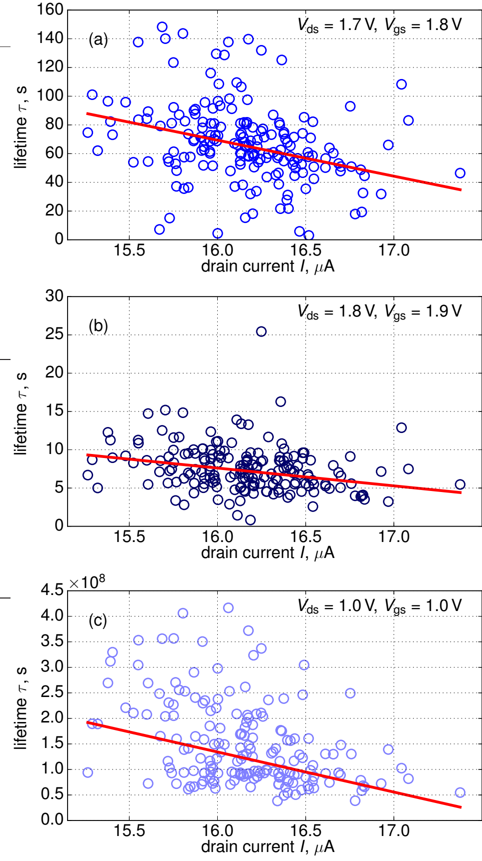

Fig. 6. Dependencies of device lifetime on the time-zero linear drain current $I^{(0)}_{\rm d,lin}$ extracted from statistical data. One can see that devices with higher $I^{(0)}_{\rm d,lin}$ degrade faster, i.e. the corresponding lifetimes are shorter.

gate length of $L_{\rm g}$ = 40 nm, an operating voltage of $V_{\rm dd}$ = 0.9 V and a high-k gate stack composed from SiO_2 and HfO_2 layers with a resulting equivalent oxide thickness of ~ 1.2 nm. These devices were stressed at three different combinations of source-gate ($V_{\rm gs}$) and source-drain ($V_{\rm ds}$) voltages: $V_{\rm ds}$ = 1.6 V, $V_{\rm gs}$ = 1.7 V; $V_{\rm ds}$ = 1.7 V, $V_{\rm gs}$ = 1.8 V; and $V_{\rm ds}$ = 1.8 V, $V_{\rm gs}$ = 1.9 V. HC stress was performed at room temperature for $\sim$ 2 ks. All these combinations correspond to $V_{\rm gs} \sim V_{\rm ds}$, i.e. to the worst-case conditions of hot-carrier degradation in short-channel devices [23, 24]. During HC stress changes in the linear drain current $\Delta I_{\rm d,lin}$ ($I_{\rm d,lin}$ corresponds to $V_{\rm ds}$ = 0.05 V and $V_{\rm gs}$ = $V_{\rm dd}$) were recorded as functions of stress time t. In our recent publication [17] the deterministic HCD model was shown to accurately reproduce experimental $\Delta I_{\rm d,lin}(t)$ dependencies.

In the stochastic approach to HCD modeling the device architecture with continuous doping profiles was used to generate a set of 200 different instantiations with discrete dopants (see [10, 11] for details). In each of these instantiations RDs are distributed throughout the device in a unique manner. Then for each of these RD configurations we solved the Boltzmann transport equation, obtained carrier energy distribution functions, calculated interface state densities $N_{\rm it}$ (depicted in Fig. 2), and then $\Delta I_{\rm d,lin}(t)$ traces. The dependencies of $\Delta I_{\rm d,lin}(t)$ on stress time t were used to extract device lifetimes (lifetime is defined as time when the relative change of the linear drain current reaches 10%). Note that all these calculations were preformed for two stress voltages ($V_{\rm ds}$ = 1.7 V, $V_{\rm gs}$ = 1.8 V and $V_{\rm ds}$ = 1.8 V, $V_{\rm gs}$ = 1.9 V) and for much milder biases $V_{\rm ds}$ = $V_{\rm gs}$ = 1.0 V which imitate conditions very similar to the operating regime.

III. Results and Discussions

Fig. 3 shows distributions of $\Delta I_{\rm d,lin}$ changes evaluated for three aforementioned combinations of stress voltages. These $\Delta I_{\rm d,lin}$ distributions become broader with stress time. Also, as we showed in [10, 11], distributions of the linear drain current $I_{\rm d,lin}$ become broader. This trend contradicts the result reported by Schlünder *et al.* [9] where the authors showed that the drain current variability slightly improved during long-term (up to 10 years) hot carriers stress. However, Schlünder and co-authors used a technique which allows extrapolation to long stress times at device use conditions; such techniques are typically based on empirical/phenomenological expressions and therefore are not sufficient to capture the entire complexity of HCD.

Fig. 4 shows $\{\Delta I_{\mathrm{d,lin}}, I_{\mathrm{d,lin}}^{(0)}\}$ tuples (where $I_{\mathrm{d,lin}}^{(0)}$ is the time-zero linear drain current) obtained for 200 instantiations and plotted for all three combinations of stress voltages and one stress time step with $t = 2\,\mathrm{s}$. Because the data shown in Fig. 4 are very scattered, in order to extract a (possible) $\Delta I_{\mathrm{d,lin}}(I_{\mathrm{d,lin}}^{(0)})$ dependence we performed the robust linear fits using the Kendall rank correlation coefficient [25]. One can see that all three datasets exhibit highly significant rank correlation. Moreover, plotted trends clearly show that the change in the linear drain current becomes more pronounced in FinFETs with higher values of $I_{\mathrm{d,lin}}^{(0)}$.

In the same manner we computed $\Delta I_{\mathrm{d,lin}}(I_{\mathrm{d,lin}}^{(0)})$ dependences for each stress time step which are summarized in Fig. 5. We can conclude that for each value of t the degradation remains more pronounced in "initially better" devices (i.e. in devices with higher $I_{\mathrm{d,lin}}^{(0)}$ values). Dependencies of device lifetime on the time-zero linear drain current (see Fig. 6) show visible TTF reduction with increasing $I_{\mathrm{d,lin}}^{(0)}$ and this behavior is consistent with the trend pronounced in Figs. 4 and 5. Note finally, that a very similar reduction of ΔV_{th} variability at long BTI stresses was previously reported in [3].

IV. Conclusions

We statistically processed linear drain current HCD traces $\Delta I_{\mathrm{d,lin}}(t)$ which were calculated for 200 configurations of random dopants in the n-channel FinFET. This analysis allowed us to identify correlation between time-zero linear drain currents and their changes during stress and then extract the dependence of device lifetime on $I_{\mathrm{d,lin}}(t = 0)$. The obtained trends show that superior FinFETs with initially higher $I_{\mathrm{d,lin}}$ values degrade faster and have shorter lifetimes.

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