Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs

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Abstract

Transistors fabricated on SiC substrates show superior properties for their application in high-power electronics. However, the performance of SiC MOSFETs in general can still not be completely exploited yet due to a higher defect density compared to Si/SiO_2 based devices. The defects give rise to a distinct hysteresis in the transfer characteristics and increased drifts of the threshold voltage over time, i.e. bias temperature instabilities, making accurate time-to-failure analysis more challenging. In our work we carefully analyze lateral channel SiC MOSFETs utilizing measure-stress-measure (MSM) schemes. To explain the experimental data we perform physics based device simulations considering the impact of a large set of single defects employing a two-state non-radiative multiphonon defect model. This approach allows us to extract defect bands for electron and hole trapping and to link them to possible defect structures proposed in the literature. Additionally, we compare simulation results employing our extracted trap bands with MSM data measured on vertical channel devices. Finally, an accurate lifetime prediction at operating conditions is presented.

Introduction

To further enhance the efficiency of MOSFETs for power conversion applications SiC has emerged as a perfectly suitable substrate material. Even though the performance of 4H-SiC MOSFETs has been substantially improved in the recent past, their reliable operation is still affected by numerous defects located in the proximity of the channel. In contrast to Si devices only little attention has been put on modeling of defects and their impact on the SiC device characteristics so far. The large number of defects present in SiC devices cause a sub-threshold hysteresis of the transfer characteristics and also large drifts of V_{th}.[1–3] While the former is typically considered a fully reversible effect, the latter accounts for long term drifts of V_{th}, giving rise to the so called bias temperature instability (BTI). The microscopic origin and energetic distributions of defects causing this behavior are still debated for SiC.[4] In general the defects can be categorized into (i) interface states, (ii) border and (iii) oxide traps.[5,6] From experiments it has been observed that the defect densities strongly depend on processing parameters, e.g. post oxidation annealing (POA), and also on the channel surface termination, which is different for lateral and vertical channel devices, as schematically shown in Fig. 1.

Even though empirical models are often used to explain the observed device characteristics, a physics based model is indispensable for accurate description, especially for reliable time-to-failure analysis. Tyaginov *et. al*[7] focused on the up-sweep $I_{\mathrm{D}}(V_{\mathrm{G}})$, and successfully modeled the temperature dependence by mainly considering pre-existing border traps. The charge trapping kinetics of these traps has been described by a non-radiative multiphonon (NMP) model.[8] In this work we use this model implemented in the 1D simulator Comphy[9] to rigorously investigate positive BTI (PBTI). For this we apply extended MSM (eMSM) sequences[10] on lateral SiC MOSFETs and calibrate the border trap distributions to explain the recorded ΔV_{th}. To further increase the accuracy of the calibration a pulse eMSM (pMSM) scheme is used as well. This enables the separation of the independent parts of the degradation. We compare the extracted trap distributions to vertical devices, and finally present a physics based device lifetime prediction.

Experimental

During operation at two distinct gate biases ($V_{\mathrm{G}}^{\mathrm{L}}$,$V_{\mathrm{G}}^{\mathrm{H}}$) a selective part of defects given by the active energy region (AER), see Fig. 2, can become charged/discharged and therefore lead to a drift of device parameters. This AER is determined by the positions of the Fermi-level E_{F} relative to the energetic position of the trap level E_{T} of the defects at low gate bias $V_{\mathrm{G}}^{\mathrm{L}}$ and high gate bias $V_{\mathrm{G}}^{\mathrm{H}}$. Compared to Si nMOSFETs the AER is slightly higher in the SiO_2 band gap in SiC nMOSFETs. Fig. 3 shows the AER during a sweep of V_{G} with a large hysteresis of I_{DS}, which is due to defects that capture charge during the up-sweep of V_{G} but do not have enough time to emit the charge during the down-sweep. The width of the hysteresis itself (Fig. 4) depends on $V_{\mathrm{G}}^{\mathrm{L}}$ and $V_{\mathrm{G}}^{\mathrm{H}}$ and on the sweep rate (SR).[3] As the degradation obtained from eMSM sequences is typically expressed as a shift of V_{th}, an initial $I_{\mathrm{D}}(V_{\mathrm{G}})$ characteristics is recorded to map I_{DS} to ΔV_{th}, as shown in Fig. 5. For this sweep it is very important to use the maximum SR = $50\,\mathrm{V\,s^{-1}}$ of the measurement tool and a very narrow bias range to conserve the pristine charge state of the device. For the subsequent stress and measure phases the stress and recovery times are successively increased, i.e. $t_{\mathrm{s}} = 10^{-2}$ to 10^{4} s and $t_{\mathrm{r}} = 100$ to 10^{5} s. The first measurement point after stress is recorded with a minimum delay of $t_{\mathrm{delay}} = 10^{-4}$ s. The employed lateral devices (L × W = (2,4,6) × 100µm) with a-SiO_2 gate insulator are stressed at fields in the range of $E_{\mathrm{ox,s}}^{\mathrm{eff}} = 3$ to $8\,\mathrm{MV\,cm^{-1}}$. Note that V_{D} is held at 0 V during stress and low ($V_{\mathrm{D}} = 0.6$ to 1.0 V) during the measure phase, to ensure a uniform carrier distribution along the channel.

Modeling and Simulation

As previously mentioned, we employ Comphy and the implemented two-state NMP model which has already been demonstrated to accurately explain BTI for Si technology with various gate stacks.[11] Contrary to the conventionally used elasitc tunneling models, in the NMP model the change in the atomic configuration is considered which results from a change in the charge state, consistent with DFT calculations[12] and experimental data.[13] In essence, each defect is considered to dwell either in its neutral or charged state. Transitions between these states are described by energetic barriers as shown in Fig. 6 in the configuration coordinate diagram. The perturbation of the channel electrostatics due to the trapped charge is accounted for in a non-self consistent manner by changing V_{G}, which leads to significantly reduced computational cost at low error compared to a fully self-consistent calculation. To more realistically approximate the band-edges near the SiC/SiO_2 interface the transitions are not assumed to be abrupt, but are linearly smoothed over 5 Å.[14] To explain the eMSM data from Fig. 7 we start with an acceptor like border trap band which has been previously extracted for Si/SiO_2 gate stacks and termed

shallow electron trap band (EB) as an initial guess.[11] The simulation results reveal that the tails of the recovery traces can already be explained nicely, see Fig. 7 (top). To further account for the fundamentally different interface of SiC MOSFETs which is visible as a fast recoverable component in the MSM data, a spatially narrow distributed defect band within the transition region between SiC and SiO_2 is introduced, see Fig. 7 (center). Note that these defects show transition barriers within the weak electron-phonon coupling regime, resulting in effective Shockley-Read-Hall (SRH) rates.[11] The combination of both trap bands finally leads to good agreement with experimental data, as visible in Fig. 7 (bottom). Particularly noteworthy is that the long term degradation data can be reprocuced by the simulation using the same defect band as known from Si/SiO_2 devices. The transition time distribution of both identified trap bands are also visible in the capture emission time (CET) map[15] which can be calculated from the eMSM data, c.f. Fig. 8. It agrees well with the CET map from our simulations visible in Fig. 9. The latter is clearly dominated by the fast EB, with many defects showing small transition times. The corresponding trap parameters are summarized in Tab. 1.

In order to experimentally separate the two defect contributions, pMSM sequences as schematically shown in Fig. 10 are used. In contrast to eMSM sequences a bias pulse with constant $t_{\mathrm{pul}} = 10\,\mathrm{s}$ is introduced after the stress and before recovery to accelerate the charge emission of all defects. As can be seen in Fig. 11 (top row) the pulse fully recovers the traps of the fast EB and the resulting recovery trace can be entirely described by the shallow EB. By decreasing $V_{\mathrm{G}}^{\mathrm{pul}}$ from 0 V to a more negative bias the AER for charge trapping increases and captured holes start to impact the ΔV_{th} characteristics as well. Additional donor like trap bands arranged at the lower part of the AER account for the impact of the hole traps, and lead to good agreement with the experimental data measured down to $V_{\mathrm{G}}^{\mathrm{pul}} = -5\,\mathrm{V}$, as shown in Fig. 11 (bottom row).

Results and Discussion

Lateral: To fully model BTI in lateral nMOSFETs we employ a ramped voltage stress (RVS) scheme[16] to cover the regime of NBTI. A constant $t_{\mathrm{s}}/t_{\mathrm{r}}$ at subsequently increasing $V_{\mathrm{G}}^{\mathrm{s}}$ and decreasing $V_{\mathrm{G}}^{\mathrm{r}}$ is used, as depicted in Fig. 12 (inset). Again, the obtained AER determines the range of defects which can be accessed by experiment. Considering two donor trap bands (c.f. Tab. 1) the main aspects of NBTI data can be consistently explained, c.f. Fig. 12. The strong temperature dependence of charge trapping offers another possibility to extend the experimental window. At room temperature a significant number of the simulated defects is not accessible due to large charge transition times, see Fig. 9, and thus contribute as fixed interface charge. However, this charge is partly released at $T = 125\,^{\circ}\mathrm{C}$, as can be seen in the $I_{\mathrm{D}}(V_{\mathrm{G}})$ from Fig. 4 which shows approximately a 1 V shift of the V_{th}. The altered electrostatic situation in the channel can be described by removing fixed charge at the interface in the simulation and finally allows us to reproduce PBTI and NBTI recovery at $T = 125\,^{\circ}\mathrm{C}$ very well, see Fig. 13.

Vertical: Following the careful calibration of our simulation environment to lateral devices, we now apply the MSM sequences to vertical channel nMOSFETs. To emphasize the deviation of defect distributions of the different interfaces we compare the experimental data with simulations using the extracted defect bands for lateral devices. Therefore we adjust the work function difference $\Delta E_{\mathrm{w},0}$ for the gate material used for vertical devices. The simulations slightly deviate from the experimental data at short readout times t_{r}. However, the degradation behavior at long t_{r} can be explained by the shallow EB, see Fig. 14, confirming that part of the contributing defects are intrinsic to SiO_2. Note that the trap density N_{T} of the fast EB has been altered to account for the different interface structure.

Defect Structures: The extracted trap densities in Fig. 15 also agree well with experimentally observed distributions.[3,17] As possible defect candidates many different structures have been proposed for bulk SiO_2 and interface defects, see a small excerpt in Fig. 16. For instance a strained O-Si-O bond can act as electron trap[18] with its CTL close to the AER and exhibit comparable defect densities in bulk SiO_2. This trap type could be responsible for intrinsic electron traps identified by Afanas'ev *et. al* in SiC/SiO_2.[17] In addition to the slow border traps, carbon dangling bonds $(\mathrm{P_{b,C}})$ are suitable candidates for the fast recoverable component. They have been detected by EDMR measurements and calculated using ab-intio methods.[19] Their CTLs are close to the mean E_{T} values of our defect bands. In earlier studies a Si-C-O_2 structure has been proposed to contribute to defect densities near $E_{\mathrm{C,SiC}}$ [20]. The increased amount of N deposited at the interface during an NO POA has been correlated to increasing trap densities close to $E_{\mathrm{C,SiC}}$.[21] Therefore $\mathrm{N_C V_{Si}}$[22] is also a likely defect candidate in SiC devices. The increased trap density close to the $E_{\mathrm{V,SiC}}$ could be attributed to carbon dimers at interstitial positions or replacing oxygen atoms.[23]

Lifetime: To determine the time-to-failure of our devices we first analyze the time required to observe $\Delta V_{\mathrm{th}} = 0.6\,\mathrm{V}$, see Fig. 17. Note that, ΔV_{th} can spuriously appear to be smaller at $T = 125\,^{\circ}\mathrm{C}$ compared to room temperature for certain t_{delay} and $V_{\mathrm{G}}^{\mathrm{s}}$ combinations. For the extrapolation of ΔV_{th} under BTI conditions to typical device lifetimes of 10 years a power-law is frequently applied to experimental data. However, the power-law predicts an unphysical non-saturating trend of ΔV_{th}. The simple thermal activation approach,[24] however, assumes normally distributed τ_{c} and accounts for the saturation of V_{th}. Nevertheless, as both models are directly applied on the experimental data the conclusions strongly depend on the readout delay t_{delay} and predict either a too pessimistic (power law) or too optimistic lifetime (thermal activation), as shown in Fig. 18. The extraction from our physical device simulations nicely explain the MSM data and give a $\Delta V_{\mathrm{th}} \approx 0.6\,\mathrm{V}$ (t_{delay}= 1 s) at DC bias conditions after 10 years of stress.

Conclusions

We characterize and simulate charge trapping in lateral SiC MOSFETs. Advanced measurements (eMSM,pMSM,RVS) with long stress and recovery times are conducted on both SiC technologies and fully reproduced through simulations. Our simulations rely on the two-state NMP model to describe the charge transitions of the involved border traps. Two electron (shallow and fast) and hole trap bands are identified and used to explain PBTI and NBTI in lateral devices. The shallow traps modeled with similar parameters as in Si/SiO_2 suggest an intrinsic charge trapping behavior of SiO_2, which is supported by a comparison with slow V_{th} drifts in vertical devices. Based on our simulations accurate lifetime predictions can be made. While empirical models appear to provide too pessimistic (power law) predictions, our results provide a physics based extrapolation at operating conditions.

Acknowledgement

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References

[1] P. M. Lenahan *et al.*, MR **81**, 1 (2018). **[2]** T. Aichinger *et al.*, MR **80**, 68 (2018). **[3]** G. Rescher *et al.*, IEDM 10.8.1 (2017). **[4]** D. M. Fleetwood, MR **80**, 266 (2018). **[5]** A. J. Lelis *et al.*, T-ED **55**, 1835 (2008). **[6]** H. Yano *et al.*, T-ED **62**, 324 (2014). **[7]** S. Tyaginov *et al.*, *IIRW*, IEEE (2018), p. 1. **[8]** T. Grasser, MR **52**, 39 (2012). **[9]** Comphy, 2019, http://comphy.eu/, 2019-07-13. **[10]** B. Kaczer *et al.*, *IRPS*, IEEE (2008), p. 20. **[11]** G. Rzepa *et al.*, MR **85**, 49 (2018). **[12]** W. Gös *et al.*, MR **87**, 286 (2018). **[13]** T. Grasser *et al.*, *IRPS* (2010), p. 16. **[14]** F. Devynck *et al.*, PRB **76**, 075351 (2007). **[15]** H. Reisinger *et al.*, *IRPS*, IEEE (2010), p. 7. **[16]** A. Kerber *et al.*, EDL **34**, 960 (2013). **[17]** V. Afanas'ev *et al.*, Phys.stat.sol.(a) **162**, 321 (1997). **[18]** A.-M. El-Sayed *et al.*, PRB **89**, 125201 (2014). **[19]** J. Cottom *et al.*, JAP **124**, (2018). **[20]** F. Devynck *et al.*, PRB **84**, 235320 (2011). **[21]** H. Yoshioka *et al.*, JAP **112**, 024520 (2012). **[22]** J. Cottom *et al.*, JAP **119**, (2016). **[23]** P. Deak *et al.*, J.Phys.D:Appl.Phys. **40**, 6242 (2007). **[24]** T. Grasser, *BTI for dev. and circ.* (Springer, 2013). **[25]** T. Kimoto *et al.*, *Fund.of SiC technology* (J.W&S, 2014). **[26]** C. Raynaud *et al.*, Dia.Rel.Mat. **19**, 1 (2010).

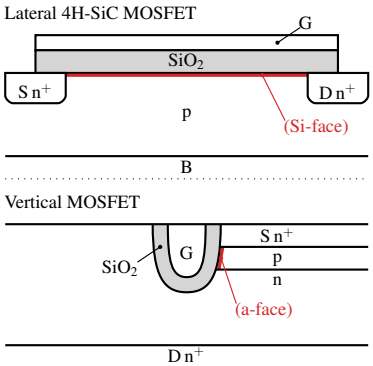

Figure 1: Schematic of a **(top)** lateral 4H − SiC/SiO_2 transistor with Si-face (0001) terminated interface and a **(bottom)** state-of-the-art vertical channel MOSFET with a-face ($11\bar{2}0$) terminated interface. The simulation tools are adjusted and used to explain lateral devices, and finally benchmarked with vertical devices.

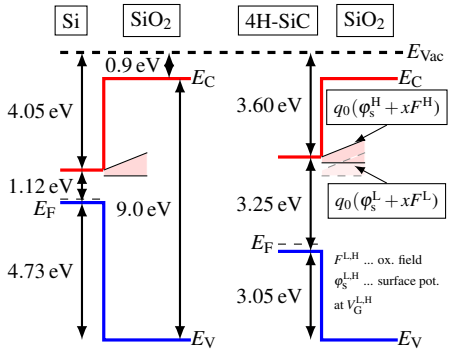

Figure 2: Band diagram with active energy regions (AER, red) for charge trapping for **(left)** Si/SiO_2 and **(right)** 4H − SiC/SiO_2 nMOS devices. For SiC-nMOS the AER for digital gate bias operation lies slightly higher, and thus border traps with different trap levels compared to Si determine the device behavior.

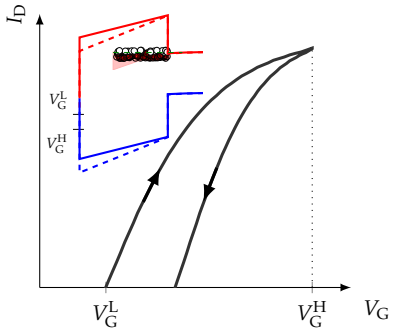

Figure 3: SiC devices exhibit a significant subthreshold hysteresis, shown with the band diagram and the AER. Border and near interface traps can get charged during upsweep (filled circles) and do not release their charge during downsweep depending on their charge transition times, leading to a shift of V_{th}.

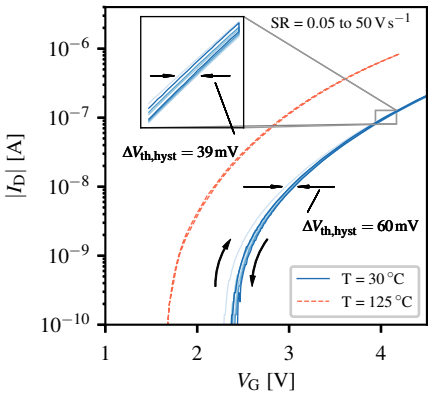

Figure 4: $I_D(V_G)$ sweeps recorded subsequently at increasing sweep rates SR show a pronounced hysteresis in I_{DS}, which further depends on V_G^L and V_G^H.[3] Thus to preserve the device pristine charge state it is inevitable to record the $I_D(V_G)$ in a narrow bias range around V_{th}. The upsweep curve at max. SR is consequently used to map back I_{DS} observed in the MSM sequences to ΔV_{th}.

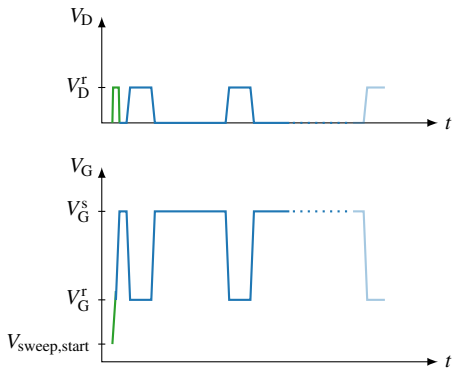

Figure 5: Typical eMSM sequence for the study of BTI in large area MOSFETs. After a narrow $I_D(V_G)$ is measured, a subsequent series of stress phases and recovery phases with increasing times are applied. During recovery a small drain bias is applied to monitor ΔV_{th}. The recovery data are used subsequently to extract trap distributions.

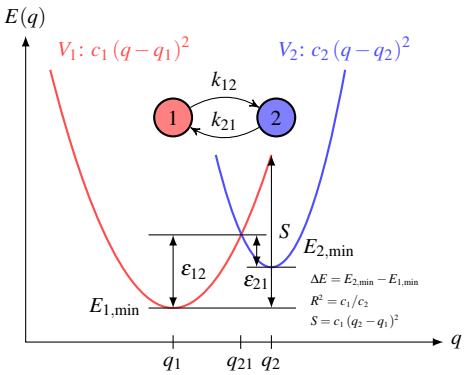

Figure 6: Defect charge transitions can be well described by the two state non-radiative multiphonon model. The two charge states are shown together with the potential energy surfaces which determine the transition rates, shown in the configuration coordinate diagram. The computationally efficient model has three main parameters ΔE, R, and S.

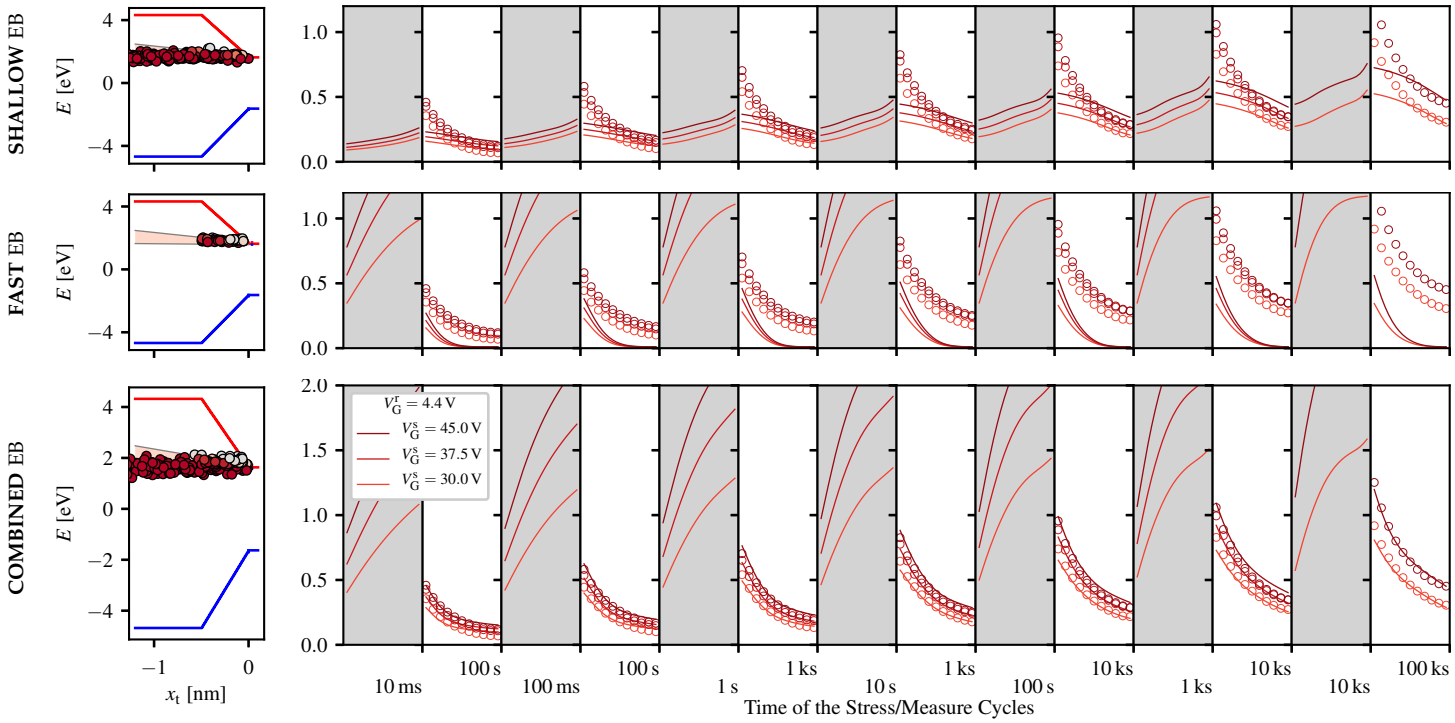

Figure 7: Measured (circles) ΔV_{th} utilizing eMSM sequences at different V_G^s and at constant $V_G^r = 4.4$ V at $T = 30$ °C and **(top)** simulation results (lines) considering the shallow electron trap band (EB) originating from border traps as extracted in[11] for Si/SiO_2 technology. The simulation explains the tails of the recovery data measured after large stress times pretty well, whereas the fast recovery behavior is not sufficiently explained with the shallow EB. **(middle)** The fast EB accounts for the large fraction of the recovery data measured within the first few decades immediately after stress release. This contribution can be ascribed to near interface traps arranged in the transition region between the substrate and oxide. **(bottom)** The combination of both defect bands shows a good agreement with the experimental data, especially for long stress and recovery times. Note that the defects in the band diagrams are sampled with a Monte Carlo method for better illustration, while a uniform grid is used in the simulation.

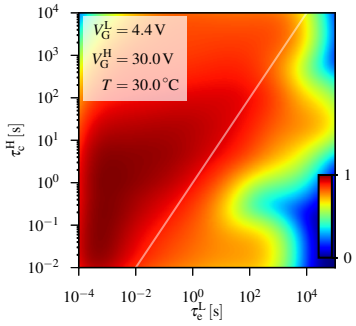

Figure 8: Experimental CET map calculated from eMSM data. The fast EB is visible as peak in distribution within the first decades of τ_e. A contribution of the shallow EB is visible at large τ_c and τ_e.

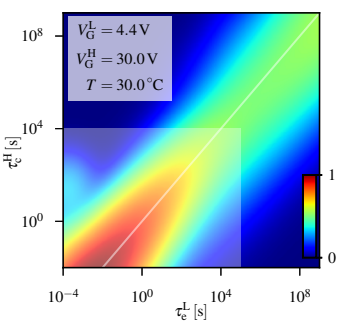

Figure 9: The simulated CET map is dominated by defects of the fast EB. Significant for the shallow EB are widely distributed τ_c and τ_e explaining the long term degradation associated with BTI.

quantity	ref.	value	unit
$E_{G,0}$	25	3.36	eV
$E_{G,1}$	26	$-3.3\cdot10^{-4}$	eVK^{-1}
m_l	25	0.33	1
$m_{t,0}$	25	0.42	1
N_{cv0}	25	$2.54\cdot10^{19}$	cm^{-3}
M_c	25	3	1
$\epsilon_{r,chan}$	25	9.76	1

parameter	TB1	TB2	TB3	TB4	
$\overline{E}_T \pm \sigma_{E_T}$	1.87±0.08	1.73±0.165	-1.12±0.24	-1.77±0.04	eV
$\overline{s} \pm \sigma_S$	-	4.93±1.95	5.2±4.89	-	eV
R	-	0.437	1.19	-	1
N_T	$2.8\cdot10^{19}$	$3.44\cdot10^{19}$	$1.26\cdot10^{19}$	$7.3\cdot10^{18}$	cm^{-3}

Table 1: Substrate channel material **(top)** parameters and the extracted defect band **(bottom)** parameters for fast EB (TB1), shallow EB (TB2) and donor like traps (TB3,4) used in our simulation.

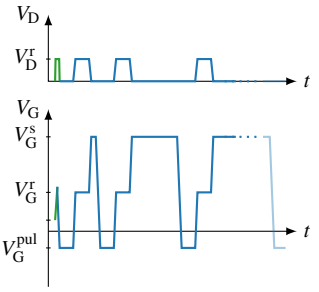

Figure 10: pMSM sequence with additional pulse prior recovery to accelerate charge emission. This enables experimental separation of defects with small and large transition times.

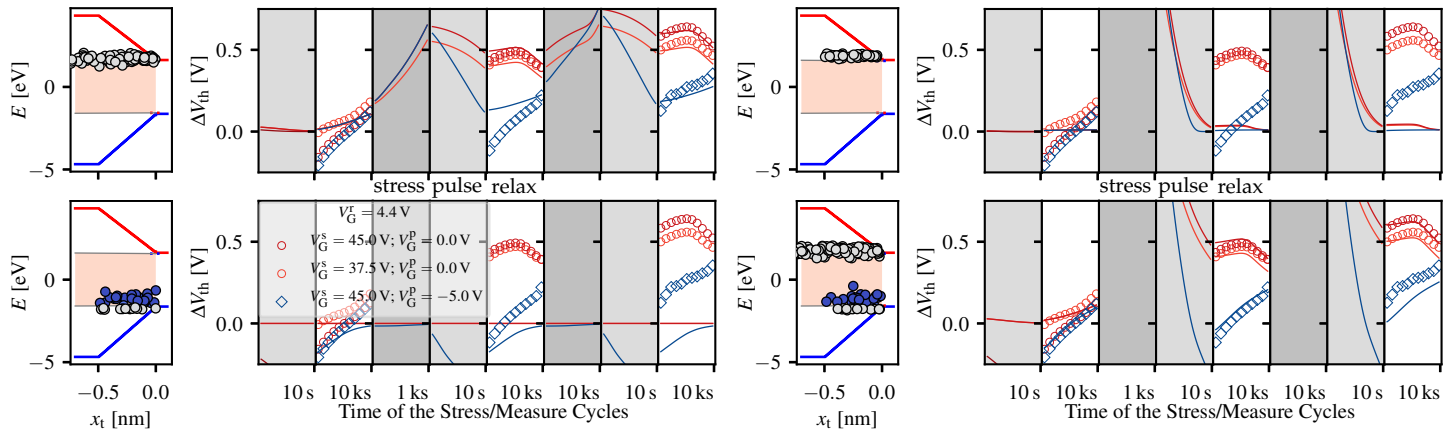

Figure 11: **(top, left)** The pMSM sequence shows that a switch to the depletion regime leads to accelerated emission of the fast recovering states. **(top, right)** The shallow EB solely explains the long term recovery behavior as long as the impact of NBTI can be neglected. **(bottom, left)** Increasing the pulse to more negative bias stimulates hole trapping when approaching the accumulation regime which is accounted for by donor like traps in the simulation. **(bottom, right)** The combination of all defect distributions is dominated by the shallow EB and consistently explains the experimental data.

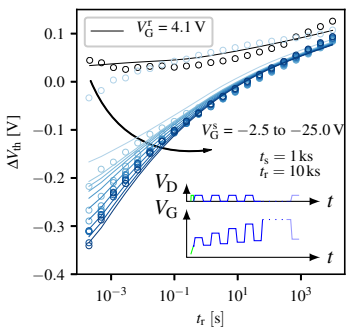

Figure 12: $t_r = 100\,ks$ ΔV_{th} trace of a pristine device (black) recorded before NBTI recovery (blue) during a RVS sequence (inset). Our simulations explain the recovery data for $V_G^s < -2.5\,V$ well.

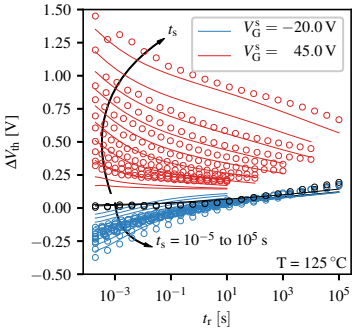

Figure 13: ΔV_{th} recovery data (symbols) at elevated temperature in comparison to the simulation (lines). Additional fixed charges account for the altered device electrostatics (c.f. Fig. 4).

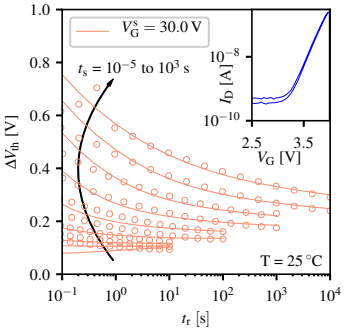

Figure 14: Vertical nMOS recovery data and simulations with the same defects as used for lateral nMOS. N_T of the fast EB has been slightly modified to account for the different interface.

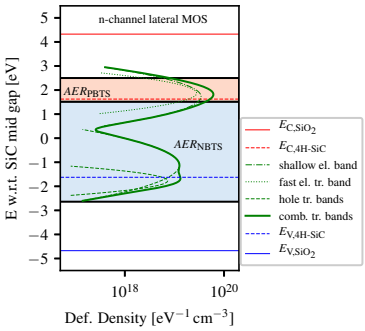

Figure 15: Defect densities within the first 5 Å from interface. Extracted densities cover the main features of those extracted by experiments[17] (not shown), like the steep increase towards $E_{C,SiC}$.

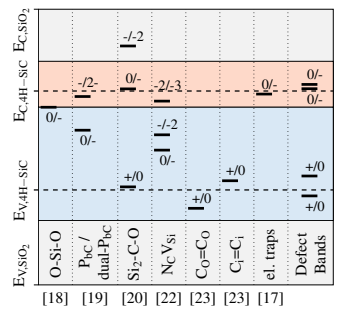

Figure 16: CTL levels of possible defect structures for charge trapping in SiC from ab-initio and electrical characterization methods, together with the mean E_T of the extracted defect bands.

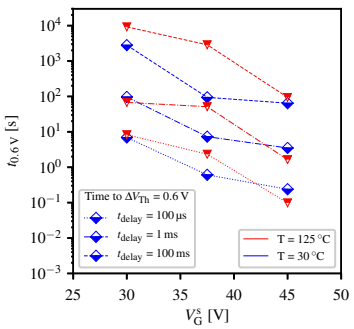

Figure 17: Bias dependence of stress time until $\Delta V_{th} = 0.6\,V$. Note that for certain combinations of t_{delay} and V_G^s, the time $t_{0.6V}$ can be observed higher at a higher T for a given V_G^s.

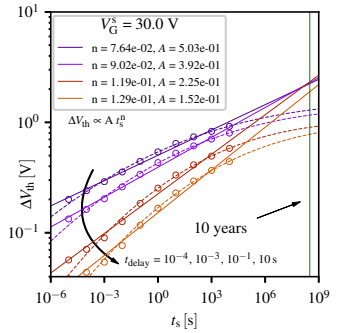

Figure 18: Empirical lifetime extrapolation with power-law and thermal activation models. The power law predicts an infinite increase of ΔV_{th} at large t_s, while the latter accounts for ΔV_{th} saturation.

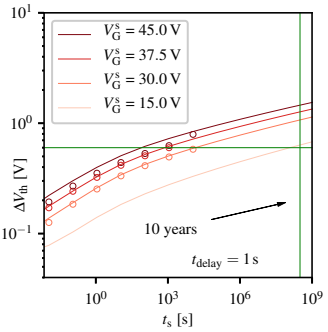

Figure 19: Accurate lifetime extrapolation from our calibrated simulation environment reveals an overall $\Delta V_{th} \approx 0.6\,V$ at operating conditions $V_G^s = 15\,V$ for a lifetime of 10 years.