CMOS Technology Compatible Magnetic Memories

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***Abstract*— With CMOS transistors' scaling showing signs of saturation, an exploration of new working principles suitable for emerging microelectronic devices accelerates. The electron spin is attractive for new device applications as a complement and a possible replacement of the electron charge currently employed by CMOS. The electron spin displays the two well-defined projections on an axis and is thus suitable for digital applications. In magnetic tunnel junctions (MTJs) the free magnetic layer possesses two orientations relative to the fixed layer: parallel and antiparallel. As the parallel and antiparallel magnetization configurations are characterized by different resistances, the thereby stored information can be read. MTJs enable a spin-based type of non-volatile magnetoresistive memory. MTJs are fabricated with a CMOS-friendly process and are quite CMOS compatible. The relative magnetization configuration can be written by means of a spin-transfer torque (STT) or a spin-orbit torque (SOT) acting on the free layer. The torques are caused by spin-polarized electrical currents and not by a magnetic field. Electrically addressable non-volatile magnetoresistive memories are attractive for stand-alone and embedded applications. The state-of-the art concepts of STT and SOT memory, in particular the required modeling approaches, are reviewed, with a particular focus on a fast external magnetic field free switching in advanced SOT-MRAM.**

Keywords—Magnetoresistive random access memory, MRAM, spin-transfer torque MRAM, spin-orbit MRAM, perpendicular magnetization, magnetic field free switching, two-pulse switching

Continuous miniaturization of semiconductor devices ensures an outstanding performance increase of modern integrated circuits. While semiconductor chips based on the 5nm technology node are approaching production, the research is shifting towards the 3nm technology node [1]. To satisfy the increasing demand for high performance CPUs and high-density storages, a disruptive technology based on a new physical phenomenon is urgently needed. As the growing power consumption becomes incompatible with the global demands of accelerating the vital industrial growth, new devices must also obey energy efficient solutions.

An attractive path to dramatically reduce the power consumption by reducing the leakage currents in modern integrated circuits is to introduce non-volatility. Non-volatility enables stand-by power free electronics which is in high demand by Internet-of-Things, automotive, and energy efficient Edge-related applications.

Magnetic tunnel junctions (MTJs) are perfectly suited as key elements of emerging nonvolatile CMOS-compatible magnetoresistive random access memory (MRAM) [2]. An MTJ possesses a simple structure of a sandwich made of two metallic ferromagnetic layers separated by a thin tunneling barrier. The digital information is encoded into two relative magnetization states with parallel and antiparallel orientations of the magnetic layers. As the tunnel resistances of these two states are different, it provides a way to access the information electrically. As the relative magnetization state can be altered by passing the electric current through the MTJ, it enables a purely electrical way to write the information into the relative magnetization state. The free layer magnetization switching is due to the current-induced spin-transfer torque (STT) [3], [4].

Perpendicularly magnetized MTJs, or p-MTJs, demand a smaller footprint than in-plane MTJs and are better suited for high-density memory applications [2]. The recent discovery of an interface-induced perpendicular anisotropy in CoFeB/MgO stacks [5] has enabled p-MTJ based MRAM with a high barrier separating the two magnetization states.

However, the switching currents are large, and their reduction represents an important challenge. Importantly, the switching current cannot be reduced at an expense of reducing the thermal barrier. The thermal barrier defines the memory cell's thermal stability and must be as high as 80 k_BT for 10 years of data retention of 1Gbit circuits. A free layer composed of CoFeB/Ta/CoFeB possesses two MgO interfaces [6], which boosts the thermal barrier. The Gilbert damping is also reduced in composite free layers [6] allowing a reduction of the switching current at the same time.

In order to scale the diameter of MTJs beyond 10nm, the use of shape anisotropy was recently suggested [7]. By elongating the FeB free layer along the direction perpendicular to the interface with MgO, the thermal stability can be increased for small diameters without sacrificing the tunneling magnetoresistance ratio (TMR).

For fabricating STT-MRAM with CMOS circuits, MTJs must withhold at least 400C°, the temperature of the back-end-of-line (BEOL) process. To integrate MTJs, the fixed more stable layer can be put on top of an MTJ. A stronger ferromagnetic exchange coupling can be used to pin the fixed layer within a synthetic ferromagnet [8]. However, to preserve the symmetry of switching between the parallel and the antiparallel configuration and back, an additional compensating magnet must be incorporated in the structure.

For reliable and fast information reading, a large TMR is required. The problem of increasing the TMR becomes more pronounced with MTJs' downscaling, because it becomes increasingly difficult to control the bit-to-bit resistance variation in small MTJs. As the resistance variation dispersion increases, the TMR must also grow to guarantee a sufficiently broad window for reliable reading. In order to continue with devices' scaling down, discovering MTJ materials capable to provide a TMR above 1000% is a pressing challenge [9].

STT-MRAM is characterized with a fast access time (10ns). It possesses high endurance (10^{12}) and is compatible with the BEOL CMOS process. STT-MRAM is also particularly attractive for use in Internet of Things, automotive, and Edge applications. It is considered as a nonvolatile replacement of conventional volatile CMOS-based DRAM and non-volatile flash memory. Although 4Gbit STT-MRAM arrays have been already reported [10], currently

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embedded implementations of 8Mb 1T-1MTJ STT-MRAM on a 28nm fully-depleted silicon-on-insulator CMOS logic platform [11] is provided. Recently, 128Mb embedded MRAM with 14ns writing speed was reported [12]. An embedded MRAM solution compatible with Intel's 22FFL FinFET technology is also available [13].

To further reduce the energy consumption in modern hierarchical multi-level processor memory caches currently mastered by SRAM it is essential to replace SRAM with a non-volatile solution. As STT-MRAM can in principle serve in L3 caches [14], the switching current density becomes very large at an access time of 5ns or shorter and may damage the tunneling oxide. In order to replace SRAM in higher-level caches, an even faster operation is required, and a new physical switching principle must be introduced.

Among the newly discovered physical phenomena suitable for next-generation MRAM is spin-orbit torque (SOT) assisted switching. In SOT-MRAM cell the MTJ's free layer is grown on a material with a large spin Hall angle [15], [16]. The current running through the material creates a high spin accumulation at the interface with the free layer. The spin accumulation diffuses into the free layer and produces a spin current and a torque capable of switching the free layer magnetization. The interface spin accumulation can also be created in materials with a strong spin-orbit interaction due to the correlations between the spin orientation and the momentum direction. Topological insulators intrinsically possess a strong spin-orbit interaction which results in spin-momentum locking, enormous spin accumulation, and strong SOTs switching the free layers at room temperature [17], [18].

The switching currents in SOT-MRAM are still large, however, they are injected in-plane along the heavy metal/ferromagnetic bilayer and do not flow through MTJs. To read the data, much smaller read currents are applied through the MTJs. Three-terminal spin-orbit torque SOT-MRAM was integrated on a 300mm CMOS wafer using CMOS compatible processes [19].

In order to switch a perpendicularly magnetizes free layer by a SOT deterministically a static in-plane magnetic field is required, which is not desired. Recently a scheme employing two orthogonal current pulses was proposed to achieve sub-ns deterministic switching without an external magnetic field [20].

Non-volatility introduced into data processing offers outstanding advantages over the standard CMOS-based Von-Neumann computing architecture and paves the way for a new low power and high-performance computation paradigm based on logic-in-memory [21] and in-memory [22], [23] computing. In these novel architectures suitable for future AI and cognitive computing [24] the same nonvolatile elements are used to store and to process the information.

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