Accelerated Capture and Emission (ACE) Measurement Pattern for Efficient BTI Characterization and Modeling

Zhicheng Wu[1*], Jacopo Franco, Dieter Claes[1], Gerhard Rzepa[2], Philippe J. Roussel, Nadine Collaert, Guido Groeseneken[1], Dimitri Linten, Tibor Grasser[2], Ben Kaczer

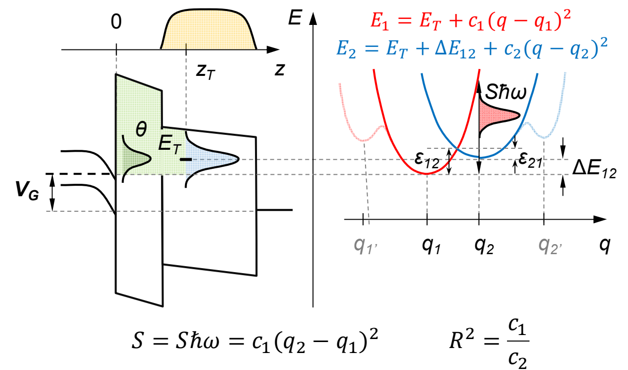
imec, Leuven, Kapeldreef 75, B3001 Leuven, Belgium
[1]also at ESAT-MICAS, KU Leuven, Belgium
[2]institute for microelectronics, T.U. Vienna, Austria
*email: Zhicheng.Wu@imec.be

***Abstract*—A new gate pattern is proposed to minimize test time while maximizing charge capture and emission into/from oxide defects for efficient and accurate BTI modeling. In conjunction with the imec/T.U. Vienna BTI simulation framework "Comphy", which encapsulates the microscopic behavior of individual defects, the Accelerated Capture and Emission (ACE) gate pattern streamlines a bottom-up approach for BTI evaluation from device to circuit level. The new pattern is systematically compared with the well-established Constant-Voltage-Stress (CVS) and Ramped-Voltage-Stress (RVS) methods and is found to show substantial improvements regarding both characterization and model-calibration efficiencies. The flow is further validated by showing good agreement between the direct projections of the model calibrated with the new pattern and experimental results of AC stress tests with various duty factors.**

***Keywords*—Bias temperature instability (BTI), life-time projection, MOSFET, non-radiative multi-phonon (NMP) model, reliability test and modeling.**

I. INTRODUCTION

BTI remains one of the major reliability concerns for deeply scaled transistors [1]. In the past decades, both empirical and physics-based models have been proposed to reproduce the complex BTI dynamics [2-4]. Among them, the 4-state non-radiative multi-phonon (NMP) model [2], verified through dedicated TDDS (Time Dependent Defect Spectroscopy) experiments [5], has been shown to successfully reproduce multiple aspects of BTI. However, the complexity of this multi-parameter model as well as the time-consuming experiments required for its calibration, discourage its adoption in an industrial environment. Efficient abstraction from 4-state to 2-state NMP model without sacrificing its physical essence has been demonstrated and applied to multiple devices technologies [6, 7]. However, for a CMOS HKMG technology, up to 4 oxide defect bands (electron and hole traps, in IL and HK) need to be represented, which still requires a total of 24 model parameters (i.e., 6 per defect band) in the simplified 2-state NMP model (Fig. 1). To accurately calibrate the (partially covariant) model parameters, large amount of information on the defect capture and emission processes needs to be probed experimentally, resulting in long stress and recovery test sequences. If



$$S = S\hbar\omega = c_1(q_2 - q_1)^2 \qquad R^2 = \frac{c_1}{c_2}$$

Six parameters for 1 defect band:
N_T, $<E_T>$, σ_{E_T}, $<S>$, σ_S, R

Fig. 1: The 2-state NMP model, as implemented in Comphy, requires 6 parameters to model each defect band [6]. $<E_t>\pm\sigma_{Et}$ denotes the distribution of oxide defect levels with respect to Si midgap; $<S>\pm\sigma_s$ and R serve as effective values for distributing the 2-state NMP model properties across different defects. Ultimately the activation energies for the capture and emission processes (ε_{12}, ε_{21}) from/to all possible charge reservoirs (i.e., Si conduction and valence bands, and metal gate) are computed (cf. Eqs 1-2); note they depend also on the defect spatial location and the gate stack electrostatics (i.e., electric fields), through the term ΔE_{12}. The multi-parameter model is inherently prone to covariance related pitfalls, if in-sufficient experimental information is fed into the parameter numerical optimizer.

insufficient experimental information is provided, local minima in the multi-dimensional parameter optimization space (related to the parameter covariance), can undermine the model calibration and therefore the predictive capability of the calibrated model.

In this paper, we design a new measurement pattern ("Accelerated Capture and Emission", ACE) by exploiting both the voltage and temperature acceleration of trapping *and* de-trapping processes. We calibrate first the parameters of the active defect bands during HKMG pMOS operation using this new pattern, and then compare the model projections with data measured by the conventional RVS ("Ramped Voltage Stress") or the more time-consuming CVS ("Constant Voltage Stress") tests. A systematic evaluation of different tests is given,

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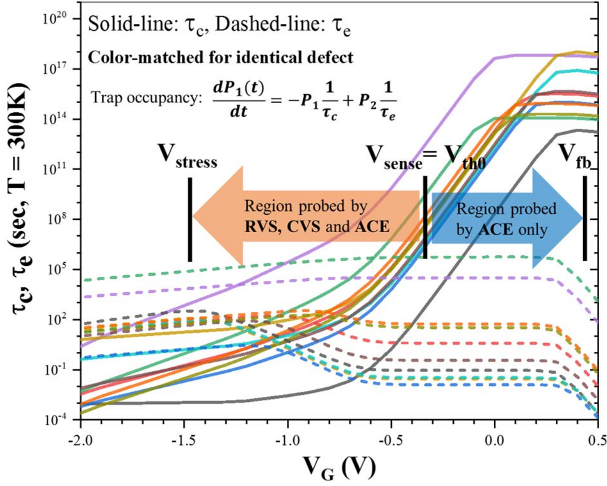


Fig. 2: Illustration of the voltage dependent capture and emission times of multiple defects, as calculated e.g., from the pMOS model calibrated in this work. While CVS and RVS are typically used for calibrating empirical power-law based acceleration models, they inherently exploit some physical features of the trapping process, e.g. CVS assesses the distribution of capture time constants of the defects energetically accessible at the applied gate bias, while RVS exploits the voltage acceleration of defect capture times to speed up the device degradation. Similarly, the newly proposed pattern exploits the voltage acceleration of both capture and emission processes to maximize the observable defect activity within a short test duration.

including a comparison of the fraction of defects probed by each test, the model calibration efficiency and the statistical robustness against covariance. We then expand our analysis to nMOS on the same HKMG wafer. The good projection accuracy of the Comphy model calibrated with the new ACE pattern, benchmarked also against AC stress data with varying duty factors recorded using an ultrafast (~$1\mu s$ delay) measurement system, serves as further validation of the proposed flow.

II. ACE TEST AND MODEL CALIBRATION

A crucial aspect of the NMP model (Fig. 1), is that both the charge capture and emission processes taking place during a given bias and temperature stress, are equally important for the model calibration. A typical example of the voltage dependence of the capture and emission times for selected defects during pMOS operation, is plotted in Fig. 2. Unlike the time-based CVS method, RVS [8] enables fast reliability screening by encompassing in a single measurement the voltage accelerated charge trapping. While CVS and RVS methods are used primarily for fitting an empirical power-law model, they both over-emphasize the charge trapping process (i.e., degradation) rather than the subsequent charge emission process (i.e., recovery); sufficient information about the recovery can only be achieved in a normal test at the expense of extremely long post-stress recovery traces (note: the fractional recovery of BTI proceeds apparently slower after stresses inducing larger degradation [9]).

To gain insight into the recovery process at minimum time expense, we design an "Accelerated Capture and Emission" [Fig. 3 (a), ACE] pattern, which includes, after each stress unit with increasing V_G, a bundle of discharge phases with gradually

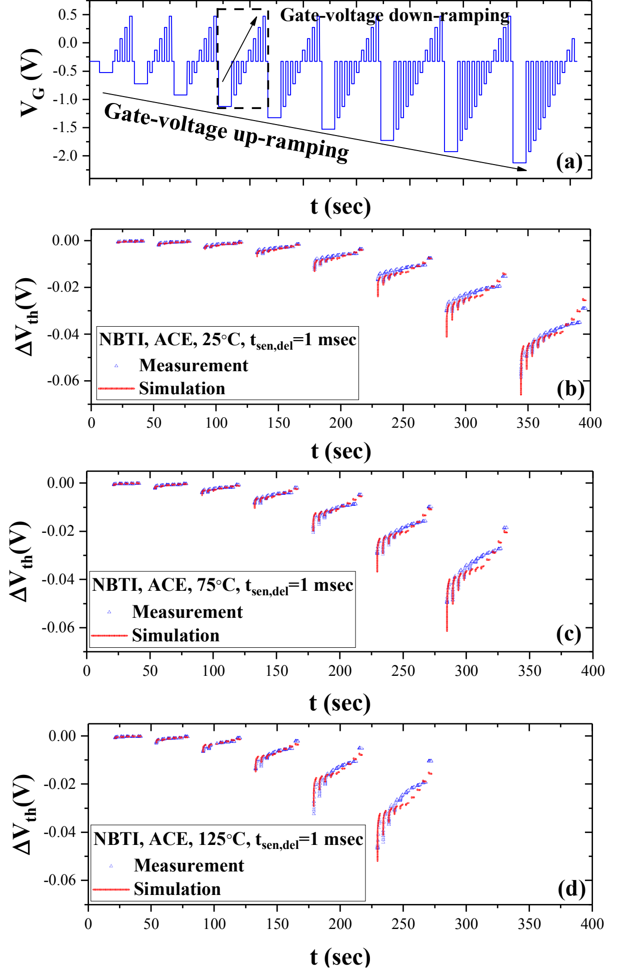


Fig. 3: The designed Accelerated Capture and Emission (ACE) test (a) aims at maximizing the capture and emission information within limited test duration and is intended to collect efficiently the data necessary for calibrating the physics-based BTI model implemented in Comphy. The ACE comprises a V_G up-ramping, which exploits the reducing trap capture time at increasing oxide electric fields (Fig. 2, left-arrow), while within a single unit [(a), dashed-lined box], a down-ramping voltage stairs until V_{fb} (i.e. $E_{ox}=0$) is used to accelerate the de-trapping process (Fig. 2, right-arrow) of the defects charged up to that point. The V_{th} shift is sensed periodically at $V_{sense}=V_{th0}$. The ACE sequence measured on HKMG pMOS at three temperatures is shown in panels (b), (c), (d), together with corresponding Comphy simulations.

reducing E_{ox} (note: the V_G is ramped down to V_{fb} to avoid applying an opposite E_{ox}, which might probe defect bands irrelevant for device operation, e.g. electron traps normally inactive during pMOS operation). Although this test sequence consisting of ramped charging and discharging voltages is apparently more complex compared to the standard RVS, it can be easily programmed in contemporary off-the-shelf semiconductor analyzer instruments, as the Keithley K26xx series or the Keysight B1530 (both used in this work). The benefits of biasing devices towards accumulation are two-fold: first, it accelerates the emission process by reducing the effective activation energy for the process (cf. ε_{21} in Fig. 1 and Eq. 2 below) and therefore boost the number of discharging (and following re-charging) events; second, it increases the capture time constant and, in turn, enhances the emission

Table I		pMOS	nMOS
IL (SiO_2)	N_T [cm^{-3}]	5.04×10^{19}	2.01×10^{18}
	$<E_T> \pm \sigma_{E_T}$ [eV]	-1.06 ± 0.26	0.62 ± 0.21
	$<S> \pm \sigma_S$ [eV]	5.04 ± 2.51	2.03 ± 0.77
	R [1]	2.75	1.30
HK(HfO_2)	N_T [cm^{-3}]	2.38×10^{20}	1.11×10^{21}
	$<E_T> \pm \sigma_{E_T}$ [eV]	-1.04 ± 0.20	0.89 ± 0.16
	$<S> \pm \sigma_S$ [eV]	9.27 ± 1.63	2.17 ± 0.58
	R [1]	2.76	0.30
Comment	imec planar device (W*L=10*1um), HKMG (MIPS), Gate-First process, EOT~0.8nm, other default setups as indicated in [6]		

Table Ⅰ: List of all defect bands parameters calibrated and used in this work. Note the distributed defect activation energies for the capture and emission processes are derived from the S and R parameters (cf. Eq.1-2). The EOT, channel doping and surface potential vs V_G are extracted using the CVC Hauser tool [10] to match a reference capacitance-voltage measurement. No self-consistent calculation is incorporated during defect band calibration/projection in this work, double well (DW) model for the quasi-permanent degradation is enabled with default parameters [6].

Table II			pMOS	nMOS
IL (SiO_2)	Capture at $\lvert V_G\rvert = \lvert V_{th0}\rvert + 0.7V$	$<\varepsilon_{12}> \pm \sigma_{\varepsilon_{12}}$	0.70 ± 0.27	0.38 ± 0.19
	Emission at $\lvert V_G\rvert = \lvert V_{th0}\rvert$	$<\varepsilon_{21}> \pm \sigma_{\varepsilon_{21}}$	0.26 ± 0.17	0.37 ± 0.17
HK(HfO_2)	Capture at $\lvert V_G\rvert = \lvert V_{th0}\rvert + 0.7V$	$<\varepsilon_{12}> \pm \sigma_{\varepsilon_{12}}$	0.85 ± 0.19	1.31 ± 0.34
	Emission at $\lvert V_G\rvert = \lvert V_{th0}\rvert$	$<\varepsilon_{21}> \pm \sigma_{\varepsilon_{21}}$	0.54 ± 0.12	1.04 ± 0.36
Comment	unit [eV]			

Table Ⅱ: List of activation energy distributions *calculated* for illustration purposes from the parameters in Table Ⅰ, using Eqs. 1-2. For simplicity, the activation energies are illustrated here only for charge exchange with the Si valence band for pMOS, or Si conduction band for nMOS–i.e., only for the most relevant transitions (note: for each defect, Comphy calculates charge transition probabilities towards all charge reservoirs, i.e. Si conduction and valence bands, and metal gate). The defects are assumed to be uniformly distributed across the oxide layers.

probability. This enhanced emission rate allows a better modeling of the defect.

The ACE measurements performed at three temperatures and the results were used for calibrating the defect band parameters in our simulation framework Comphy for a HKMG Gate-First technology. Fig. 3 documents how the calibrated model (parameters) excellently reproduces the complex charge and discharge features of the ACE data.

The device under study and the corresponding calibrated defect band parameters for this technology are summarized in Table I. Note that Comphy implements a simplified 2-state NMP model, which has been shown to reproduce reasonably well the characteristics of the more complete 4-state model (includes defect meta-stable states), at a significantly reduced computational complexity [6]. Due to the simplification from 4-state to 2-state, the NMP model parameters ($<S>\pm\sigma_S$ and R) are assumed to be effective values, while the other parameters ($<Et>\pm\sigma_{Et}$ and N_T) retain their physical meanings. The activation energies for the capture and emission processes are calculated from the values in Table I as [6]:

$$\varepsilon_{12} = \frac{S}{(R^2-1)^2}\left(1 - R\sqrt{\frac{S+\Delta E_{12}(R^2-1)}{S}}\right)^2 \qquad (1)$$

$$\varepsilon_{21} = \varepsilon_{12} - \Delta E_{12} \qquad (2)$$

A conversion of the parameters listed in Table I into the activation energy distributions (ε_{21}, ε_{12}) is shown in Table Ⅱ, to illustrate how the calibrated model parameters convert into a range of activation energies < ~1eV, consistent with the typical observations of single defect studies (e.g., temperature dependence of defect characteristic times as observed in Random Telegraph Noise or TDDS experiments [2,6,12]). For simplicity, only the activation energies for charge capture at operating voltage (i.e., $E_{ox,IL}$=3.8MV/cm) and for charge emission at V_G=V_{th0} are shown. Also, only the charge exchanges between the oxide defects and the dominant charge reservoir (i.e., Si valence band for pMOS, and Si conduction band for nMOS) are illustrated in Table Ⅱ. However, we note that Comphy calculates transition probabilities towards all charge reservoirs (i.e., Si band edges and metal gate) at each gate bias. As will be discussed later, a typical BTI test is able to probe only a small fraction (i.e., the lower tail) of the distribution of activation energies, resulting from the plethora of defects present in amorphous oxides.

III. Validation against CVS and RVS

To validate the accuracy of the calibrated model beyond the measurement window, we performed standard eMSM (extended-measure-stress-measure method, here used as representative of CVS) [1] and RVS [8] sequences. The model previously calibrated only with ACE data is shown to accurately reproduce these different, more conventional stress sequences (Fig. 4, 5). To illustrate the superior defect characterization efficiency of the ACE sequence, Fig. 6 depicts the normalized fraction of defects that changes occupancy during three test sequences (ACE, eMSM and RVS), categorized according to their electrostatic impact on V_{th}: the ACE test induces clearly more defects to charge and discharge due to both the gradually increasing V_G across subsequent test

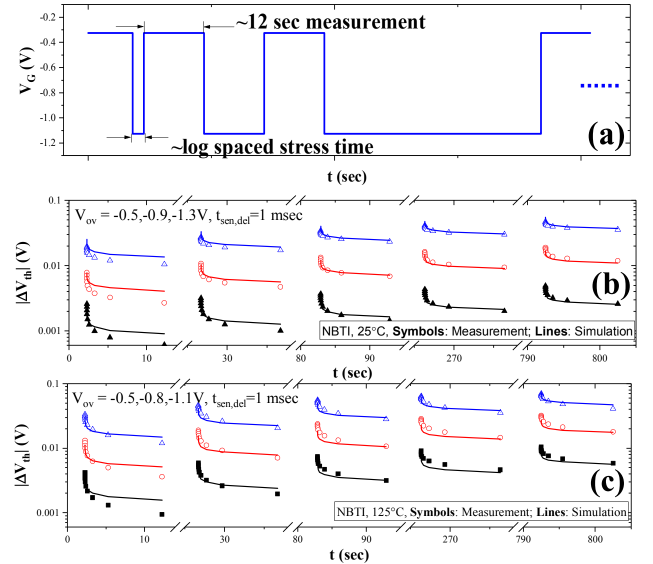


Fig. 4: Standard eMSM (CVS) sequence [1] was performed at six overdrive voltages (V_{ov}) and two temperatures. The previously calibrated defect bands in Comphy (ACE, Fig. 3) accurately reproduce the measured ΔV_{th} traces [(b), (c)].

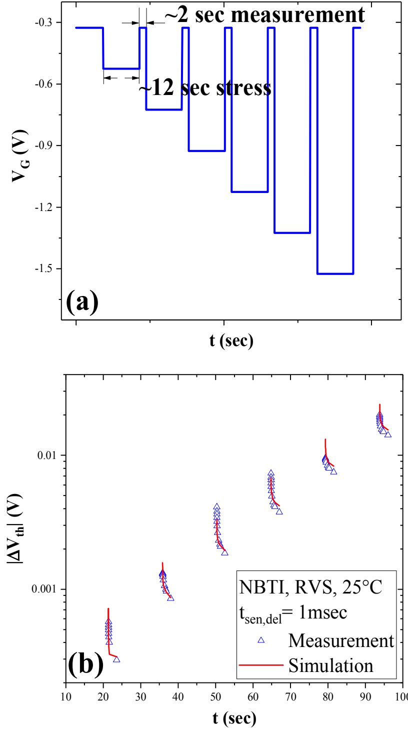


Fig. 5: An RVS measurement used for testing the calibrated model: as in Fig. 4 for CVS, the calculations of the calibrated model match also the measured RVS data.

units and the V_G down-ramping within each test unit [cf. Fig. 3 (a)]. Fig. 7 (a) summarizes the number of individual defects charging and discharging as a result of the stimuli induced by the three different test sequences: the ACE results in a clearly larger number of "active defects". Furthermore, the recursive single unit of the ACE test sequence [Fig. 3 (a), dashed-lined box] boosts the cumulative counts of trapping and de-trapping events [Fig. 7 (b)]. This repeated observations, further enhance the physics-relevant insight, given that the charge exchange is a stochastic process with transition time exponentially

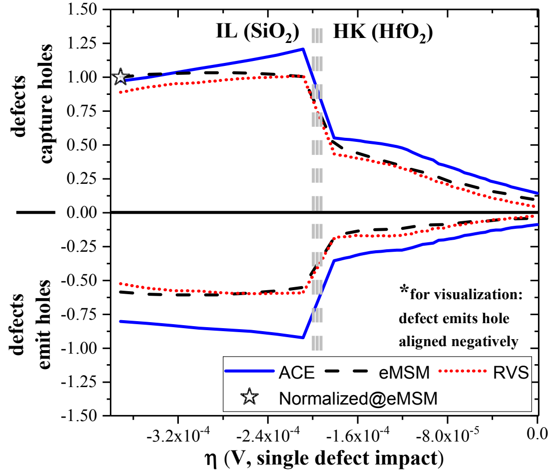


Fig. 6: Normalized numbers of defects that charge and discharge during each test, plotted with respect to their electrostatic impact on V_{th}. The ACE (25°C) results in a larger number of active defects in both HK and IL compared to eMSM (25°C, V_{ov}=-1.3V), RVS (25°C).

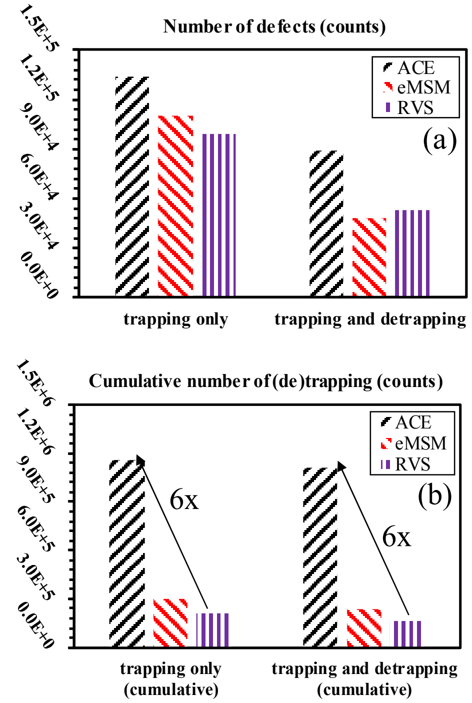


Fig. 7: (a) Total numbers of defects that charge or/and discharge during three different test sequences, integrated over the oxide depth (cf. Fig. 6). (b) Cumulative number of charge transitions (e.g. each defect can trap or/and emit a charge multiple times during the test). The ACE clearly induces more defect activity.

distributed around the defect characteristic time dictated by the activation energy of the process [2].

IV. Comparison and Discussion

The excellent agreement between the model projections and the various experimental data discussed so far, suggests that the calibrated defect band model constitutes an accurate representation of the oxide defects in the pMOS technology used here. We now proceed to evaluate quantitatively what fraction of the total defects, assumed to exist in this dielectric stack, is probed by these different test sequences. As shown in Fig. 8, we consider the standard eMSM protocol with 5 stress voltages (0.2V V_{ov}-step) at 2 temperatures. It is necessary to mention here that for the test performed at 125°C, the maximum V_{ov} is 0.2V lower than at lower temperatures, to avoid triggering other degradation mechanisms (i.e. TDDB, note: the gate leakage current is also measured during the test for reference, in order to be able to exclude the final portion of the collected data in the event of a soft-breakdown–not shown here). We use the sequence in Fig. 3 at three temperatures for the ACE test. Notice that the single-unit based voltage up-ramping of ACE test allow to conveniently trim the data without the need of choosing a suitable max V_G beforehand.

As already discussed, Comphy exploits the 2-state NMP theory as the core model for single defect occupancy. In order to connect individual defect responses to their collective behavior (i.e., in large area devices), two independent Gaussian distributions (for E_t and S, in grid mode), together with the corresponding device electrostatics, are used (cf. Fig. 1). Therefore, the Comphy framework allows to capture individual

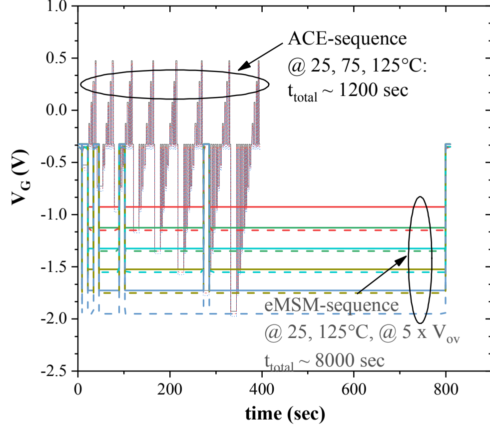
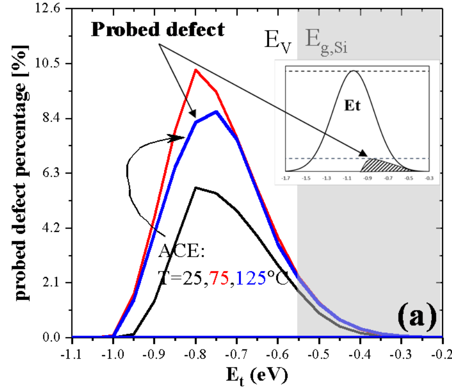


Fig. 8: A commonly used NBTI eMSM test matrix (5x stress voltages, 2x stress temperatures) compared to ACE sequence. Note the different test durations and voltage coverage.



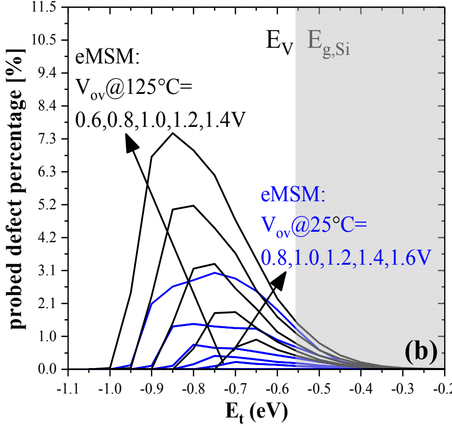
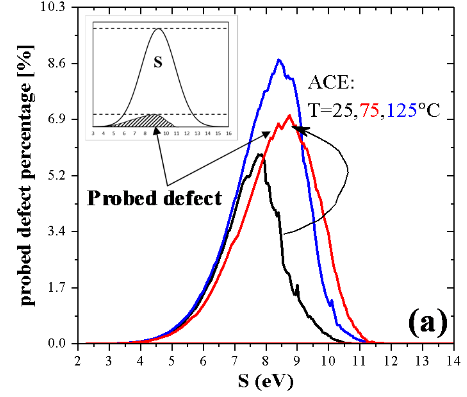


Fig. 9: Fraction of HK defects probed by the (a) ACE and (b) eMSM, as a function of defect energy level (E_t). ACE shows improved characterization efficiency compared to eMSM. Note: these values are proportional to the max V_{ov}, which is limited to avoid triggering other degradation mechanisms [e.g. the reduced peak at 125°C compared to 75°C in (a) is related to a truncated max V_{ov}, same in Fig. 10 (a)]. The inset sketches the probed defect with respect to the entire modeled defect bands. The mean value of modeled defect band (Gaussian distribution) lies beyond the probed defects range, which is typical for a reliable gate stack with low V_{th} degradation [11], not showing any saturation of the degradation kinetics within the measurement time range.

defect responses and represent them in a statistical way. Fig. 9 shows the fraction of probed HK defects as a function of the defect energy level E_t, which is primarily sensitive to the applied V_{ov} range. Similarly, Fig. 10 shows the fraction of probed defects as a function of the defect relaxation energy S, which is sensitive to the stress duration and measurement temperature. In both plots, it is evident that the ACE probes a larger percentage of defects. The "self-evaluation" flow demonstrated here (i.e., taking note of the fraction of the modeled defects, actually probed by the test used for the model calibration itself), can serve as a general evaluation metrics of efficiency for any test sequence.



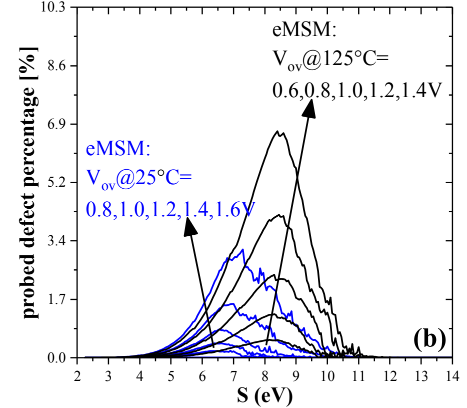


Fig. 10: Similar to Fig. 9, fraction of probed HK defects as a function of the relaxation energy S (note: the activation energies for the capture and emission processes ε_{12} and ε_{21}, are derived from the S and R parameters, see Fig. 1 and Table II) confirming the superior characterization efficiency of (a) ACE over (b) eMSM.

As depicted in the insets of Fig. 9 (a) and Fig. 10 (a), the overall probed defects only represent ~10% of totally modeled ones. The magnitude of such fraction is mainly limited by the stress voltage range, test duration and measurement temperature range, irrespective of the particular test sequence considered. However, it is worth noting also that a relatively low fraction of probed defects can be considered as a characteristic of all well-behaved gate stacks in general, for which a sufficient BTI reliability is the consequence of the limited fraction of accessible oxide defects [11].

V. VALIDATION AGAINST AC STRESS DATA

So far, only pMOS devices were considered in the analysis. The model calibration flow based on the ACE sequence was also performed for the nMOS device on the same HKMG Gate-First technology. The calibrated nMOS defect band parameters are also summarized in Table I and II. To further validate the

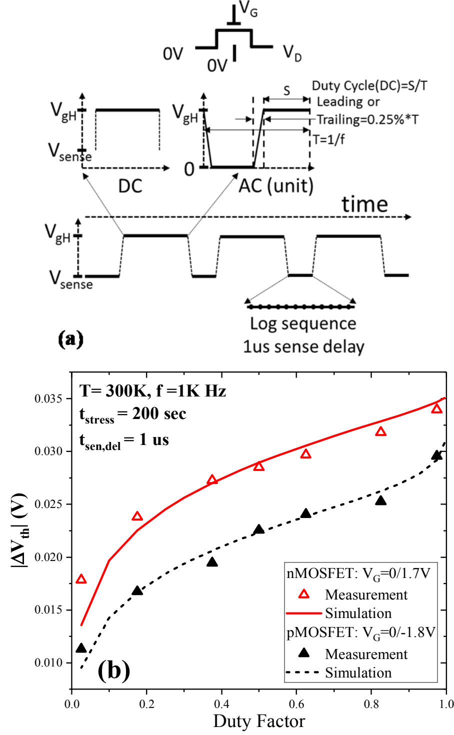


Fig. 11: (a) Ultra-fast setup is used for both AC and DC tests with *1μs* sense delay (Keysight B1530); the timing of the system was optimized to maintain signal integrity; (b) AC-eMSM with different duty factors were measured for both n/p MOS to further consolidate the accuracy of the model calibrated with ACE: the measured ΔV_{th} is accurately reproduced across the whole range of duty factors. No virtual third state (available as an option in Comphy to better reproduce the AC behavior of switching traps, as understood from the 4-state NMP model) was used for these AC projections [6,13] (also in Fig. 12), inducing some marginal mismatch between the measurement data and the simulations.

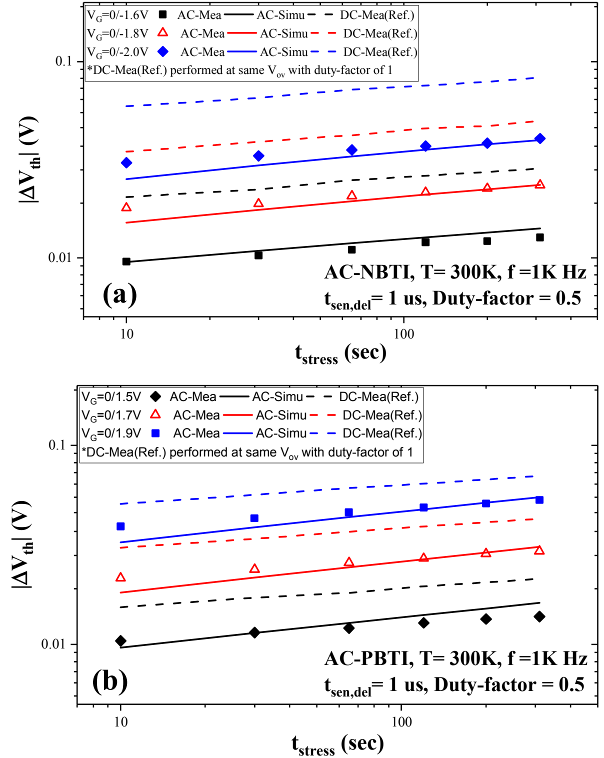


Fig. 12: (a) AC-eMSM experiment performed on the pMOS device. The measurement results (symbols) are reproduced sufficiently well by the defect bands calibrated previously with ACE (solid lines). The dashed lines are the DC stress reference measurement. (b) The same calibration procedure based on the ACE pattern (Fig. 3) was implemented for the nMOS on the same HKMG wafer: a similar good prediction of the AC behavior validates the approach also for PBTI.

accuracy of the complete model under circuit operation conditions, we performed AC stresses using a Waveform Generator/Fast Measurement Unit (WGFMU, Keysight B1530) with a sense delay of *~1μs* [Fig. 11 (a)]. The model *previously calibrated only with ACE data* reproduces the typical "S" shaped duty-factor dependence [Fig. 11 (b)] and the reduced degradation in AC stress compared to DC stress (Fig. 12) [14].

Given the multiple experimental validations of the model calibrated with ACE sequence above, one can conclude that for the specific defect population present in the studied HKMG technology, the proposed ACE sequence constitutes a very effective probing strategy.

VI. Statistical Evaluatin of Model Calibration Efficiency

To further investigate the superior effectiveness of ACE in probing *any* arbitrary defects distribution, and therefore its capability to alleviate the parameters covariance issue when calibrating the multi-parameter model to *any* technology, we performed a statistical Monte Carlo exercise with the following flow:

1) Random values (seed) are generated for the 6 parameters describing a HK defect band for a technology;

2) Comphy is used for generating "artificial" datasets that one would measure with the eMSM test matrix (total test duration ~7k sec) or with the ACE sequence (~0.8k sec) on this fictious technology;

3) Comphy is used for calibrating a model from scratch to reproduce the "artificial" datasets, starting from fixed initial values and with a fixed number of optimizations (iterations of the numerical optimizer);

This flow is repeated for different random seeds and results are summarized in Fig. 13. As shown in Fig. 13 (a) (b), the ACE-based calibration statistically shows similar or smaller error on the calibration of the 6 parameters, despite its ~9x reduced total test time as compared to eMSM sequence. From an industrial perspective, the most important aspect to evaluate is the accuracy of the projected end-of-life ΔV_{th} at nominal operating conditions (e.g., 10 years, 125°C, V_{ov}=0.7V). We therefore compare this metric using three approaches:

a) Power-law extrapolation on the "artificial" eMSM data;

b) Comphy model calibrated on the "artificial" eMSM data;

c) Comphy model calibrated on the "artificial" ACE data;

The latter approach (c) statistically yields the smallest error on the end-of-life projection compared to the former two approaches [Fig. 13 (c)].

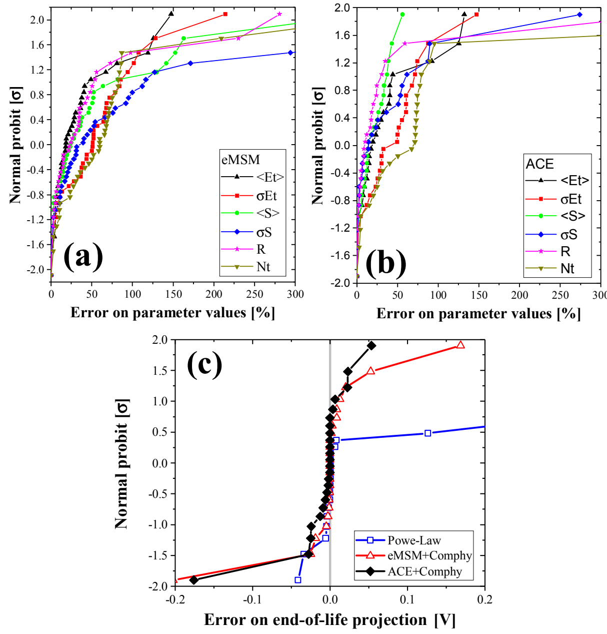


Fig. 13 (a) (b): Statistical Monte Carlo benchmarking of the (co-variance induced) error on model parameters as calibrated with eMSM (a) and ACE (b) sequences. Despite the 9x shorter total test duration, the ACE sequence shows slightly better parameter convergence after fixed number of optimizations. Fig. 13 (c): the Comphy models calibrated with "artificial" ACE data also statistically shows smaller errors on end-of-life ΔV_{th} projection.

VII. Conclusion

We have demonstrated a new efficient BTI test pattern based on voltage and temperature acceleration of charge trapping and de-trapping. The new "accelerated capture and emission" (ACE) test was systematically evaluated using the imec/T.U. Vienna BTI modeling framework "Comphy" and it was shown to offer superior test throughput, defect characterization efficiency and projection accuracy as compared to more conventional CVS and RVS methods. In particular, the new pattern was shown to be very effective for the calibration of NMP model parameters, overcoming the intrinsic parameter covariance issue. Comphy models calibrated with the ACE pattern on different device technologies have been shown elsewhere to yield more accurate life-time projection in novel junction-less devices [15] and to serve as powerful pathfinding tool for dipole-based gate stack design [16].

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