A method for simulating the influence of grain boundaries and material interfaces on electromigration

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ABSTRACT

Continued scaling of the back-end-of-line copper metalization has shown to significantly increase the resistivity and decrease the lifetime of interconnects. The primary reason is the impact of microstructure, meaning the influence of grain boundaries and material interfaces on the movement of conducting electrons and atoms during electromigration. Modeling this phenomenon is especially challenging since the boundaries and interfaces must be treated independently from the grain bulk. Usually, this results in an extremely fine mesh with very high computational and memory requirements. In this manuscript, we present an efficient approach to treat grain boundaries and material interfaces when modeling electromigration in copper nano-interconnects. Our approach uses several spatial material parameters to identify the locations of the grain boundaries and material interfaces during a simulation, thereby not requiring the definition of multiple materials or complex meshes and geometrical interfaces. Using this method even very coarse meshes, with grid spacings twice the size of the thinnest element (the grain boundary thickness), were able to reasonably reproduce the vacancy concentration of thin copper interconnects, including their microstructure. Furthermore, we were able to calculate the stress build-up at triple points with high accuracy even when using a very coarse mesh.

1. Introduction

The continued trend in transistor scaling according to Moore's Law must be supported by a simultaneous scaling of the interconnect lines. While a variety of materials and structures are being investigated to further shrink transistor dimensions, the passive components, such as metal interconnects, are starting to become a bottleneck in circuit performance. Mitigating the impact of size effects in interconnect structures is essential for scaling to continue. These effects include line and via sidewall roughness, the intersection of porous low-κ voids with the sidewall, copper (Cu) surface and copper/barrier interface roughness, and the presence of grain boundaries (GBs) [1]. The most commonly used metal, copper, is showing undesirable behavior in the nanoscale, including increased resistivity due to grain boundary and surface roughness scattering, as well as heightened electromigration (EM) effects. These effects result in undesired performance limitations and even limitations in the device lifetime. Regardless, it is expected that copper will continue to be used in some form for the next several technology nodes and will remain the preferred solution for the interconnect metal until at least 2021 [1].

When the thickness of a copper line is reduced, the average crystal grain size decreases almost linearly, as characterized by Sun et al. [2] and shown in Fig. 1 for a wide range of processing conditions. This decrease in grain size and the overall reduction in the metal thickness means that grain boundaries and material interfaces (MIs) play an increasingly important role in the conductive behavior of metals. The influence of these properties on electron scattering has been explored most notably by Fuchs [3], Mayadas and Schatzkes [4], and Sondheimer [5]. Along with the changes in the conductive behavior of copper nano-interconnects, the reliability of the metal lines is significantly influenced by their granular microstructure. Electromigration is the major reliability concern in the metal interconnects, present in modern integrated circuits. EM degradation results in chip failure due to the nucleation and subsequent growth of a void, which ultimately leads to an increasing line resistance and an open circuit failure [6].

Many attempts are underway to replace copper interconnects, including the local interconnect middle-of-line, the M1 level, and tight-pitch level metalizations with EM-resistant alternatives, such as cobalt and carbon nanotubes [7,8]. However, due to the planned continued use of copper nano-interconnects for advanced nodes up to 7 nm [9], it must be ensured that EM is properly modeled and that nano-interconnect lifetimes can be appropriately estimated. The critical metal interconnect layers are shown in Fig. 2. These layers are the closest to the front end of line (FEOL) devices, while the higher metal interconnects generally have a larger cross sectional area and lower current density [10].
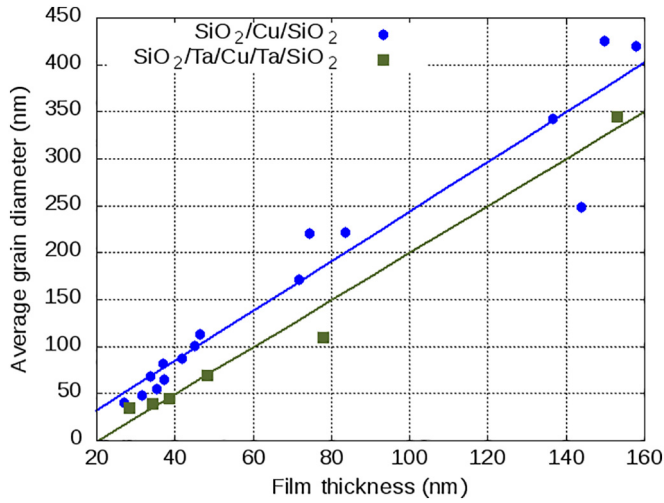
Fig. 1. Relationship between the film thickness and grain diameter using values obtained from [2]. The symbols are the measurements, while the lines are best-fit linear regressions. As the film thickness is decreased, the average grain size decreases, meaning that more grain boundaries are present.
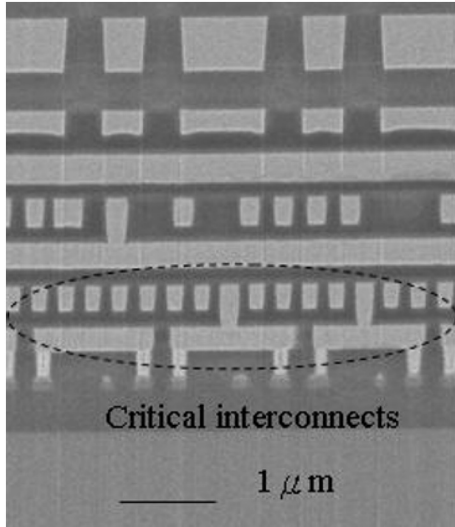

Fig. 2. TEM view of the multilayer copper interconnect scheme, with the electromigration-critical layers circled. Reprinted by permission from Springer Nature: Springer, Integrated process feasibility of hard-mask for tight pitch interconnects fabrication, Chun-Jen Weng, 2011 [10].

In this manuscript, a method to accelerate electromigration simulations of grained copper interconnect lines is presented. In order to attribute the effects of granularity on the electromigration reliability of an interconnect structure, most studies apply an effective diffusivity (D_{eff}) parameter, which is a combination of the bulk (D_B) and grain boundary (D_{GB}) diffusivities [11–13] to continuum or bulk simulations. This parameter is calculated using

$$D_{eff} = D_B + \frac{t_{GB}}{D} D_{GB}, \tag{1}$$

where t_{GB} refers to the thickness of the grain boundary migration channel and D is the mean grain size.

As an alternative to this approach, simulations have been performed by explicitly defining all grains and meshing the full structure [13–15]; such an approach requires very fine meshes, especially to properly define grain boundaries and points where the grain boundary and material interface meet. This method has been used to model small sections of an interconnect line with few grains, as described in the work of Sukharev et al. [14]. The authors used a finite element tool to mesh the structure, including a defined grain boundary and material interface thickness. The high aspect ratio between the interconnect size and boundary thicknesses results in a very dense mesh and a limitation in the size of interconnect which can be modeled.

2. Copper interconnect

The behavior of copper at the nanoscale is very different from that observed in thick films, especially, when considering its resistivity and predisposition to electromigration failure. Experiments have shown that the lifetime of copper interconnects has approximately halved at every new technology node, even at the same current density [16]. An increasing influence of grain boundaries and material interfaces has been shown to be the core reason for the increase in EM effects [12,17] in copper. If one only considers these influences on the copper resistivity, a drastic change in the interconnect behavior can be observed. It should also be noted that the sheer fact that the interconnect has less volume also contributes to an increasing speed with which electromigration phenomena can influence a failure. A smaller void is thereby sufficient to cause a failure. The presence of microstructure serves to exacerbate the effect.

The continued scaling has also resulted in a significant increase in the current density, required to flow through the metal interconnect, which is expected to continue at least until 2026 [9]. As shown in Fig. 3, the operational current density, provided by the International Technology Roadmap for Semiconductors (ITRS), is represented with blue dots, while the maximum allowed DC current density for device performance (J_{max}) is also given, along with the maximum current density allowed before electromigration failure (J_{EM}). The two factors of increasing resistivity and reduced sizes work together to limit the maximum current densities and accelerate the failure time of nano-scaled copper interconnects. This causes the maximum and electromigration current densities to reduce, while the operational current density must be increased. It is quite evident that the desired operational current density has already surpassed the maximum recommended current density so finding new materials soon is of critical importance.

In this section, the influence of continuously shrinking copper lines and granular microstructure on the conductivity and electromigration phenomena in copper interconnects is described.
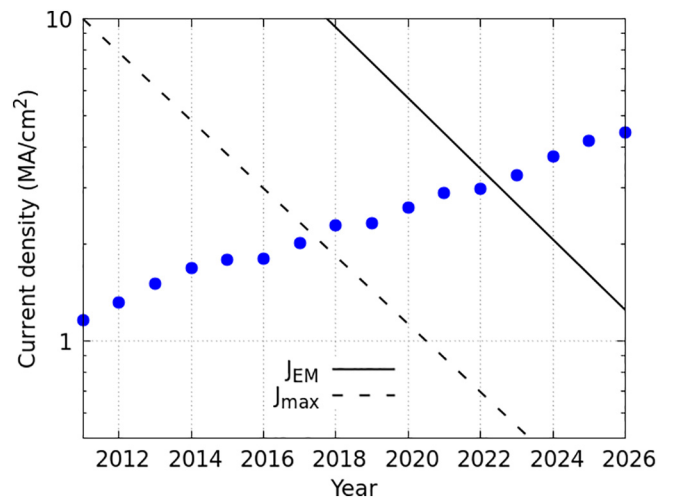

Fig. 3. The evolution of the maximum allowed DC current density J_{max} and electromigration failure inducing current density J_{EM}, according to the ITRS [9]. The blue dots show the operational current density as recommended by the ITRS. Similar data has been reported by researchers in [18,19]. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)
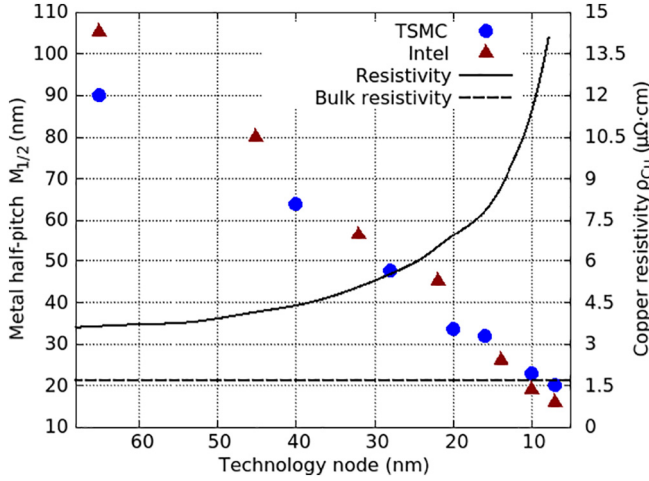
Fig. 4. Effective Cu interconnect resistivity and expected resistivity at future nodes as a function of the technology node obtained from [22]. The increasing resistivity from the bulk value of 1.68 μΩ·cm is dueto the increased influence of GB and MI scattering. In addition, the metal half-pitch for the technology nodes from TSMC (●) and Intel (▲) are shown.

2.1. Conductivity

When considering the resistivity or conductivity of a nano-sized metal line, three main components must be included:

1) Intrinsic resistivity of the bulk material, limited only by the electron mean-free-path (MFP).
2) The increase in resistivity due to surface scattering including material interfaces.
3) The increase in resistivity due to grain boundary scattering.

The resistivity has steadily increased with the introduction of new technology nodes as depicted in Fig. 4. There, the relationship between the technology nodes and interconnect half-pitch from major industrial manufacturers is also shown. The same technology node can relate to a different copper line thickness, depending on manufacturer [9]. For example, at the 7 nm technology node, the Taiwan Semiconductor Manufacturing Corporation (TSMC) and Intel are planning to have a minimum copper half-pitch of 20 nm and 16 nm, respectively. At these thicknesses, the copper resistivity is expected to be about 15 μΩ·cm, an increase by nine times from the bulk value of 1.68 μΩ·cm. The connection between the metal line width (half-pitch) and increasing resistivity is very evident in Fig. 4. In order to include the influence of grain boundaries and material interfaces on the copper resistivity, several models have been proposed over the years [3–5,20,21].

The effects of the granular microstructure, surface scattering on boundaries and interfaces, and cross-sectional area of a copper interconnect on its resistivity ρ_f is commonly modeled by applying a continuum equation derived by Clarke et al. and based on the works of Fuchs, Mayadas, and Shatzkes [20].

$$\frac{\rho_f}{\rho_i} = 1 + \frac{3\lambda}{4w}(1-p) + \frac{3\lambda}{2D}\left(\frac{R}{1-R}\right),$$ (2)

where ρ_i is the bulk resistivity, λ is the electron MFP, w is the metal width, p is the probability of electron scattering from a material interface, D is the average grain diameter, and R is the probability of electron scattering from a GB. The added temperature influence on the final resistivity ρ is calculated using

$$\frac{\rho}{\rho_f} = 1 + \alpha_e(T - T_{ref}),$$ (3)

where T is the temperature, T_{ref} is the reference (room) temperature,

and $\alpha_e = 0.0043 K^{-1}$ is the temperature-dependent factor for Cu resistivity also referred to as the temperature coefficient of resistance (TCR). Several studies suggest that the TCR value varies according to the microstructure in several metals when looking at the difference between nanosized and microsized grains [23,24]. However, this was shown not to be the case for nanosized copper where the grain size varied between 20 nm and 120 nm [25], a range of interest for the study presented in this manuscript, and in copper lines from different data sets [26]: The TCR value remained unchanged at about $0.004 K^{-1}$.

Monte Carlo methods have also been used to better define the influence of MI and GB scattering on copper resistivity [21]. Most simulations dealing with the conductivity and reliability of copper interconnects use Eq. (2). However, this approach provides a new bulk value for the microstructure-dependent resistivity, while the effects of an individual grain boundary cannot be analyzed. For this, we need to make sure the entire line, with its microstructure, is represented in an appropriate technology computer aided design (TCAD) environment. This can be done by observing that the proximity to grain boundaries and material interfaces, which play a major role in reducing the local conductivity, can be treated as a parameter which influences conductivity. Therefore, finding the local conductivity based on the distance of each point inside the grain to a GB or MI can help create a spatial representation of the resistivity or conductivity inside a copper line.

Once the distance to the boundaries d_b from every point inside the individual metal grains is known, the GB- and MI-dependent local resistivities ρ_l inside the Cu line can be derived from the intrinsic resistivity ρ_i using

$$\rho_l = \rho_i\left(1 + \frac{3\lambda}{8 d_b}\right).$$ (4)

Conductivity is one of the primary properties which influences the electromigration behavior of copper. A high current density and a high electron wind commonly lead to the diffusion of metal atoms in the direction of electron motion. The diffusion is governed by the atom diffusivity property of the material, which also varies depending on whether the atom is located in the grain, the grain boundary, or along the interface between the metal and adjacent material. Because atoms are more strongly bound inside the grain lattice than at the grain boundaries, it is expected that their migration is more likely to take place along the boundary, meaning that their diffusivity there is increased. Previous attempts to introduce microstructure in electromigration simulations are based on the review of Sukharev et al., [27] and nevertheless relied on a bulk value for the copper conductivity, resulting in inherent inaccuracies when modeling the microstructure.

2.2. Electromigration

2.2.1. Physics of electromigration

The physics of electromigration is described in detail in the work of Ceric and Selberherr [19]. Essentially there are two driving forces for electromigration: The *direct force*, arising from the direct action of the external field on the charge of the migrating ion and the *wind force*, arising due to the scattering of the conduction electrons by the impurity or point defect under consideration:

$$\vec{F} = \vec{F}_{direct} + \vec{F}_{wind} = (Z_{direct} + Z_{wind})e\,\vec{E} = Z^*\,e\,\vec{E}$$ (5)

Here, the Z^* is the effective valence of the defect and is a sum of the direct (Z_{direct}) and wind (Z_{wind}) valences, e is the elementary charge, and $\vec{E}$ is the applied electric field. In free-electron-like metals, such as copper, the wind-force contribution is expected to be dominant. The value for the effective valence of copper was calculated to be about -5 [28], which has been confirmed successfully in many subsequent studies on copper electromigration, both through measurements and modeling [29].

In order to experimentally determine electromigration effects on a new interconnect technology, measuring the failure behavior of all materials which make up the interconnect is necessary. This is becoming an increasingly difficult task, since advanced technology nodes rely on the implementation of several different materials and very small sizes. Usually, experiments are performed in accelerated conditions, meaning that failure times are less than about 1000 h. According to Black's equation [30], the end of life can be accelerated by increasing the current density or by increasing temperature. The expected lifetime in terms of the mean time to failure (MTTF) in real world conditions can therefore be extracted using a lognormal failure plot, which follows Black's equation

$$MTTF = \frac{A}{j^n} \exp\left(\frac{E_t}{k_B\,T}\right),$$ (6)

where n and E_t are the density exponent and activation energy, respectively, which are determined by experiment; A is a constant determined by the material properties and geometry of the interconnect, j is the current density, and k_B is Boltzmann's constant. It should be noted that simulations, just like measurements, are carried out using the same accelerated conditions in order to as closely as possible match the experimental conditions.

2.2.2. Influence of microstructure

Current state-of-the-art models and simulators of interconnect electromigration reliability cannot appropriately take into consideration the complex metallic microstructure and are therefore not able to address EM interconnect failure at advanced nodes. In addition to their influence on conductivity, grain boundaries and material interfaces act as fast diffusivity pathways for vacancies as well as locations of vacancy generation and annihilation [31]. Previous attempts to include the influence of the microstructure in EM simulations relied on introducing GBs as a thin layer, requiring a very fine mesh, thereby needing significant computational and memory costs to perform a single simulation. This limits the simulation to two dimensions and forces using very small sections of an interconnect, thereby restricting the geometry to simple grain structures [32]. In this work a novel EM modeling framework, which treats boundaries and interfaces as a material parameter is presented. The inclusion of the microstructure allows to properly treat the influence of local parameters including resistivity, vacancy diffusivity, vacancy diffusion activation energy, and effective valence. This method allows modeling the EM behavior for realistic nanoscaled Cu interconnect lines.

Recently, we have included the microstructure of copper interconnects in electromigration simulations by including grain boundaries and material interfaces as spatial parameters using the distance from a GB or MI as a material parameter [33]. This distance parameter was then used to determine the local electrical conductivity $\sigma_l = 1/\rho_l$ of the copper line as well as the essential variables of the vacancy diffusion coefficient including the pre-exponential factor for vacancy diffusion D_{v0} and the activation energy E_a given by

$$D_v = D_{v0}\,\exp\left(-\frac{E_a}{k_B\,T}\right),$$ (7)

The pre-exponential factor for vacancy diffusion D_{v0} and the activation energy for diffusion E_a vary between the crystalline grain, GB, and MI according to Table 1 [6,31]. Assuming a grain boundary

Table 1
Microstructure-dependent material parameters for the vacancy dynamics model from [6,31].

Vacancy diffusion parameter	Grain	GB	MI
Pre-exponential factor (D_{v0}) s^{-1}	0.52	52	520
Activation energy (E_a)	0.89	0.7	0.5

thickness of t_{GB}, the distance parameter was used in order to assign localized spatial parameters for D_{v0} and E_a. In the work presented in [33], when the distance to a GB or MI d_b was less thanone half t_{GB}, the GB parameters from Table 1 were applied. Otherwise, bulk grain parameters of 0.52 cm^2/s and 0.89 eV were applied for D_{v0} and E_a, respectively. The main drawback in the method presented in [33] is that the GB and MI were not differentiated and were treated as influencing electromigration and conductivity in the same way with a single set of material parameters. Although improving on a general continuum copper approach, this method leads to potential errors in the simulations.

In addition, the method presented previously diminishes the effective influence of the MI in the model since the E_a and D_{v0} values inside grain boundaries and material interfaces were assigned according to the distance from an edge being less than one half of the effective boundary thickness. The GB is characterized as the distance from the grain boundary in both directions - or both grains which share the boundary - while the MI only has one relevant direction - into the copper grain - resulting in its effective thickness being one half that of the GB thickness.

The above-described method [33] was updated to separate the influence of the parameters assigned to the grain boundaries to those for the material interfaces [34]. A framework is presented for which every discretized point in the interconnect volume is assigned a value depending on the following rules:

1) If the point is within 0.5·t_{GB} to a material interface, assign material interface parameters.
2) If 1) is not true and the point is within 0.5·t_{GB} to a grain boundary, assign grain boundary parameters.
3) If 1) and 2) are not true, assign bulk parameters.

In this manuscript, we build on the frameworks presented in [33,34] and introduce grain boundary orientation to the model. By doing this, we can properly treat the diffusion blocking of some bamboo-like grain boundaries, while allowing for grain boundaries, which are oriented in the direction of the electron wind, to accelerate the electromigration phenomena. For this, we modify the simulation framework as described in the following section.

3. Modeling framework

In the modeling framework described here the grain bulk, grain boundaries, and material interfaces are differentiated using spatial material parameters instead of explicitly defining different materials, which potentially requires complex meshes. It builds on the frameworks previously presented in [33,34] and advances the state-of-the-art by introducing grain directionality within the model. The proposed flow in the framework requires the interconnection between a variety of tools, including a tessellation software and an electromigration simulator, which is based on the finite element method (FEM). There are three primary steps to the framework, as visualized in Fig. 5:

1) Grain tessellation: The open-source software Neper [35] is used to generate the crystalline copper geometry. This step needs to have the desired interconnect geometry and average grain diameter as inputs.
2) Spatial parameter assignment: The microstructured geometry is imported into an in-house tool, where a Cartesian grid is generated. Each point on the grid is assigned several parameter values, including distance to the nearest boundary and atom diffusivity. The effective boundary thickness and desired grid resolution are passed as parameters.
3) Electromigration simulation: Finally, the spatial parameters are imported into a finite element simulator, where the electromigration model is implemented and simulations are performed. In this study,
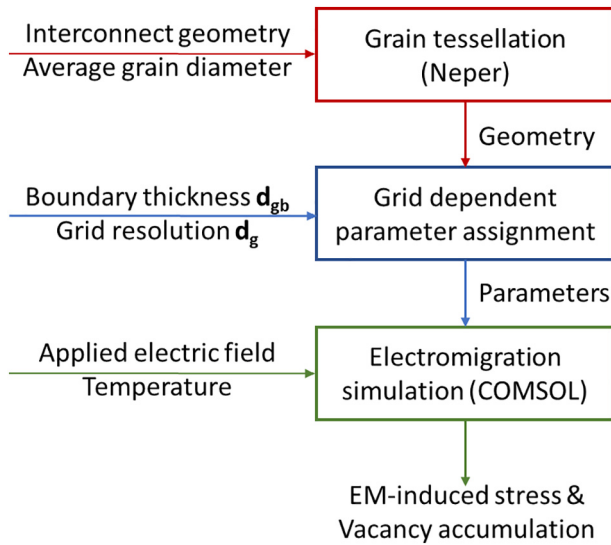
Fig. 5. Three phases of the implemented modeling framework to properly simulate electromigration in copper nano-interconnects, while taking grain boundaries and material interfaces into consideration.

Fig. 6. Vonoroi tessellation of two metal lines with a grain diameter of 50 nm and cross-sectional dimensions of (a) 200 nm × 200 nm and (b) 40 nm × 40 nm.

conclude that a reduction in the Cu dimensions, while keeping the grain size the same, leads to a bamboo grain microstructure [21,38,39]. This means that the grain boundaries are primarily near-perpendicular to the direction of the applied electric field and the direction of the atom diffusion. Because of this, they simultaneously act as fast diffusivity pathways and diffusion barriers, depending on the grain boundary orientation.

3.1.1. Device under simulation

In this work, we test our model using a sample two-dimensional (2D) interconnect line with a cross-sectional area of 20 nm × 20 nm, a length of 2000 nm, and an average grain size of 25 nm, which fits well the grain sizes measured in [2]. As can be observed from Fig. 1 the linear nature of the grain diameter and film thickness relationship is only valid for films thicker than about 40 nm. In order to find the grain diameter at 20 nm, we extrapolated the first few points from the graph, noting an exponential regression, as shown in Fig. 7. Here, we clearly see that the average grain diameter for a 20 nm thick film is about 25 nm.

As discussed above, this combination of small interconnect dimensions and large grain size results in a bamboo-like grain structure, with a few sections where grains appear stacked on top of each other, as depicted in Fig. 8. From the top to the bottom of Fig. 8 we show the left, middle, and right sections of the granular copper geometry, respectively. The sections are intentionally chosen to show the general bamboo-like structure in addition to stacked grains in the middle section and a triangular grain in the far right section of the wire (figure

the EM model was implemented inside COMSOL Multiphysics [36], which was used to carry out the FEM simulations. The electro-thermo-mechanical problem is then initiated with an applied electric field and ambient temperature.

3.1. Grain tessellation

The stochastic polycrystalline structure of the metal line is generated using a Voronoi tessellation procedure, which is modeled based on the following: Assuming spherical grains and knowing the mean diameter of a grain, the volume of each grain is calculated. The volume to be filled by the grain pattern, which corresponds to the total volume of the interconnect line, is divided by this average grain volume to give the total expected number of grains. An actual number of grains is then picked randomly from a Poisson distribution with the mean equal to the expected number of grains. For each grain a seed point is placed at a random location within the interconnect volume to be filled by the grain pattern. A two- or three-dimensional Voronoi tessellation is generated based on the seed points by associating each node in the simulation mesh with the nearest seed point and thereby assigning it to the grain defined by that seed point. From those seed point locations circular (2D) or spherical (3D) growth is initiated, forming the grains. When circles/spheres hit each other, they merge to create a grain boundary. The orientation of the boundary depends on the pre-determined preferred orientation and can be adapted depending on the metal chosen to be studied. This proceeds until the entire interconnect volume is filled with grains. For our purposes, this process was performed using the Neper tessellation tool, developed at CNRS and MINES Saint-Etienne [35] and the generated granular microstructure was extracted for further simulations. The Neper tool allows for the generation of a Vonoroi tessellation with an ideal copper orientation of $(1\ 1\ 2)[1\ 1\ \bar{1}]$ and $(\bar{1}\ 1\ 2)[1\ \bar{1}\ 1]$ [37].

In order to show the key features of the tessellation tool used in this study, the above mentioned technique was applied to two different copper lines: One with dimensions of 200 nm × 200 nm and a second with dimensions of 40 nm × 40 nm. The average grain diameter was set to 50 nm. The results are shown in Fig. 6. In the larger wire shown in Fig. 6(a) we note a very granular structure. However, when the grain diameter is larger than the dimensions of the metal wire, a bamboo structure forms, depicted in Fig. 6(b). This is consistent with many studies that show that as a wire becomes more narrow the grains begin to be more bamboo-like and less granular [38,39]. Thereby, we
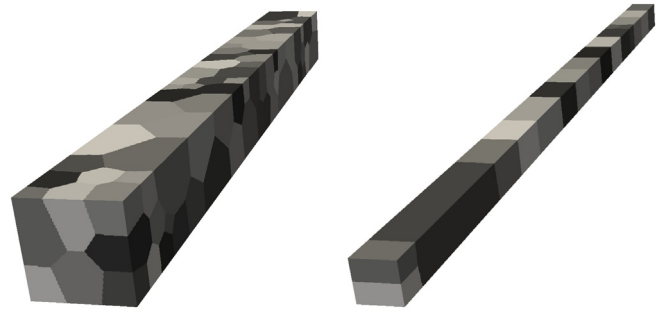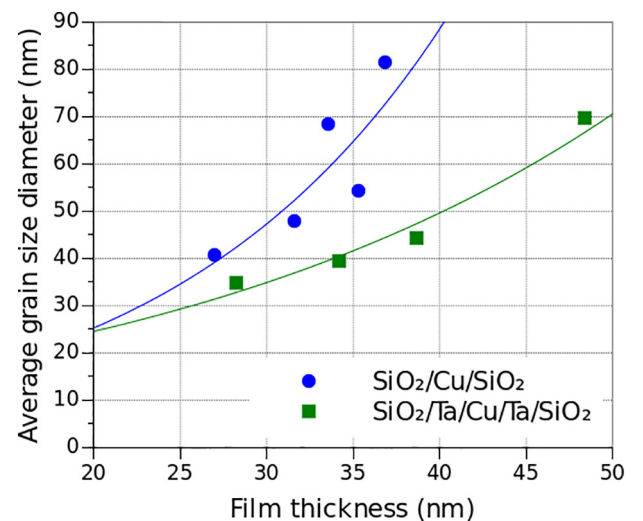

Fig. 7. Relationship between the film thickness and grain diameter using values obtained from [2]. The symbols are the measurements, while the lines are best-fit exponential regressions.
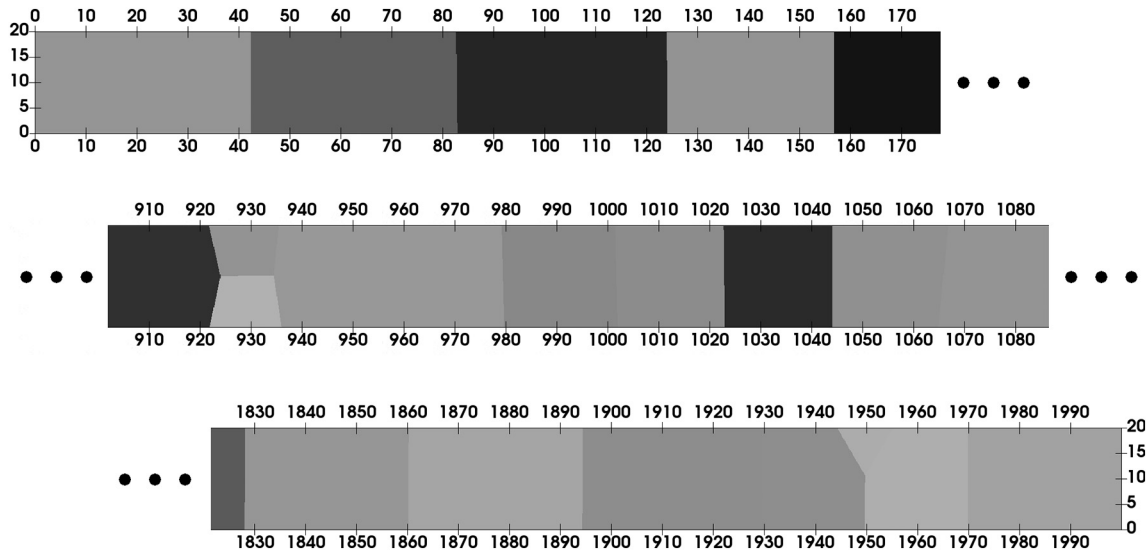
Fig. 8. Granular structure for the copper line used in this study with both axes in [nm]. (top) Left-most section of the line, with the columnar structure evident. (middle) Middle section where one sample of a stacked grain is evident. (bottom) Right-most section with more complex features.

bottom). This geometry is then imported into an in-house tool in order for the appropriate spatial material parameters to be assigned and overlayed on top of the generated microstructure.

3.2. Spatial parameter assignment

The spatial parameters, which are used to identify the location of the GB and MI are explicitly defined on all Cartesian mesh intersect points, while a linear interpolation is used to populate the entire material domain between the defined points. This proceeds according to the flowchart shown in Fig. 9. First, the microstructure is imported and a desired boundary thickness and grid resolution are assigned. GB and MI thicknesses of 1 nm were assumed for most of this study, because this value was found to be appropriate from previous publications [40]. The flowchart in Fig. 9 summarizes the implemented workflow. All grid points are iterated and material parameters are assigned for each grid point according to the following sequence:

1) Iterate through all grains until the grain which contains the current point is located.
2) Find the nearest edge which defines the grain and is closest to the given grid point. An edge can be a grain boundary or a material interface.
3) Find the distance from the nearest edge. This distance is one of the key parameters for the material conductivity.
4) Calculate the local conductivity using Eq. (4) and apply it to the grid point.
5) If the distance to the nearest edge is greater than the defined boundary thickness, bulk parameters for $D_{v0} = 0.52 cm^2/s$ and $E_a = 0.89 eV$ are assigned at that grid point.
6) If the distance to the nearest edge is smaller than the defined boundary thickness, then find out if the nearest edge E_k is a material interface.
7) If E_k is a material interface, assign MI properties for $D_{v0} = 520 cm^2/s$ and $E_a = 0.5 eV$ at that grid point.
8) If E_k is a grain boundary, find out the angle that the grain boundary makes with the direction of the electric field θ and apply the grain boundary properties of $D_{v0} = 52 cm^2/s \cdot \cos(\theta)$ and $E_a = 0.5 eV$ at that grid point.
9) If the last grid point has not been reached, move to the next grid point and begin again with step 1).

It should be noted that recently, copper interconnects are no longer surrounded by the same dielectric material on all sides, meaning that the diffusive properties at each material interface may differ, depending on which surface is observed; top, bottom, and sidewalls may have different properties [13,14,19,41,42]. If this is the case, Step 7, the assignment of MI properties, can be extended to assign parameters which depend on the dielectric material bounding each surface. This extension is quite trivial to implement and follows the flow of the proposed method in Fig. 9 by the addition of further test or question boxes to decide which MI interface parameters need to be assigned at which surface.

The results of the process from Fig. 9, when applied on a geometry with dimensions 20 nm × 2000 nm, with an average grain diameter of 25 nm, boundary thickness of 1 nm, and grid resolution of 0.5 nm are shown in Fig. 10. In Fig. 10(a) only the grid points are shown in relation to the microstructure. In Fig. 10(b), the distance to the nearest edge is plotted. This value is used to calculate the local conductivities inside the thin film. Fig. 10(c) and Fig. 10(d) depict the assignment of the grid points for the pre-exponential factor D_{v0} and activation energy E_a, respectively, from Eq. (7), as given in Table 1.

3.3. Electromigration model

The EM model requires the simultaneous solution of three physical phenomena including calculating the current density, temperature and self heating for the electro-thermal problem, vacancy, atom, and ion dynamics through the interconnect, and solid mechanics to calculate the strain induced by the vacancy transport. Ultimately, the EM-induced stress is calculated, as shown in Fig. 11. The stress threshold refers to the stress level which will either cause a crack in the metal line or will result in void nucleation. The nucleated void then continues to grow, ultimately leading to an open circuit failure.

3.3.1. Electro-thermal problem

By applying the microstructure-dependent resistivity given by Clarke et al. [20], an expression for the resistivity with respect to the distance to the nearest boundary λ has been derived in Eq. (4). By applying this equation and the spatial parameter for the distance from a boundary from Fig. 10(b) a spatial parameter for the localized resistivity or conductivity of a copper line at each point in the line is generated, instead of using a single continuum value. It was found that an electron mean free path value of $\lambda = 4$ nm and a bulk resistivity of

Geometry
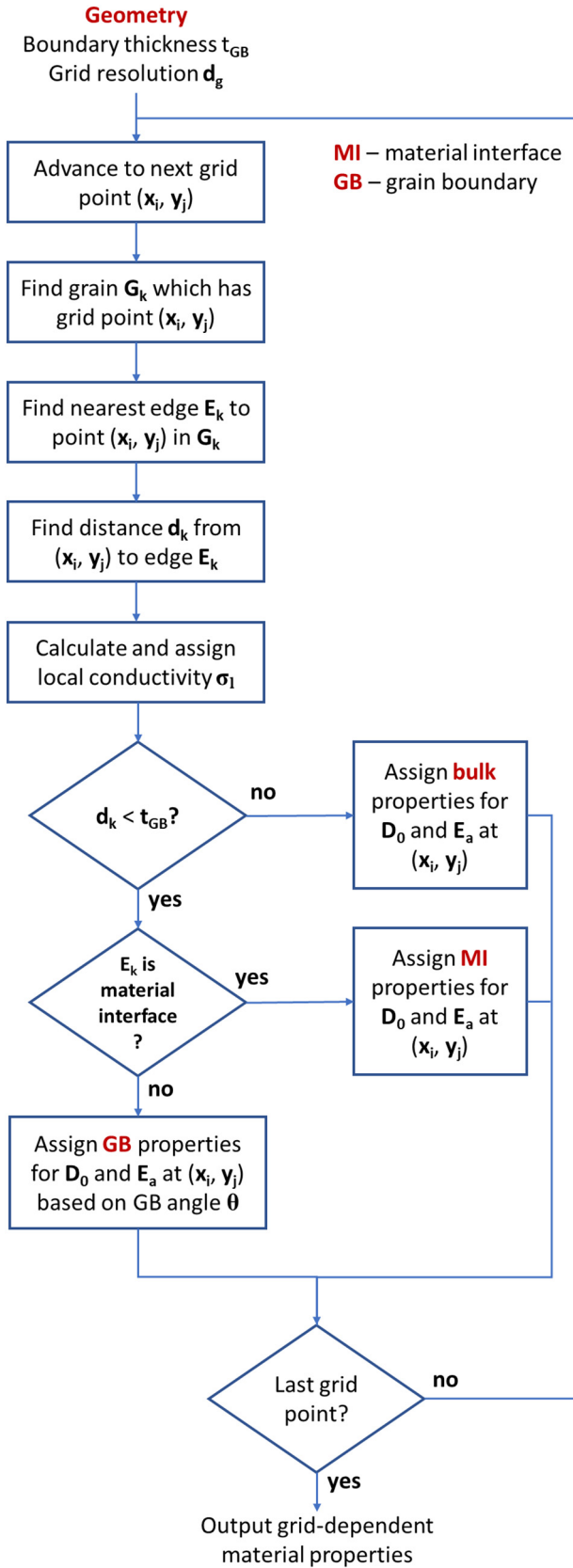Boundary thickness t_{GB}
Grid resolution d_g

Advance to next grid
point (x_i, y_j)

MI – material interface
GB – grain boundary

Find grain G_k which has
grid point (x_i, y_j)

Find nearest edge E_k to
point (x_i, y_j) in G_k

Find distance d_k from
(x_i, y_j) to edge E_k

Calculate and assign
local conductivity σ_l

$d_k < t_{GB}$? —no→ Assign **bulk**
properties for
D_0 and E_a at
(x_i, y_j)

yes

E_k is
material
interface
? —yes→ Assign **MI**
properties for
D_0 and E_a at
(x_i, y_j)

no

Assign **GB** properties
for D_0 and E_a at (x_i, y_j)
based on GB angle θ

Last grid
point? —no→

yes

Output grid-dependent
material properties

Fig. 9. Flow chart for the process of assigning the necessary material parameters to each grid point in the simulation space.

$1.68 \times 10^{-8}\, \Omega \cdot$m proved to be optimal in order to match the experimental results shown in Fig. 1.

After the distances have been converted to local conductivities for each grid point, linear interpolation is applied to generate the conductivity at all locations in the interconnect, as shown in Fig. 12(a). The temperature influence on the spatial resistivity parameter was calculated using Eq. (3) where ρ_l should be substituted instead of ρ_f, with the result depicted in Fig. 12(b). It is clear that the boundaries have a much smaller conductivity than the grain bulk. In addition, small grains experience a reduced conductivity when compared to larger grains. This is expected, since there will be less boundary scattering events in larger grains.

The primary goal of the electrothermal problem is to describe the temperature distribution in the interconnect and surrounding passivation layers. Joule heating must be considered, since this can lead to high thermal gradients in the interconnect and an increased proclivity to electromigration failure. The system of equations which must be solved is given by [6]:

$$\nabla \cdot (\gamma_T \nabla T) = c_p\, \rho_m \frac{\partial T}{\partial t} - p_d \tag{8}$$

$$p_d = \gamma_E\, \|\overrightarrow{\nabla j}\|^2 \tag{9}$$

$$\nabla \cdot (\gamma_E \overrightarrow{\nabla j}) = 0 \tag{10}$$

In the above equations, γ_T is the material specific thermal conductivity, T is the temperature, γ_E is the electrical conductivity, $\overrightarrow{j}$ is the current density, c_p is the specific heat, ρ_m is the mass density, and p_d is the electrical power loss density.

Due to the high thermal conductivity of copper and the high ambient temperatures applied during electromigration characterization and simulation, it is frequently sufficient to assume that the ambient temperature of 300 °C is evenly spread through the interconnect. While this may not be true for systems including a dielectric, especially with novel dielectrics involving air, it is beyond the scope of this study, which deals with the influence of the grains inside the copper interconnect. An average current density of 1 MA/cm^2 is applied to the copper line for the electromigration simulation, resulting in the current density distribution shown in Fig. 13. From the figure, it can be noted that the material interfaces experience a significant reduction in the current density, while the grain boundaries are more complex. The grain boundary itself experiences a reduction in the current density, but the thin layers near the boundary show current accumulation. This behavior is due to the abrupt change in conductivity at the grain boundary, resulting in charge accumulation there.

3.3.2. Vacancy dynamics

The TCAD model used to calculate the vacancy dynamics and EM-induced stress is described in detail in [31]. The total vacancy flux depends on the current density $\overrightarrow{j}$ from Fig. 13 and is given by

$$\overrightarrow{J_v} = -D_v(\sigma)\left[\nabla C_v + \frac{C_v}{k_B\, T}\left(e\, Z^* \rho\, \overrightarrow{j} - \frac{Q^*}{k_B\, T}\nabla T + f\, \Omega \nabla \sigma \right) \right], \tag{11}$$

with C_v the vacancy concentration, Q^* the heat of transport, f the vacancy relaxation ration, Ω the atomic volume, and σ the hydrostatic stress. The influence of stress in the metal layer on the diffusivity also needs to be included in the vacancy dynamics. This effect is taken into account by modifying the diffusion coefficient expression from Eq. (7) and adding an exponential dependence on the hydrostatic stress as noted in [27]:

$$D_v = D_{v0}\, \exp\left(\frac{\Omega\, \sigma - E_a}{k_B\, T} \right). \tag{12}$$

The diffusivity's dependence on the hydrostatic stress, which changes during the electromigration simulation due to stress build-up,
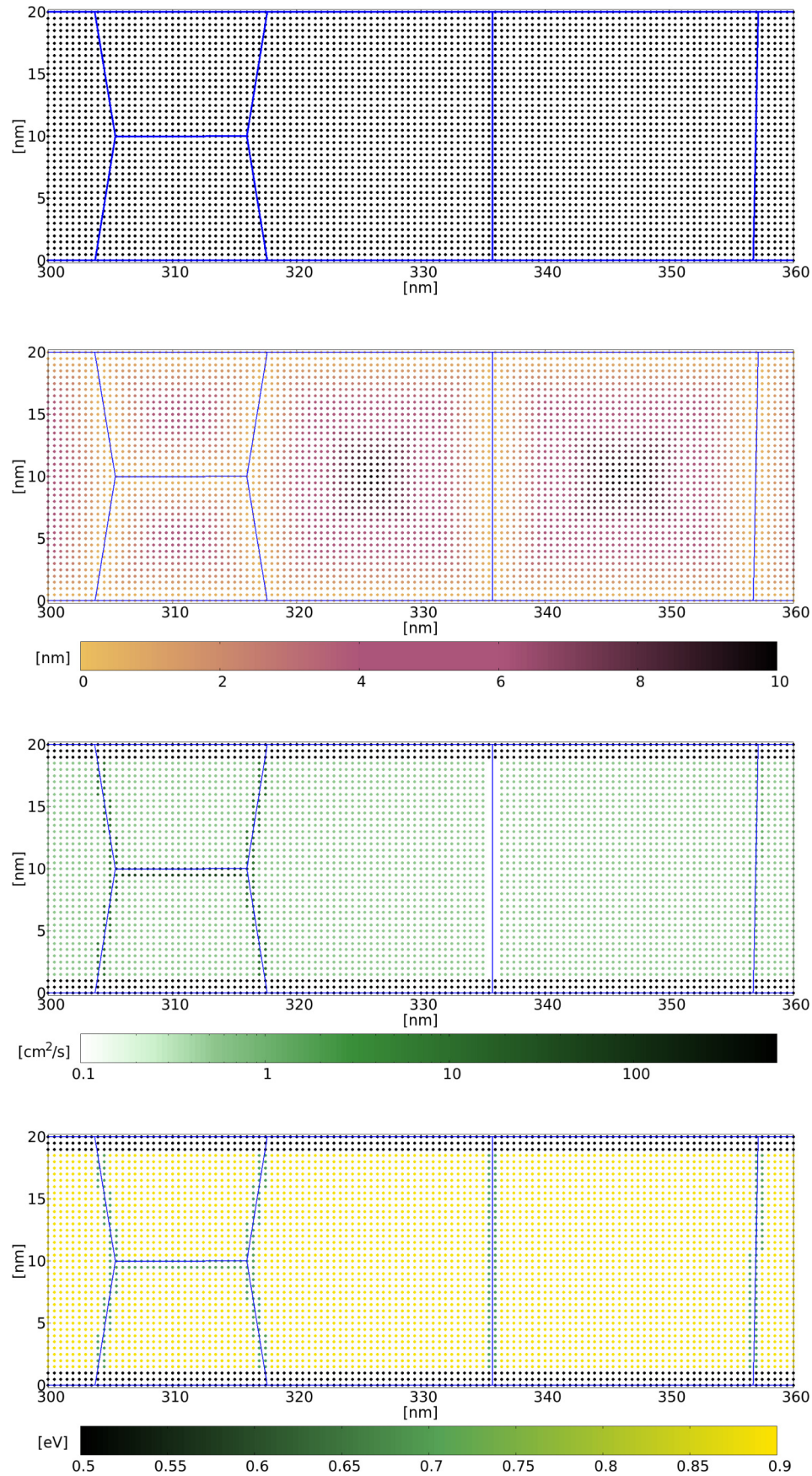
Fig. 10. Spatial parameter assignments at grid points as used in this study in order to properly treat the influence of grain boundaries and material interfaces during electromigration simulations. The grid size shown in all figures above is 0.5 nm. (a) Grid points with the exact edges overlayed; (b) distance from a grain boundary or material interface [nm]; (c) assigned values for the diffusion pre-exponential D_{v0} [cm^2/s]; and (d) assigned values for the activation energy for diffusion E_a [eV].
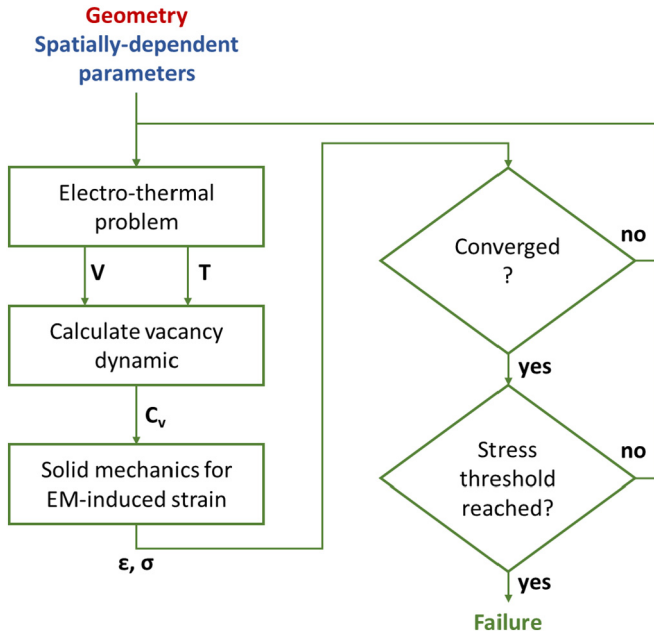
Fig. 11. Flow chart for the electromigration model.

is the reason why a spatial parameter for the diffusivity D is not applied in the previous step, but rather D_{v0} and E_a are used and the local diffusivity D is calculated every time the stress changes. The accumulation and depletion of vacancies is found according to the continuity equation

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J_v} + G, \tag{13}$$

where G is a surface function which models vacancy generation and annihilation, taking place at GBs and MIs only. Applying this term at the GBs and MIs only is also made possible with the presented method. This term is applied using

$$G = \frac{\partial C_{v,T}}{\partial t} = \frac{\chi}{\tau}\left[C_{v,eq} - C_{v,T}\left(1 + \frac{\omega_R}{\omega_T\, C_v}\right)\right], \tag{14}$$

where G is a spatial parameter applied to the entire interconnect line. In addition, $C_{v,T}$ and $C_{v,eq}$ are the trapped and equilibrium vacancy concentrations, respectively, τ is the relaxation time, ω_R and ω_T are the vacancy release and trapping rates, respectively, and χ is a step function which is 1 in the GB and MI and 0 otherwise. The spatial representations of parameter D_v, required to calculate the diffusion coefficient in Eq. (7) and Eq. (11), is given in Fig. 14. A logarithmic representation is chosen in order to better visualize the parameter, whose value varies by several orders of magnitude between the grain bulk and material interface. The parameter χ is shown in Fig. 15; essentially, it is only used to activate certain parts of the model which physically only take place at the boundaries and interfaces. As in previous figures, these parameters are shown only for a small section of the total interconnect surface.

Solving Eqs. (11) to (13) gives the time dependent change of the vacancy concentration inside the copper film. The rise of vacancies at one end of the wire and hillocks on the other end results in the increase in tensile and compressive stresses, respectively. Once a critical stress level is reached, the material can no longer conduct sufficient current for the required application, resulting in failure.

3.3.3. Electromigration-induced hydrostatic stress

The vacancy concentration, obtained by solving Eqs. (11) to (13), is accompanied by mechanical strain. This is due to the accumulation and reduction of vacancies at different locations in the interconnect. The changes in volume caused by the migration and formation of vacancies
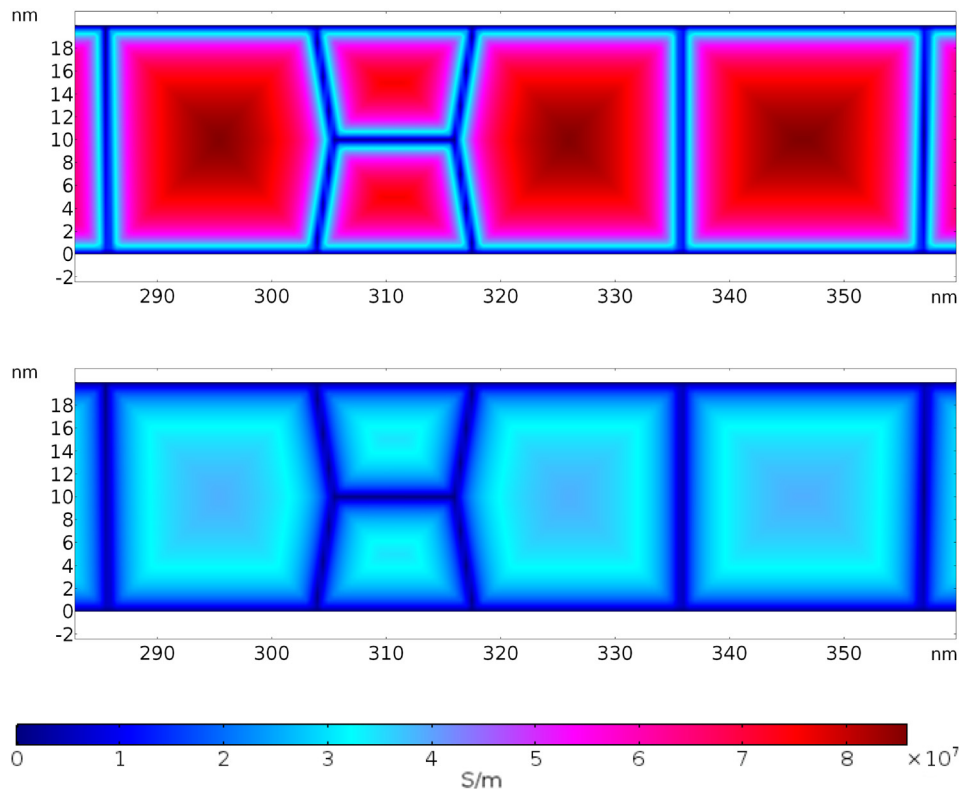

Fig. 12. Spatial parameters implemented within the finite element tool with the resulting spatial microstructure-dependent conductivity within the thin copper line. (a) Local conductivities at room temperature and (b) local conductivities under accelerated conditions (T = 300°C).
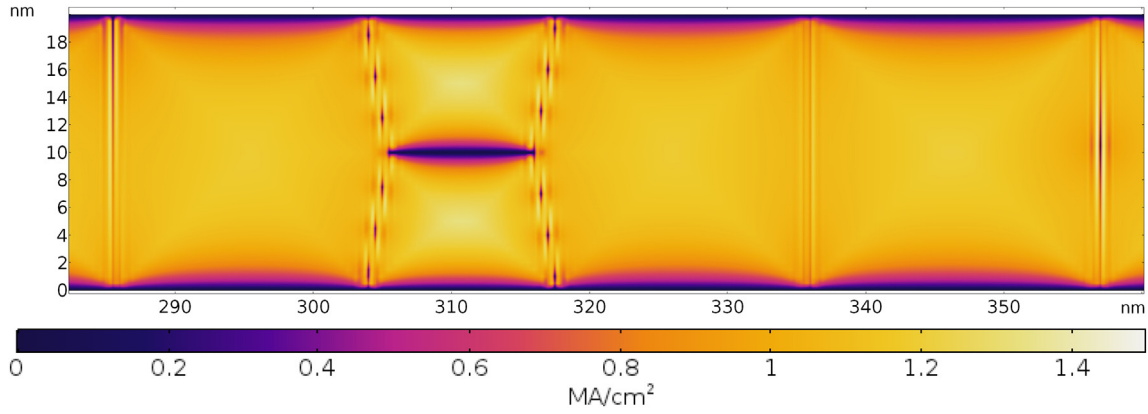
Fig. 13. Current density through a section of a copper line shown in Fig. 12 when a current density of 1 MA/cm^2 is applied.
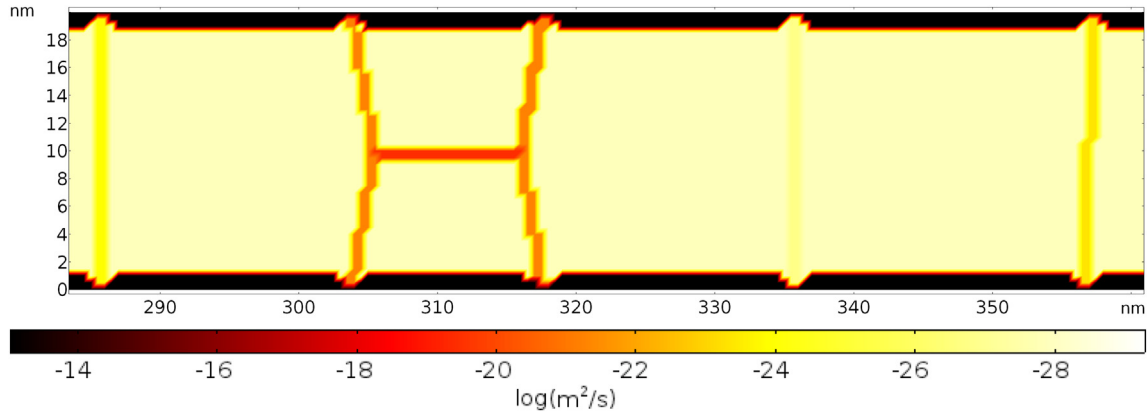

Fig. 14. Logarithm of the microstructure dependent vacancy diffusion coefficient D_v, used for the EM simulation in Eq. (11).
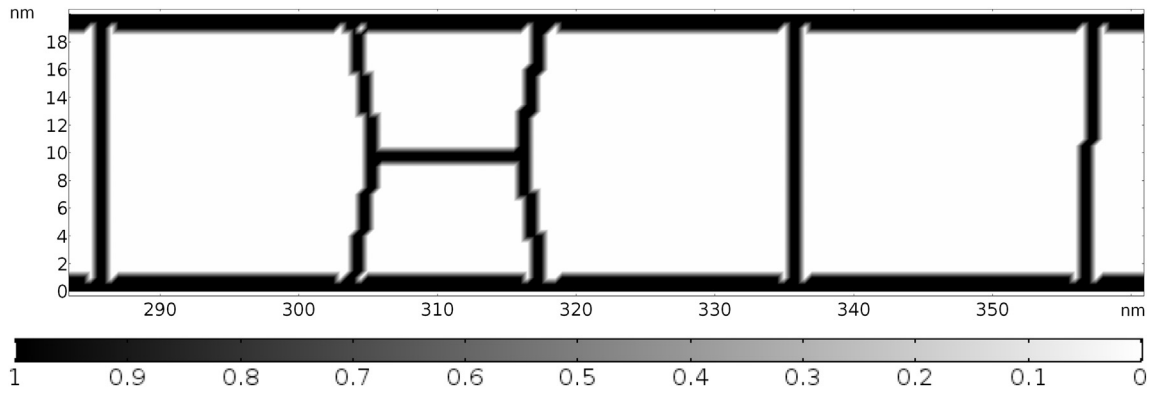

Fig. 15. Step function χ used to make sure vacancy generation and annihilation are only modeled in the GB and MI.

is represented by [43].

$$\frac{\partial \varepsilon}{\partial t} = \frac{\partial \varepsilon^m}{\partial t} + \chi \frac{\partial \varepsilon^f}{\partial t} \tag{15}$$

where ε is the trace of the strain tensor, while ε^m and ε^f represent the strain induced due to the migration and formation of vacancies. The second term is multiplied by χ because vacancy formation takes place only at the grain boundaries and material interfaces. The induced strain can then be derived to

$$\frac{\partial \varepsilon}{\partial t} = \Omega[(1 - f)\nabla \cdot \vec{J_v} + \chi f \, G]. \tag{16}$$

The above Eq. (16) connects the vacancy transport and mechanics models. Using Einstein's summation notation, the stress problem is given by the equilibrium equations [43,44].

$$\frac{\partial \sigma_{ij}}{\partial x_j} = 0 \qquad i, j = 1, 2, 3 \tag{17}$$

along with the small displacement approximation for line deformation

$$\varepsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right), \, i, j = 1, 2, 3 \tag{18}$$

and the constitutive equation

$$\sigma_{ij} = C_{ijkl} \, \varepsilon_{kl}, \tag{19}$$

where elastic deformation is assumed. The stress and strain tensor are given by σ_{ij} and ε_{ij}, respectively, and C_{ijkl} represents the stiffness tensor. Given that the strain in a dual-damascene interconnect is anistropic [19], the induced strain is modeled by applying one third of the strain

in Eq. (16) in each Cartesian direction.

Observing Eq. (11) and Eq. (16), we note that the vacancy flux depends on the stress, which in tern depends on the vacancy flux. In order to solve the above set of equations, time discretization is required and needs to be low enough that the induced error is minimal. In our solver, the entire flow sequence shown in Fig. 11 is solved at every time step. While segregated solvers are used to solve each of the electro-thermal, vacancy dynamics, and solid mechanics problems, Newton's method is used to obtain a solution to the entire set of equations at each step with a minimal error.

4. Simulations and discussion

The initial set of simulations were performed using bulk copper parameters from [19,43] and without including any microstructure components. All simulations were performed assuming an initial vacancy concentration of $C_{v0} = 10^{16} cm^{-3}$, evenly distributed throughout the copper line, with an applied current density of $1 \, MA/cm^2$ at a temperature of $300 \, °C$. The two-dimensional simulations were performed on a wire with a height of $20 \, nm$ with varying lengths of $250 \, nm$, $500 \, nm$, $750 \, nm$, $1000 \, nm$, $1500 \, nm$, and $2000 \, nm$, with the results shown in Fig. 16. It can be noted that the onset of vacancy transport and the slope of the increasing vacancy concentration is identical for all simulated lengths; however, the vacancy concentration reaches a steady state sooner in shorter metal lines, due to the atom back flux, which affects the vacancy diffusion [45]. The effect of the back flux is also noted in the reduction in the vacancy concentration after about $10^5 \, s$ for the 2000 nm line. The two ends of the copper line where accumulation of atoms and vacancies takes place are assumed to border a zero-diffusivity region, causing a sharp boundary. The reduction in vacancy accumulation therefore occurs because atom concentration at one end of the wire reaches its peak concentration and starts diffusing more towards the middle of the wire and towards the end where vacancies are forming. The same takes place on the other end with atom accumulation: As the concentration of atoms reaches its peak it starts to expand towards the middle of the wire, where it cancels out some of the vacancies, effectively dampening the electromigration effect. The shorter the wire is, the sooner this dampening takes place. Therefore, for the remaining simulations, a line length of 2000 nm was used, with a cross-sectional surface area of $20 \, nm \times 20 \, nm$ and an average grain diameter of 25 nm.
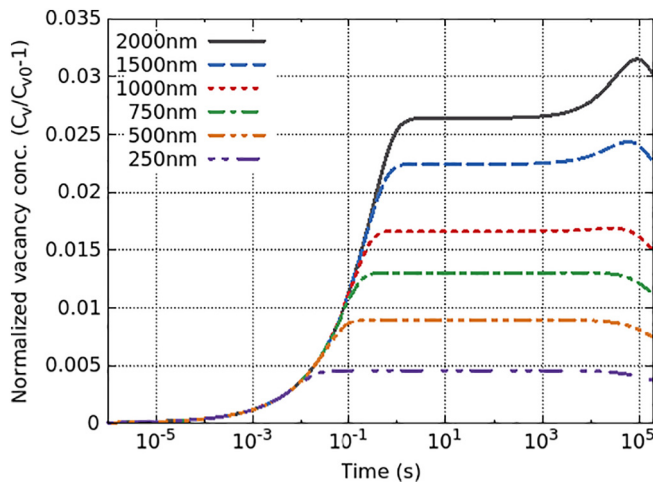

Fig. 16. Vacancy concentration in copper while ignoring microstructure effects for different line lengths with the line thickness set to 20 nm. A current density of $1 \, MA/cm^2$ is applied at a temperature of $300 \, °C$.

4.1. Vacancy concentration

The vacancy concentration at $t = 0 \, s$ and after $200 \, s$ under the previously described conditions for a copper interconnect shown in Fig. 8 is given in Fig. 17. In Fig. 17(a) the impact of the grain boundary on the initial re-distribution of the vacancies can be noted: The initial condition applied is that of evenly distributed vacancies throughout the copper line with a concentration $C_{v0} = 10^{16} cm^{-3}$. However, due to the different diffusivities in the grain bulk, grain boundary, and material interfaces, the vacancies immediately redistribute and the impact of the boundaries and interfaces is evident. If a more complex initial vacancy concentration or intrinsic stress needs to be included in the simulation, this can be done in one of two ways:

1) Using the spatial parameter assignment described in the previous section, one can include initial values for the vacancy concentration and residual stress.
2) The finite element simulator allows describing the initial values of all parameters as a function, dependent on the location (x,y,z), temperature, or any other environmental property.

After 200 s, the vacancy concentration in the grain bulk has caught up to that of the material interfaces, but the grain boundaries still play a role in their distribution, as evidenced in Fig. 17(b). Therein, the vacancy distribution within a grain follows the traditional pattern seen in continuum copper electromigration simulations, but at grain boundaries an abrupt change can be noted. This agrees with the prevailing opinion that columnar grain boundaries partially serve as vacancy blocking sites.

4.1.1. Mesh effects

Sample simulations were performed on a thin copper line using grid and mesh resolutions of 0.25 nm, 0.4 nm, 0.5 nm, 0.8 nm, and 1 nm for both the spatial parameter assignment and the electromigration simulation, with results for the vacancy concentration shown in Fig. 18. In these simulations, the resolution of the applied spatial parameters is identical to the mesh resolution. Once again, the simulation was performed on a 2000 nm long line with a cross-sectional surface area of $20 \, nm \times 20 \, nm$ and an average grain diameter of 25 nm. An initial vacancy concentration of $C_{v0} = 10^{16} cm^{-3}$ was assumed to be evenly distributed throughout the copper line and a current density of $1 \, MA/cm^2$ was applied at a temperature of $300 \, °C$. A large variation between the bulk and the granular copper structure can be noted, both in an increase in the vacancy concentration and in the early time at with which EM is initiated. We note also how well the 1 nm grid resolution replicates the smaller grids. Using a 1 nm grid spacing instead of 0.25 nm allows for a sixteen-fold decrease in simulation time and memory, a meaningful advantage of this framework.

The vacancy concentration plot in Fig. 19 shows the influence of a changing mesh resolution in the electromigration finite element simulator, while the resolution of the spatial parameter assignment is fixed at 0.1 nm. Once again, we note the quality of the method, even when the grid resolution is set to 2 nm. This resolution allows for a simulation to complete within about 10 min, while still taking into consideration the copper microstructure with reasonable accuracy.

4.2. Electromigration-induced hydrostatic stress

The electromigration-induced hydrostatic stress is described in Eqs. (15)–(19). In Fig. 20, the distribution of this stress in a section of the copper interconnect is shown. Of note is that the stress is significantly higher in the grain boundaries and material interfaces when compared to the grain bulk. In addition, we note that high stresses accumulate at triple points, where a grain boundary intersects a material interface. This is most pronounced at points $(x,y) = (336 \, nm, \, 0 \, nm)$ and $(x,y) = (336 \, nm, 20 \, nm)$ in the line shown in Fig. 20.
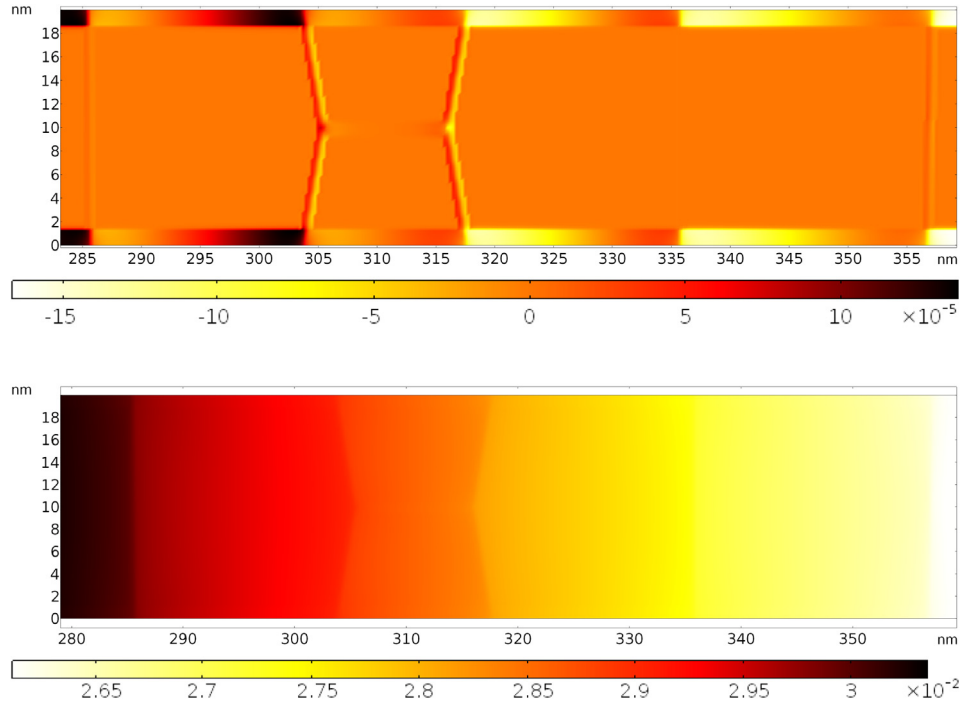
Fig. 17. Normalized vacancy concentration [$C_v/C_{v0} - 1$] at (a) t = 0 s and (b) t = 200 s. The average grain diameter is 25 nm, the applied current density is 1 MA/cm^2, and the applied temperature is 300 °C. (a) Normalized vacancy concentration at t = 0 s and (b) normalized vacancy concentration at t = 200 s.
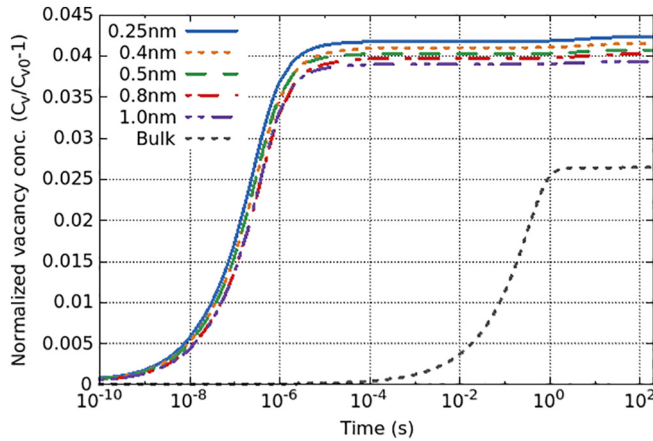

Fig. 18. Normalized vacancy concentration ($C_v/C_{v0} - 1$) using different mesh resolutions with the GB thickness set to 1 nm. Both the resolution of the spatial parameter application and the electromigration mesh are varied. The black dotted line represents bulk copper.
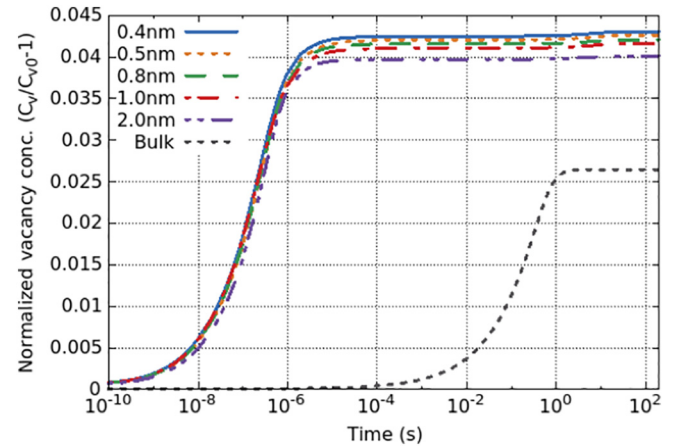

Fig. 19. Normalized vacancy concentration ($C_v/C_{v0} - 1$) using different mesh resolutions with the GB thickness set to 1 nm. The resolution of the spatial parameters is set to 0.1 nm, while only the mesh for the electromigration simulation is varied. The black dotted line represents bulk copper.

4.2.1. Mesh effects

In Fig. 21, the maximum EM-induced hydrostatic stress is plotted for various grid and mesh resolutions after performing the same simulations described in the previous section. The plot corresponds to a 200 s simulation with an applied current of 1 MA/cm^2 and an ambient temperature of 300 °C. For these simulations both the spatial parameter assignment and finite element mesh resolution was varied. The maximum stress was found to be at the far left corners of the wire where the x axis is at 0 nm; this corresponds to the furthest point in the direction of electron flow. This is expected since it is the first location in this structure where the vacancies can no longer diffuse and thereby only accumulate, causing the highest stress. We note that the mesh resolution has a significant influence on the calculated maximum stress, which is not desired and makes this result not trustworthy. Nevertheless, an advantage of this method is the ability to efficiently model the vacancy distribution and subsequent stress build-up in triple points

without the need for complex meshes. This is addressed later in this section.

The results shown in Fig. 22 confirm the previous observation that the mesh resolution has a significant influence on the calculated maximum stress. These simulations were performed with the spatial parameter assignment resolution set to 0.1 nm, while varying the electromigration finite element mesh from 0.4 nm to 2.0 nm. Once again the plot corresponds to a 200 s simulation with an applied current of 1 MA/cm^2 and an ambient temperature of 300 °C. Because we see significant mesh-dependent variation, this model should be used with this in mind and is useful to simulate the localized stress at various location in the copper interconnect, such as at triple points, but that it may not be accurate when attempting to find the maximum stress in a copper line.

When looking at the maximum EM-induced stress values, the dependence on the mesh resolution is evident. In Fig. 23 the maximum
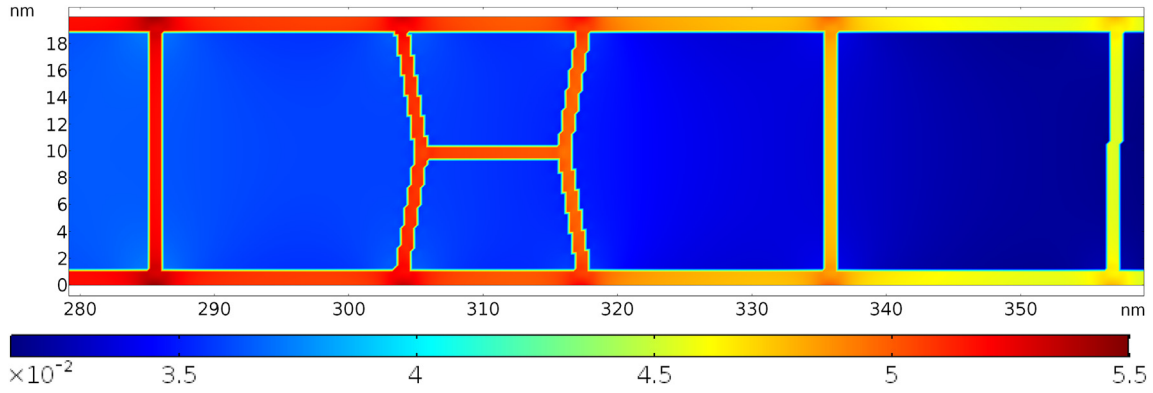
Fig. 20. Electromigration-induced hydrostatic stress (MN/m^2) $t = 200$ s. The average grain diameter is 25 nm, the applied current density is 1 MA/cm^2, and the applied temperature is 300 °C.
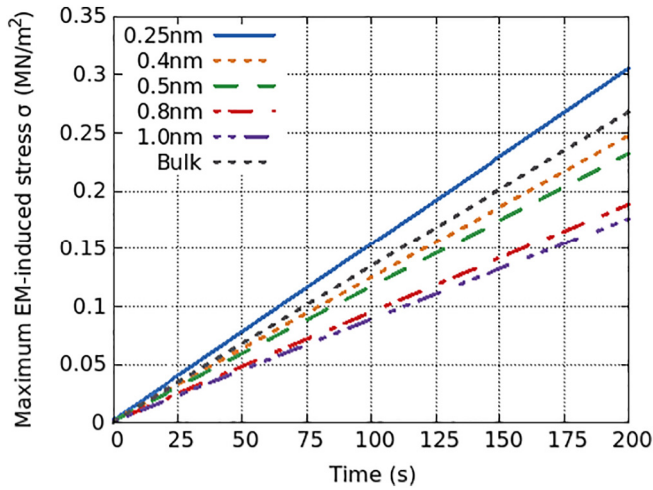

Fig. 21. Maximum EM-induced hydrostatic stress (NM/m^2) using different mesh resolutions with the GB thickness set to 1 nm. Both the resolution of the spatial parameter application and the electromigration mesh are varied. The black dotted line represents bulk copper.
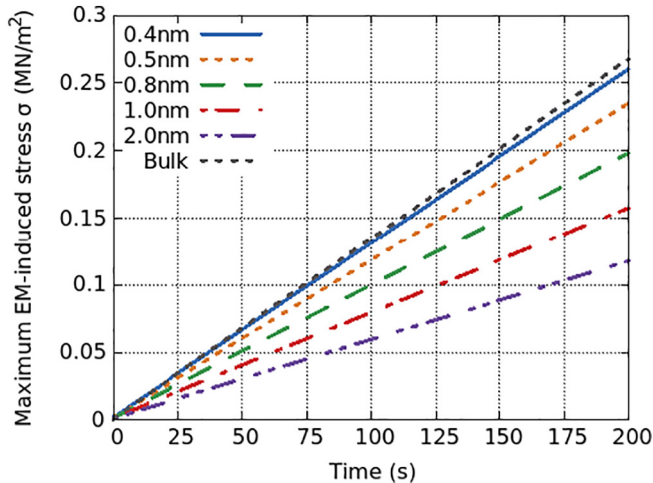

Fig. 23. Dependence of the mesh resolution on the calculated maximum electromigration-induced stress after a 200 s simulation at a current of 1 MA/cm^2 and at a 300 °C temperature. The red dots correspond to a case where the spatial parameter and EM grid are equivalent, while the blue squares have a spatial parameter spacing set at 0.1 nm. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

suggests that there are too many estimations taking place to calculate the maximum stress and that this section of the calculation cannot be trusted, even though the general trend of increasing stress with time is appropriate. It is also noteworthy that the grid resolution for the spatial parameter assignment does not influence the quality of the maximum EM-induced stress calculation.

4.2.2. Local stress

In order to test the influence of the mesh resolution on the calculated stress at a triple point, we observed the stress at coordinate $(x,y) = (124$ nm, 20 nm$)$, corresponding to a columnar grain boundary location between two grains, as can be seen in Fig. 8. The results are shown in Fig. 24 and Fig. 25 for varying mesh resolutions. When the resolution of the spatial parameter assignment and the finite element mesh was varied from 0.25 nm to 1 nm, the variation noted in the stress at the triple point was 7.6%. Setting the resolution of the spatial parameter assignment to 0.1 nm and varying the finite element mesh resolution from 0.4 nm to 2 nm resulted in a variation in the stress at the triple point of about 4.8%. Therefore, we can say with some confidence that the proposed method is able to provide relatively good estimates in the electromigration behavior of a nanosized copper interconnect even with course meshes and short simulation times. The

Fig. 22. Maximum EM-induced hydrostatic stress using different mesh resolutions with the GB thickness set to 1 nm. The resolution of the spatial parameters is set to 0.1 nm, while only the mesh for the electromigration simulation is varied. The black dotted line represents bulk copper.

induced stress after a 200 s simulation is plotted against the mesh resolution. Here, we note that a coarsening of the mesh by a factor of four results in a reduction of the calculated maximum stress by one half. This
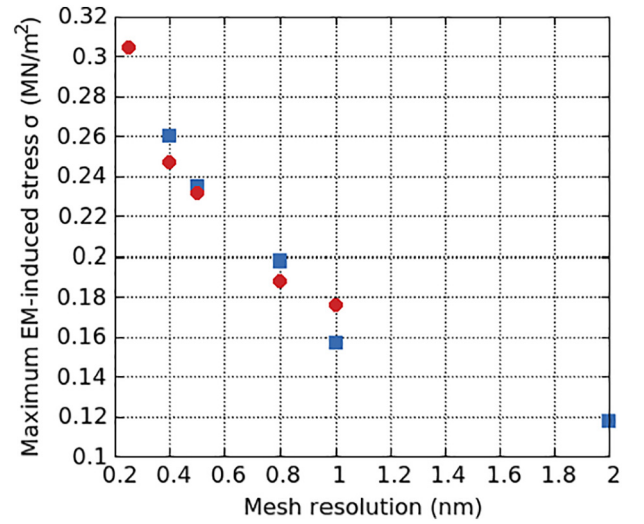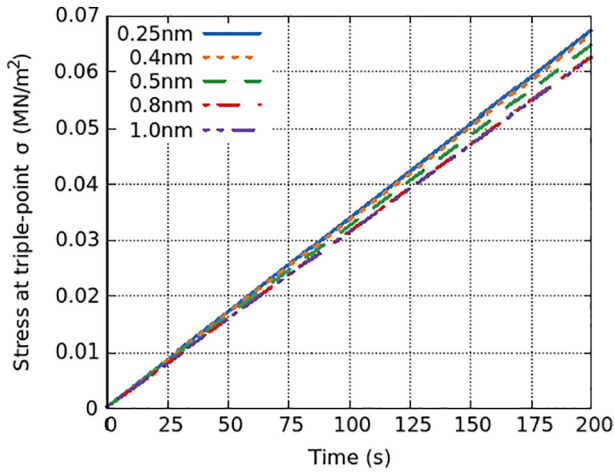
Fig. 24. EM-induced hydrostatic stress (NM/m^2) at a triple point when using different mesh resolutions with the GB thickness set to 1 nm. Both the resolution of the spatial parameter application and the electromigration mesh are varied.
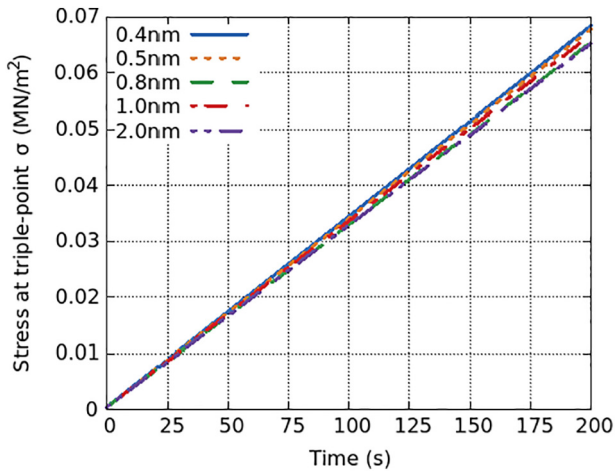

Fig. 25. EM-induced hydrostatic stress (NM/m^2) at a triple point when using different mesh resolutions with the GB thickness set to 1 nm. The resolution of the spatial parameters is set to 0.1 nm, while only the mesh for the electromigration simulation is varied.

simulation times are discussed further in the following section.

4.3. Simulation time

The simulation times for the vacancy concentration and electromigration-induced stress simulations are given in Fig. 26. Fig. 26(a) shows the simulation times for the electromigration simulation where both the spatial parameter resolution and mesh resolution are equally varied. We note a significant reduction in simulation time when using a 0.8 nm or 1 nm mesh resolution, without a significant loss in accuracy in the vacancy concentration or triple point stress, when compared to the 0.25 nm mesh.

In Fig. 26(b) the simulation times for the electromigration simulation when the spatial parameter resolution is fixed at 0.1 nm and the mesh resolution is varied. We note a similar behavior to that observed in Fig. 26(a), suggesting that the mesh resolution during the electromigration simulation is the determining factor for the simulation time and not the resolution of the applied spatial parameters.

5. Conclusion

Bulk electromigration models often underestimate the time at which electromigration effects are initiated as well as the vacancy concentration level at which back flux begins to take effect. This is due to the inability of bulk models to properly take into account the complex microstructure of a thin interconnect without increasing the computational complexity beyond realistic levels. For copper nano-interconnects it is essential to include the grain boundaries and material interfaces in any EM model due to their significant influence on conductivity and atom diffusivity.

Previous attempts to include microstructure have consisted of introducing grain boundaries and material interfaces as thin material layers independent of a copper grain or treating each grain in a copper line as independent. However, both of these methods require very fine and complex meshes. The increased complexity and computation time and memory frequently makes it impossible to perform accurate simulations. In this manuscript we presented a modeling framework which takes into consideration the grain boundaries and material interfaces while minimizing the computational effort and the simulation time. This is achieved by introducing spatial material parameters for the essential aspects of an EM model, those being atom diffusivity and conductivity. This allows using coarser meshes, while still achieving reasonable accuracy for the vacancy concentration change during simulation.

Furthermore, this simulation framework can be used to model the influence of triple points on the build-up of electromigration-induced stress. Triple points are those where grain boundaries and material
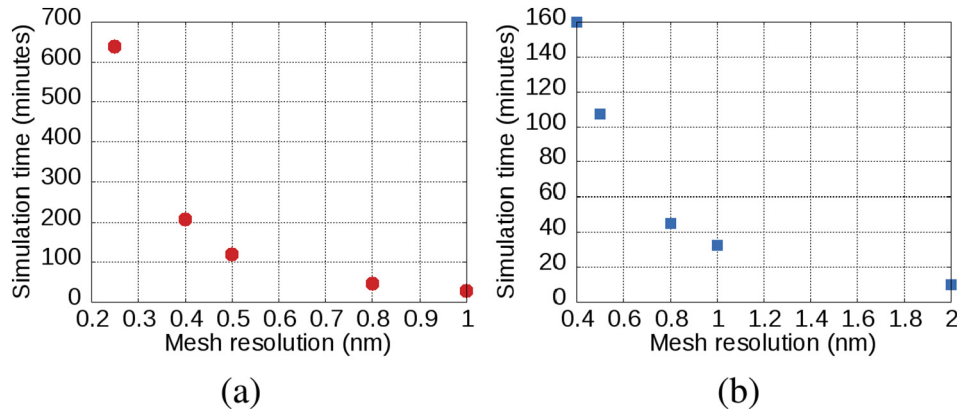

(a)

(b)

Fig. 26. The dependence of the mesh resolution on the simulation time for the electromigration simulations given in (a) Fig. 18, Fig. 21, and Fig. 24 and (b) Fig. 19, Fig. 22, and Fig. 25.

interfaces meet. We note that, although the model is not accurate in determining the maximum EM-induced stress in a full copper interconnect, it is able to reproduce the induced stress at triple points. Coarsening the mesh and allowing for a significant reduction in simulation time did not introduce significant errors, keeping mesh-induced variations below 8%.

Conflict of interest

There is no conflict of interest.

Acknowledgment

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