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Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors

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Two-dimensional semiconductors could be used to fabricate ultimately scaled field-effect transistors and more-than-Moore nanoelectronic devices. However, these targets cannot be reached without appropriate gate insulators that are scalable to the nanometre range. Typically used oxides such as SiO_2, Al_2O_3 and HfO_2 are, however, amorphous when scaled, and 2D hexagonal boron nitride exhibits excessive gate leakage currents. Here, we show that epitaxial calcium fluoride (CaF_2), which can form a quasi van der Waals interface with 2D semiconductors, can serve as an ultrathin gate insulator for 2D devices. We fabricate scalable bilayer MoS_2 field-effect transistors with a crystalline CaF_2 insulator of ~2 nm thickness, which corresponds to an equivalent oxide thickness of less than 1 nm. Our devices exhibit low leakage currents and competitive device performance characteristics, including subthreshold swings down to 90 mV dec^{-1}, on/off current ratios up to 10^7 and a small hysteresis.

Two-dimensional (2D) semiconductors are potential channel materials for next-generation field-effect transistors (FETs) and could extend the life of Moore's law by providing scaled channel geometries below 5 nm. FETs based on graphene[1], silicene[2], black phosphorus[3,4] and transition metal dichalcogenides (including MoS_2 (refs. [5–10]), $MoSe_2$ (ref. [11]), $MoTe_2$ (ref. [12]), WS_2 (ref. [13]) and WSe_2 (refs. [14,15])) have, for example, been reported. Furthermore, excellent transistor characteristics have been obtained for MoS_2 FETs, including on/off current ratios up to 10^{10} (ref. [8]) and subthreshold swing values down to 69 mV dec^{-1} (ref. [16]). There have also been attempts to create integrated circuits using MoS_2 FETs[17–19].

The miniaturization of 2D technologies without considerable loss in device performance is difficult. Although the fabrication of competitive 2D FETs with scaled channel dimensions is possible[20], scaling the gate insulator and controlling its precise thickness and quality remain challenging. Typically, oxides known from silicon technologies (such as SiO_2, Al_2O_3 and HfO_2) are used as an insulator, but these materials are amorphous when grown in thin layers, which makes the fabrication of high-quality interfaces with the channel difficult. To address this problem, different insulators need to be identified and hexagonal boron nitride (hBN) has, in particular, been intensively explored[21]. However, hBN has a small bandgap of ~6 eV (ref. [22]), a small dielectric constant of 5.06 (ref. [23]) and unfortunate band offsets to most 2D materials. As scaled technologies require equivalent oxide thicknesses below 1 nm (corresponding to a physical thickness of below 1.3 nm in hBN), hBN will result in excessive thermionic and tunnelling leakage currents (Supplementary Fig. 1).

Epitaxially grown—and thus crystalline—calcium fluoride (CaF_2) has attractive insulating properties even for a physical thickness of ~2 nm (equivalent oxide thickness of ~0.9 nm). It offers a combination of high dielectric constant ($\varepsilon = 8.43$), extremely wide bandgap ($E_g = 12.1$ eV) and high effective carrier mass ($m^* = 1.0 m_0$)[24]. It also has a closely matched lattice constant (0.546 nm) with silicon (0.543 nm), which allows high-quality CaF_2 layers to be grown on silicon and germanium substrates using molecular-beam epitaxy (MBE)[25,26]. Furthermore, the CaF_2(111) surface is terminated by fluorine atoms, which make it chemically inert and free of dangling bonds requiring hydrogen passivation[27], known to result in device reliability challenges. The inert nature of the CaF_2(111) surface has been confirmed previously by Auger spectra measurements[28], and heteroepitaxy of 2D materials on a 3D CaF_2 surface has been shown to be possible, even for considerable lattice mismatch, leading to a high-quality quasi van der Waals interface[28], a result that would not be achieved on chemically active substrates. Recent studies have demonstrated epitaxy of $MoSe_2$ (ref. [29]) and $MoTe_2$ (ref. [30]) on CaF_2(111) bulk substrates. These results underline that CaF_2 is compatible with 2D semiconductors and thus can be considered a promising insulating material for the very large-scale integration of 2D devices. It is also important that CaF_2 is stable in air and poorly dissolvable in water.

CaF_2 is only one of a wide class of epitaxial fluorides[25]. Some of these materials—such as antiferromagnetic NiF_2 (ref. [31]) and MnF_2 (ref. [32]), diamagnetic ZrF_2 (ref. [32]) and ferroelectric $BaMgF_4$ (ref. [33])—have additional properties that could be of value in the development of future electronic device technologies. Ferroelectric $BaMgF_4$ could, for example, be of use in the scaling of future negative-capacitance 2D FETs[34]. Nevertheless, the potential of fluorides in modern electronic devices has not yet been fully explored. Previously, CaF_2 films have been used as barrier layers in resonant tunnelling diodes[35] and superlattices[36], together with CdF_2 films. In terms of using CaF_2 as a gate insulator in FETs, only a few working transistors have been reported; these were based on 640-nm-thick CaF_2 layers and exhibited poor reproducibility[37]. However, over the past decade, considerable progress has been achieved in MBE-grown tunnel-thin CaF_2 layers, which has revived the idea of using fluoride insulators in FETs[38].

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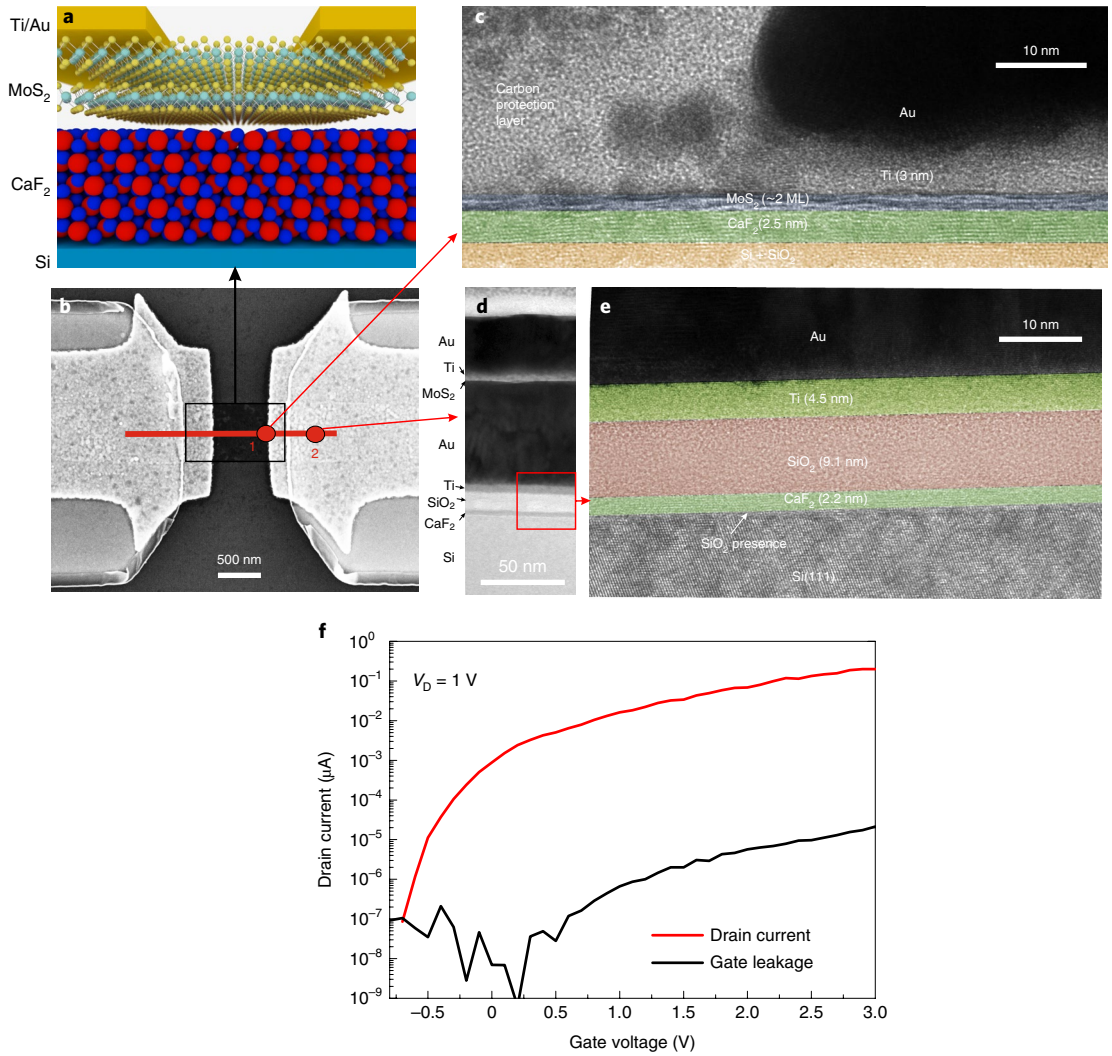

Fig. 1 | Bilayer MoS_2 FETs with 2-nm-thick CaF_2 insulators. a, Atomistic structure of the quasi van der Waals interface between F-terminated CaF_2(111) and MoS_2 in the channel area of our devices. **b**, SEM image of our MoS_2 FET. The black outline encloses the channel area with the source/drain electrodes, where MoS_2 is on top of CaF_2, as shown in **a**. The red line indicates the approximate location of the cut for the TEM sample, with two locations (1 and 2) where the images were collected. **c**, TEM image obtained in the channel area (location 1). **d**, Low-resolution TEM image obtained outside the channel area (location 2). The structure is the same as for the contact pads, with an SiO_2 isolation layer deposited on top of CaF_2 and MoS_2 sandwiched between two metal layers. **e**, High-resolution TEM image obtained in location 2 where the CaF_2 layers are visible. **f**, Gate leakage through the CaF_2 layer is negligible compared to the drain current, which underlines the high quality of our MoS_2 FETs.

In this Article, we show that CaF_2 can serve as a high-quality insulator for 2D technologies. We combine chemical vapour deposition (CVD)-grown MoS_2 with epitaxially grown CaF_2 to create bilayer MoS_2 FETs with CaF_2 gate insulators that are ~2 nm thick. Hundreds of devices were fabricated in order to study their variability and reproducibility.

Fabrication of MoS_2 FETs with ultrathin CaF_2 insulators

We deposited ultrathin CaF_2 layers onto an atomically clean Si(111) surface using an optimized MBE growth technique[26] at 250 °C (for further details see Methods). The growth process and crystalline quality of CaF_2 were controlled in real time using reflection high-energy electron diffraction (RHEED)[39] (corresponding images are provided in Supplementary Fig. 2). The thickness of CaF_2 measured by a quartz oscillator was 6–7 monolayers (MLs, 1 ML = 0.315 nm), which is close to the values measured using transmission electron microscopy (TEM). The first step of transistor fabrication consisted of the formation of SiO_2 (5–10 nm)/Ti/Au source/drain contact pads using sputtering. The MoS_2 film grown by CVD[40] at 750 °C was then transferred onto the substrate (see ref. [41] and Methods for further details). The quality of our MoS_2 films was examined using optical second harmonic generation (SHG), Raman spectroscopy and atomic force microscopy measurements. We found that our devices are located in a bilayer region of the MoS_2 film. The grain size is ~10–15 μm at the nucleation stage and several micrometres when the film is formed (Supplementary Figs. 3 and 4). Finally, MoS_2 channels with length L and width W varying between 400 and 800 nm were shaped, then additional electron-beam evaporated Ti/Au layers were deposited to contact the channels. (Further details about the structure of our devices are provided in Supplementary Fig. 5.)

Layout and microscopic structure of CaF_2/MoS_2 FETs

The atomic structure of CaF_2(111) is similar to that of 2D materials, with F–Ca–F monolayers with a thickness of 0.315 nm. This makes calcium fluoride a natural candidate for integration into 2D

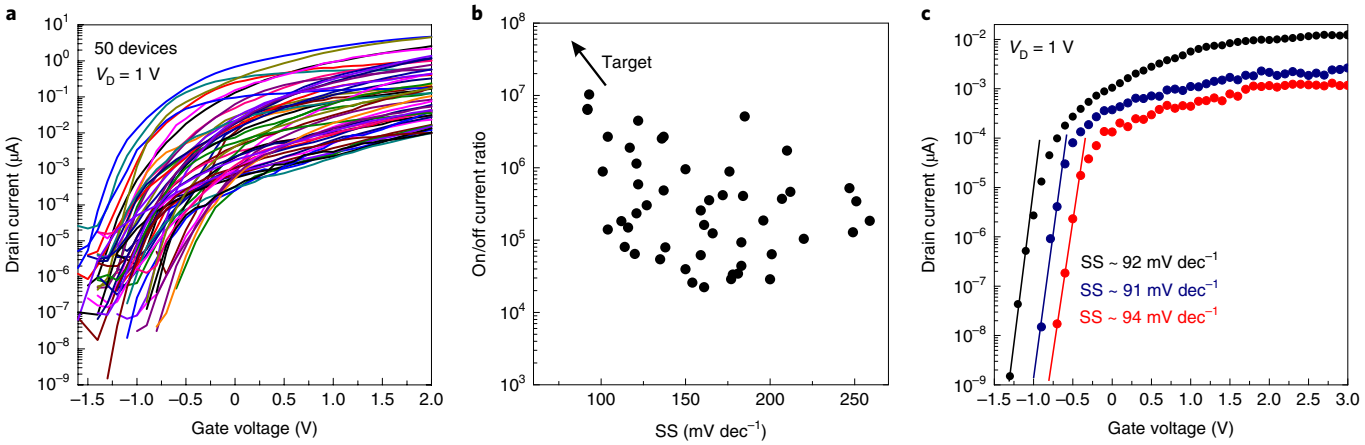

Fig. 2 | Device-to-device variability. a, I_D–V_G characteristics of 50 CaF_2/MoS_2 FETs from two different Si/CaF_2 substrates. **b**, Distributions of measured on/off current ratios and SSs for these devices. **c**, Some devices exhibit SS values down to 90 mV dec^{-1}. The lines represent linear fits to the data in the subthreshold regions.

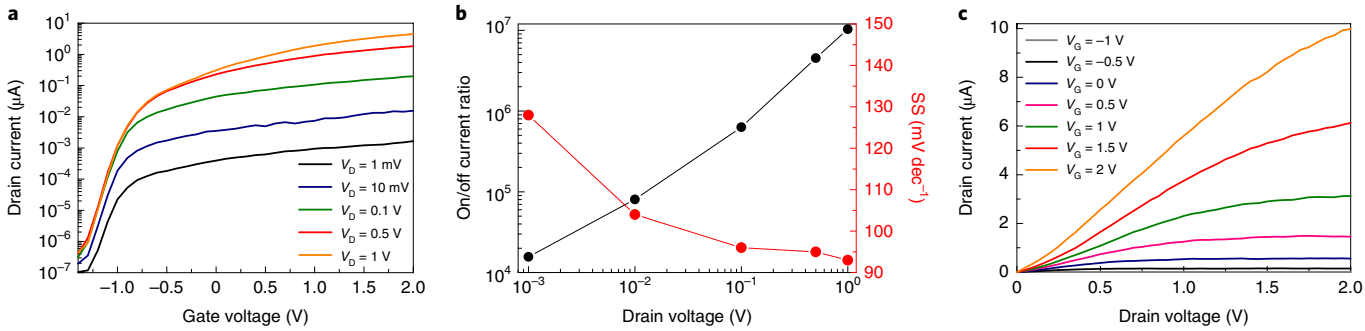

Fig. 3 | Best transistor performance achieved for our CaF_2/MoS_2 FETs. a, I_D–V_G characteristics measured for the best high-current device. **b**, On/off current ratio and SS extracted at different V_D (lines are guides to the eye connecting the experimental points). The best performance of this device is achieved at V_D = 1 V. **c**, I_D–V_D characteristics recorded on the same device exhibit saturation.

process flows. An essential ingredient of our devices is the virtually defect-free CaF_2(111)/MoS_2 interface, which is formed by the F-terminated calcium fluoride substrate, a quasi van der Waals gap and an atomically flat MoS_2 layer (Fig. 1a). This interface is present in the channel area and under the source/drain electrodes, as marked in the scanning electron microscope (SEM) image in Fig. 1b. To verify the layer structure of our device, we cut a 70-nm-thick specimen using a focused ion beam (FIB) along the line marked in Fig. 1b and performed TEM measurements. Figure 1c shows a TEM image obtained for the channel area. The interface between MoS_2 and layered crystalline CaF_2 of ~8 ML, which corresponds to a physical thickness of ~2.5 nm, can be clearly seen. For different substrates, the number of CaF_2 monolayers varies between six and eight (thickness between 1.9 and 2.5 nm). By recording electron energy loss spectra (EELS; see Supplementary Fig. 6) at the interface between CaF_2 and the Si substrate we observe some SiO_2 (less than 1 nm thick), which is formed by oxidation resulting from prolonged exposure to air of our CaF_2/Si substrates before device fabrication.

Taking into account thickness fluctuations[26] of the CaF_2 and the presence of a thin thermal oxide layer, we modelled the tunnel leakages measured for numerous devices and found that the effective gate insulator thickness is ~2 nm (Supplementary Fig. 8). The layered structure of our CaF_2 films is clearly visible in the TEM image obtained using low-dose imaging (Fig. 1c,e). Although electron irradiation is known to be destructive for CaF_2 samples[42], these investigations indicate the extremely high stability of our thin CaF_2 layers, where the desorption of F by the electron beam and subsequent formation of CaO are not as favourable as in CaF_2 bulk crystals[42]. Nevertheless, we found that TEM measurements can destroy the Si substrate a few nanometres below the Si/CaF_2 interface; however, this only occurs within the channel area (Supplementary Fig. 7). Outside the channel area our sample is unaffected by TEM irradiation. There we can clearly see MoS_2 sandwiched between two metal layers and an SiO_2 isolation layer on top of the CaF_2/Si substrate (Fig. 1d,e). As a final verification of the properties of our 2-nm-thick CaF_2 insulator, the measured gate leakage was found to be negligible compared to the drain current of our MoS_2 FET (Fig. 1f).

Performance characteristics of CaF_2/MoS_2 FETs

Using the process flow described above, we fabricated over 100 devices on two different CaF_2 substrates. In Fig. 2a we show the gate transfer (I_D–V_G) characteristics measured for 50 devices from both substrates. The typical on currents vary from 1 nA to nearly 10 μA, which is probably because of the non-homogeneous nature of the CVD MoS_2 film and different effective channel widths. At the same time, the measured on/off current ratios of some devices approach 10^7 (Fig. 2b), which is excellent for back-gated MoS_2 FETs with a tunnel-thin gate insulator. Note that for the devices with overall lower currents, the measured on/off current ratios are probably underestimated due to the limited measurement resolution,

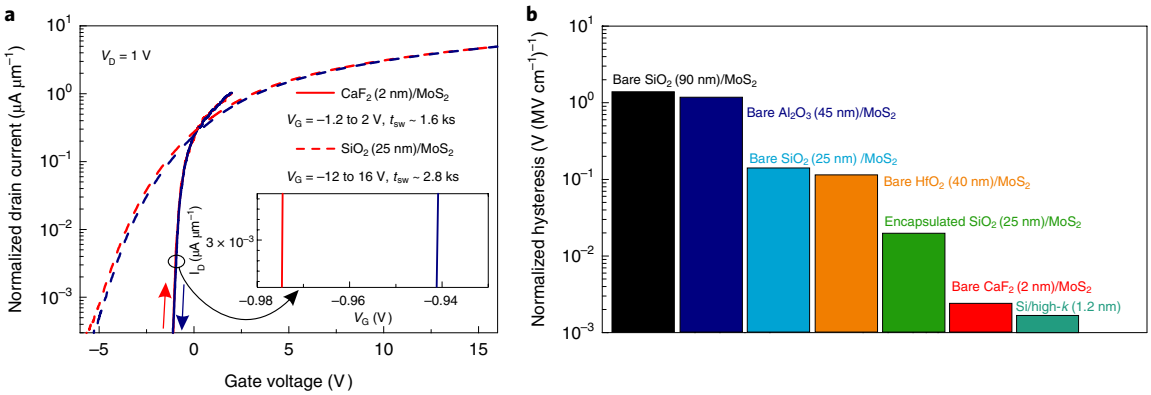

Fig. 4 | Hysteresis in our CaF_2/MoS_2 FETs. a, Ultra-slow sweep I_D-V_G characteristics measured for our CaF_2(2 nm)/MoS_2 FETs and Al_2O_3-encapsulated SiO_2(25 nm)/MoS_2 devices reported in our previous work[8]. Inset: hysteresis in our CaF_2(2 nm)/MoS_2 FETs near V_{th}. **b**, For comparable sweep times, the hysteresis width has to be normalized to the insulator field factor $\Delta V_G/d_{ins}$. For our best CaF_2(2 nm)/MoS_2 devices it is comparable to Si/high-k (1.2 nm) FETs, and the worst device has few times larger hysteresis (Supplementary Fig. 12). Note that the values for the Al_2O_3/MoS_2 (ref. [48]) and HfO_2/MoS_2 FETs[50] could be underestimated, because much smaller sweep times have probably been used in the corresponding studies.

which affects the off current. At the same time, the subthreshold swing (SS) values of most devices are smaller than 150 mV dec^{-1}, while being close to 90 mV dec^{-1} for some devices (Fig. 2b,c). These values are among the best ever reported for back-gated MoS_2 FETs. Although in these prototypes SS ≈ 90 mV dec^{-1} is achieved mostly for the devices with lower current (Fig. 2c), several high-current devices also exhibit small SS values (for example, Fig. 3). We also performed technology computer-aided design (TCAD) simulations using our previously established models for MoS_2 FETs[43,44] (for more details see Methods) and obtained reasonable fits of the measured I_D-V_G characteristics (Supplementary Figs. 9–11). According to these results, the SS of our devices is not affected by Schottky barriers, which are known to be one of the major factors limiting the performance of MoS_2 FETs[45,46]. This is because for an insulator thickness of only ~2 nm the Schottky barrier has negligible length, thus being almost completely transparent. As such, the deviation of our SS values from 60 mV dec^{-1} is mainly due to defects (for example, S vacancies) in our CVD-grown MoS_2 films, as well as a possible presence of adsorbates on top of the bare MoS_2 channel and at the interface with CaF_2. This leads to an interface state density $D_{it} \approx 1 \times 10^{13}$ cm^{-2} eV^{-1} (for more details see Supplementary Fig. 11), which is similar to the values typically measured for CVD-grown MoS_2 films[47]. Thus, we believe that further optimization of MoS_2 processing in FETs fabricated on epitaxial fluorides and transition to more versatile configurations, such as top-gated devices and perhaps negative-capacitance FETs with ferroelectric fluorides[33], will lead to further improvements of these emerging devices.

In Fig. 3a we show typical I_D-V_G characteristics measured for a device that simultaneously exhibits high drain currents and steep SS (TCAD fits of these results are provided in Supplementary Fig. 9). The best transistor performance is achieved at $V_D = 1$ V, with a maximum measured on current of ~5 μA (or ~6 μA μm^{-1} if normalized to the channel width), on/off current ratio close to 10^7 and SS as small as 93 mV dec^{-1} (Fig. 3b). The output (I_D-V_D) characteristics measured for different V_G (Fig. 3c) also show promising behaviour with a large degree of current control and saturation. All these results confirm the promising nature of our devices and thus the high potential for further development, especially taking into account that such fundamental limitations as Schottky barriers are already addressed by scaling of the insulator thickness.

Electrical stability of CaF_2/MoS_2 FETs

Finally, we verified the electrical stability of our CaF_2/MoS_2 FETs by performing ultra-slow sweep hysteresis measurements with total sweep times t_{sw} of several thousands of seconds. In Fig. 4a we compare the I_D-V_G characteristics measured for our CaF_2/MoS_2 devices with those of SiO_2/MoS_2 FETs with Al_2O_3 encapsulation reported in our previous work[8], which were found to exhibit the smallest hysteresis ever observed in 2D technologies. In addition to comparable values of I_D normalized to the channel width and considerably smaller SS for our CaF_2/MoS_2 FETs, we found that the hysteresis width ΔV_H in our best CaF_2/MoS_2 FETs is very small. For a fair comparison we normalized ΔV_H to the insulator field factor[8] $\Delta V_G/d_{ins}$, with ΔV_G being the width of the V_G sweep range. In Fig. 4b we compare the related results for our CaF_2/MoS_2 FETs (for more data see Supplementary Figs. 12 and 14) with literature reports for different technologies[8,48–50] and our measurement data for Si/high-k FETs (Supplementary Fig. 13). Although our devices with ultrathin CaF_2 operate at considerably higher insulator fields of up to 10 MV cm^{-1} (compared with 6.4 MV cm^{-1} for the devices with 25-nm-thick SiO_2), their hysteresis stability is even better than for encapsulated SiO_2/MoS_2 FETs, not to mention less advanced devices with bare channels. Furthermore, the values for our best CaF_2/MoS_2 FETs, such as the device shown in Fig. 4a, are comparable to Si/high-k FETs. However, some of our devices were found to exhibit a more sizable hysteresis (Supplementary Fig. 12), though still smaller than in encapsulated SiO_2/MoS_2 FETs. The variability of the hysteresis between different devices is probably due to the grainy structure of our CVD-grown MoS_2 film (Supplementary Fig. 3), which leads to a different local quality of MoS_2 for different devices. Namely, the channels of some devices contain certain grain boundaries with numerous S vacancies[51–53]. In addition to degrading the device performance, these S vacancies are able to interact with water adsorbates penetrating through the grain boundaries towards the CaF_2/MoS_2 interface, thus causing the hysteresis[54]. Note that direct trapping of carriers by S vacancies or other channel defects[55] does not appear to be a possible mechanism for the hysteresis, as these processes are very fast[44]. At the same time, our best devices probably contain more uniform channels, which makes the hysteresis considerably smaller (a more detailed discussion about the origin of the hysteresis in our CaF_2/MoS_2 FETs is provided in Supplementary Section 8). As such, the hysteresis in our devices is mostly due to the channel quality and the interaction of the bare MoS_2 films with the environment, which should not be expected in devices with passivated channels. This is very different from MoS_2 FETs with amorphous SiO_2, Al_2O_3 and HfO_2 insulators, where a considerable contribution to the hysteresis comes from oxide defects energetically aligned within certain defect bands[56]. Therefore, we can conclude that CaF_2 is nearly free from

slow insulator traps that would be able to contribute to charge trapping issues near the CaF_2/MoS_2 interface. The latter indicates that in addition to an excellent transistor performance, 2D FETs with CaF_2 are also more than competitive in terms of their reliability, which is a fundamental requirement for commercial applications.

Conclusions

We have reported CVD-grown bilayer MoS_2 FETs on an epitaxially grown CaF_2 insulator that has a thinness of only 2 nm, and have shown that this scalable technology can be used to fabricate numerous transistors on a single chip. The devices exhibit SSs down to 90 mV dec^{-1} and on/off current ratios up to 10^7, which are among the leading values reported for back-gated devices. Notably, our CaF_2/MoS_2 FETs appear to be free from the performance-limiting effects of Schottky barriers, which is due to the use of the tunnel-thin gate insulator. Furthermore, we have demonstrated that the devices have a high electrical stability even for insulator fields of 10–15 MV cm^{-1} and exhibit a record small hysteresis for 2D devices. These device characteristics are due to the valuable dielectric properties of CaF_2 and its good compatibility with MoS_2, which leads to a virtually defect-free quasi van der Waals interface between the materials. Together with the recent demonstration of epitaxial growth of 2D semiconductors on $CaF_2(111)$ (refs. [29,30]) our results suggest that calcium fluoride could provide ultra-scaled dielectric layers for the development of next-generation 2D nanoelectronics.

Methods

MBE growth of CaF_2 insulators. Ultrathin CaF_2 layers were epitaxially grown on weakly doped single-crystal n-Si(111) substrates with $N_D = 1\times10^{15}$ cm^{-3} and a misorientation of 5 to 10 angular minutes. Before the growth process, a protective oxide layer was formed after chemical treatment by following the procedure suggested in ref. [57]. This layer was removed by annealing for 2 min at 1,200 °C under ultra-high-vacuum conditions (~10^{-8}–10^{-7} Pa). This allowed us to obtain an atomically clean 7×7 Si(111) surface. The CaF_2 film was grown on this surface by MBE at 250 °C, which is known to be the optimum temperature to produce pinhole-free homogeneous CaF_2 layers[26]. The deposition rate of CaF_2 measured by a quartz oscillator was ~1.3 nm min^{-1}. The growth processes and crystalline quality of the CaF_2 layers were monitored using RHEED with an electron energy of 15 keV (see the diffraction images in Supplementary Fig. 2).

Device fabrication. A bilayer MoS_2 film serving as a channel was grown on *c*-plane sapphire using the CVD process described in ref. [40]. Namely, CVD growth was performed at atmospheric pressure and 750 °C using sulfur and MoO_3 as powder precursors and ultra-high-purity Ar as the carrier gas.

All lithography steps were carried out using electron-beam lithography. First we deposited SiO_2(5–10 nm)/Ti/Au contact pads using sputtering. Isolation with the SiO_2 layer is required to minimize parasitic leakage currents through the 15–20 μm sized square electrodes, which have to be so large to form a reliable contact with the probe. Then 7×7 mm CVD-grown MoS_2 films were transferred onto the $CaF_2(111)$ substrate with pre-shaped isolated contact pads using the process suggested in ref. [41]. In particular, we used a polystyrene film as a carrier polymer and dissolved it in toluene after the transfer process. The transferred MoS_2 film was subsequently etched by reactive ion etching to define the transistor channels with *L* and *W* between 400 and 800 nm. Finally, the channels were contacted by electron-beam-evaporated Ti/Au pads deposited on top of MoS_2 in the contact areas. This second layer of Ti/Au was slightly extended to contact the MoS_2 on top of the bare CaF_2 surface.

TEM measurements. To achieve a high contrast in TEM measurements, the devices were covered by a 10-nm-thick carbon layer deposited using sputtering. After this, a TEM lamella preparation process was performed with a dual beam system. First a thicker granular platinum protective layer was deposited using a focused electron beam followed by focused ion beam deposition. A TEM lamella was cut out along the channel of the device. Finally, the samples were examined using a TEM set-up at a pressure of ~1×10^{-5} Pa. During the measurements, we recorded EELS spectra to verify the layer structure of our device.

SHG and Raman analysis of the MoS_2 films. To evaluate the number of layers in our MoS_2 film, we performed optical SHG measurements. First we obtained a SHG map in the single-layer area of our film grown on a sapphire substrate and evaluated the grain sizes. We examined a 50×50 μm^2 area of the film transferred onto the CaF_2 substrate, where most of our devices are located. From the obtained SHG map and polarization-resolved SHG images, we determined an even number of layers in our film. Finally, we performed Raman measurements with a 532 nm laser and confirmed the bilayer thickness of the MoS_2 film.

Electrical characterization. Electrical characterization of our MoS_2/CaF_2 FETs consisted of measurements of I_D-V_G and I_D-V_D characteristics. These measurements were conducted using a Keithley 2636 parameter analyser in the chamber of a Lakeshore vacuum probe station (~5×10^{-6} torr) at room temperature and in complete darkness. To correctly resolve the on/off current ratio, we used the autorange measurement mode. The hysteresis of the I_D-V_G characteristics was investigated by doing double sweeps with varied sweep times t_{sw}. The extracted hysteresis widths were plotted versus the measurement frequency $f = 1/t_{sw}$, as suggested in our previous work[49].

TCAD simulations. For the simulations of the device characteristics we used a drift-diffusion model implemented into our TCAD simulator MINIMOS-NT[58] within the GTS framework (http://www.globaltcad.com/en/products/minimos-nt.html). Because 2D FETs lack an efficient doping scheme and the Fermi level of most metals is pinned within the bandgap, the current flow at the contacts is dominated by Schottky barriers[59,60]. As such, our drift-diffusion TCAD method is coupled with a model accounting for both tunnelling through the potential barrier and thermionic emission[45]. This modelling framework was previously calibrated to MoS_2 devices with a SiO_2 gate dielectric[43,44].

Data availability

The data that support the graphs within this Article and further details of this study are available from the corresponding author upon reasonable request.

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Author contributions

Y.Y.I. introduced the idea of MoS_2 FETs with an ultrathin CaF_2 insulator, performed their characterization and prepared the manuscript. A.G.B. performed MBE growth of CaF_2 and provided the substrates. D.K.P. and S.W. fabricated MoS_2 FETs. T.K. performed TCAD simulations. M.T. contributed to preparation of figures. L.M. and M.P. performed SHG and Raman measurements, respectively. M.S.-P. and A.S.-T. performed TEM measurements and sample preparation, respectively. M.I.V. performed quantitative analysis of gate leakage currents using tunnel models. M.W. programmed electrical measurements. N.S.S., T.M. and T.G. supervised this work. All authors regularly discussed the results and commented on the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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