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Reliability of scalable MoS_2 FETs with 2 nm crystalline CaF_2 insulators

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Abstract

Two-dimensional (2D) semiconductors are currently considered a very promising alternative to Si for channel applications in next-generation field-effect transistors of sub-5 nm designs. However, their huge potential cannot be fully exploited owing to a lack of competitive insulators which are required to effectively separate the channel from the gate, while being scalable down to few nanometers thicknesses. Recently we have made an attempt at addressing this issue by using crystalline CaF_2 insulators and demonstrated competitive MoS_2 devices with the insulator thickness of only about 2 nm. Here we report a detailed study of the performance, reliability and thermal stability of these devices. We demonstrate that, in contrast to SiO_2 and other amorphous oxides, CaF_2 has a very low density of insulator defects which are responsible for the hysteresis and long-term drifts of the transistor characteristics. At the same time, CaF_2 exhibits smaller leakage currents and higher electric stability compared to hBN. By comparing our MoS_2 transistors with CaF_2 fabricated using MoS_2 films of different quality, we show that the major limitations on the performance and reliability of these devices come from the bare channel rather than from the superior CaF_2 insulator. Finally, we perform the first study of degradation mechanisms only observed for tunnel-thin gate insulators in 2D devices. While these degradation mechanisms are similar for hBN and CaF_2, they are less pronounced in CaF_2. Our results therefore present a solution to a very important roadblock on the way towards fully scalable 2D nanoelectronics with competitive performance and reliability.

Next-generation field-effect transistors (FETs) with two-dimensional (2D) channel materials provide a means to overcome the limitations of Si technologies and enable scaled channel geometries below 5 nm, thereby extending Moore's law. Starting from the first graphene FETs [1, 2], several groups have fabricated functional FETs with other 2D materials. Among them most attention has been paid to transition metal dichalcogenides such as MoS_2 [3–8], $MoSe_2$ [9], $MoTe_2$ [10], WS_2 [11] and WSe_2 [12, 13]. In addition, successful demonstrations of FETs with more exotic materials such as black phosphorus [14, 15] and even silicene [16] can be also found in the literature. Up to now, MoS_2 FETs have been shown to exhibit the best performance, with sub-threshold swing (SS) [8] values down to 69 mV dec^{-1} and on/off current ratios [6] up to 10^{10}. Furthermore, several attempts on circuit integration of MoS_2 FETs have been also reported [17–19].

Despite all recent progress achieved on 2D FET prototypes, the transition towards commercial 2D FETs still remains a challenge. The main reasons for this are the absence of fully scalable fabrication process flows and a poor reliability of the currently available devices, which are mainly due to the absence of competitive insulators for these new technologies. For instance, conventional oxides, such as SiO_2, Al_2O_3 and HfO_2, are amorphous when grown in thin layers and contain numerous defects. This leads to a poor quality of the interfaces with 2D channels and thus strongly

degraded device performance and reliability [20–22]. On the other side, the use of 2D hexagonal boron nitride (hBN), which is often considered to be the best insulator for future 2D devices [23, 24], has indeed resulted in significantly enhanced channel mobilities [25] and improved reliability [21, 26], owing to a van der Waals interface between hBN and 2D semiconductors. However, hBN has a small out-of-plane low-frequency dielectric constant of either 3.76 [27] or 5.06 [28], a small bandgap of about 6 eV [29] and unfortunate band offsets to most 2D materials. As such, hBN appears to be barely suitable for the use in ultra-scaled 2D devices with equivalent oxide thicknesses (EOT) below 1 nm (corresponding to a physical thickness of below 1.3 nm in hBN), as it will lead to excessive thermionic and tunneling leakage currents.

In our recent work [30] we have made an attempt to overcome this bottleneck and reported functional MoS_2 FETs with crystalline calcium fluoride (fluorite, CaF_2) of only about 2 nm thickness, while reaching SS down to 90 mV dec^{-1} and on/off current ratios up to 10^7 already for the first prototypes. In contrast to conventional oxides and hBN, CaF_2 insulators satisfy all the conditions required for scalable 2D electronics, a huge bandgap ($E_g = 12.1$ eV) and a comparably high dielectric constant ($\varepsilon = 8.43$) [31]. This allows us to achieve tunnel leakage currents which are comparable to those through the typically used high-k oxides even for sub-1 nm EOT, while outperforming hBN and SiO_2 by several orders of magnitude [30, 32]. At the same time, the inert CaF_2(1 1 1) surface forms a quasi van der Waals interface [33] with 2D materials (figure 1(a)), which is of much higher quality than the interfaces between 2D materials and currently used oxides. This, in particular, makes heteroepitaxy of 2D materials on CaF_2(1 1 1) possible, as already confirmed for $MoSe_2$ [34] and $MoTe_2$ [35]. Finally, the layer thickness and crystalline quality of CaF_2 can be controlled on-site when growing this material on Si(1 1 1) substrates using molecular beam epitaxy (MBE), see more details in the methods section.

While opening a way to the further development of 2D FETs and other emerging devices with various fascinating fluoride materials [36–38], we argue that estimation of the real potential of any new technology requires proper understanding of their reliability. In particular, all previously reported 2D FETs suffer from charge trapping by insulator defects. This charge trapping appears as a fast sweep hysteresis [20, 21, 39–42] and long-term drifts of the gate transfer characteristics [21, 43–46], which are known from Si technologies as bias-temperature instabilities (BTI) [47, 48]. Here we examine CaF_2(2 nm)/MoS_2 FETs similar to those reported in our previous work [30] and pay particular attention to their reliability. By comparing the results for CaF_2/MoS_2 FETs with different channel quality and their counterparts with hBN and SiO_2, we demonstrate that in devices with CaF_2 insulators the main reliability, performance and thermal stability limitations are due to the bare MoS_2 channel and its interaction with adsorbates. As for the CaF_2 insulator, we show that it contains a very small number of defects and starts to degrade only under extreme electrical overloads above 7 MV cm^{-1}, which is far above the requirements for normal operation of our devices. The results provide additional confirmation that CaF_2 is a very promising insulator for 2D electronics.

1. CaF_2/MoS_2 devices

Our devices are back-gated bilayer MoS_2 FETs with a channel grown by chemical vapour deposition (CVD) [49] and transferred onto the CaF_2/Si(1 1 1) substrates using the method presented in [50]. CaF_2 films of about 6–7 monolayers (ML, 1 ML =0.315 nm) have been grown on atomically clean Si(1 1 1) surface using our established MBE process [51], which is a fully scalable technology. The thickness of CaF_2 was confirmed to be about 2 nm using transmission electron microscope (TEM) [30]. The source/drain contact pads are made of Ti/Au and the channel lengths and widths are between 400 and 800 nm for different devices (see more details in the methods section).

The schematic channel cross-section of our CaF_2/MoS_2 FETs is shown in figure1(a). As the layered structure of CaF_2 with its F-Ca-F monolayers is rather similar to that of 2D materials, the interface with MoS_2 is well-defined and contains a quasi van der Waals gap [33]. Most importantly, a F-terminated atomically flat surface does not provide any dangling bonds, which are typically present in 2D FETs with amorphous oxides. In figure 1(b) we show the scanning electron microscope (SEM) image of our devices which consist of two contact pads connected to the MoS_2 channel in between. We fabricated two sets of devices on nearly identical CaF_2/Si(1 1 1) substrates but with MoS_2 films of differently adjusted CVD growth processes. Namely, in our first CVD growth experiments (Process 1) the control of the sulfur concentration in the chamber was limited, and during the next experiments (Process 2) this has been considerably improved. As shown by atomic force microscope (AFM) images in figure 1(c), the quality of the Process 1 MoS_2 films is considerably lower than that of Process 2. This appears in nearly ten times larger grain sizes of MoS_2 in Process 2, which is known to be an important figure of merit for the quality of CVD-grown films [52–54]. Namely, the film with the larger grain size contains less grain boundaries, which leads to a smaller number of intrinsic defects and improved electrical properties. In figure 1(d) we compare the gate transfer ($I_D - V_G$) characteristics of two best (among few tens) devices fabricated using both processes. In agreement with the results of [53], by using MoS_2 films of Process 2 we achieve more competitive devices with a maximum measured on current of about 5 μA (or about 6 μA μm^{-1} if normalized to the channel width), which is two orders of magnitude larger than for the best Process 1 FET. This is likely

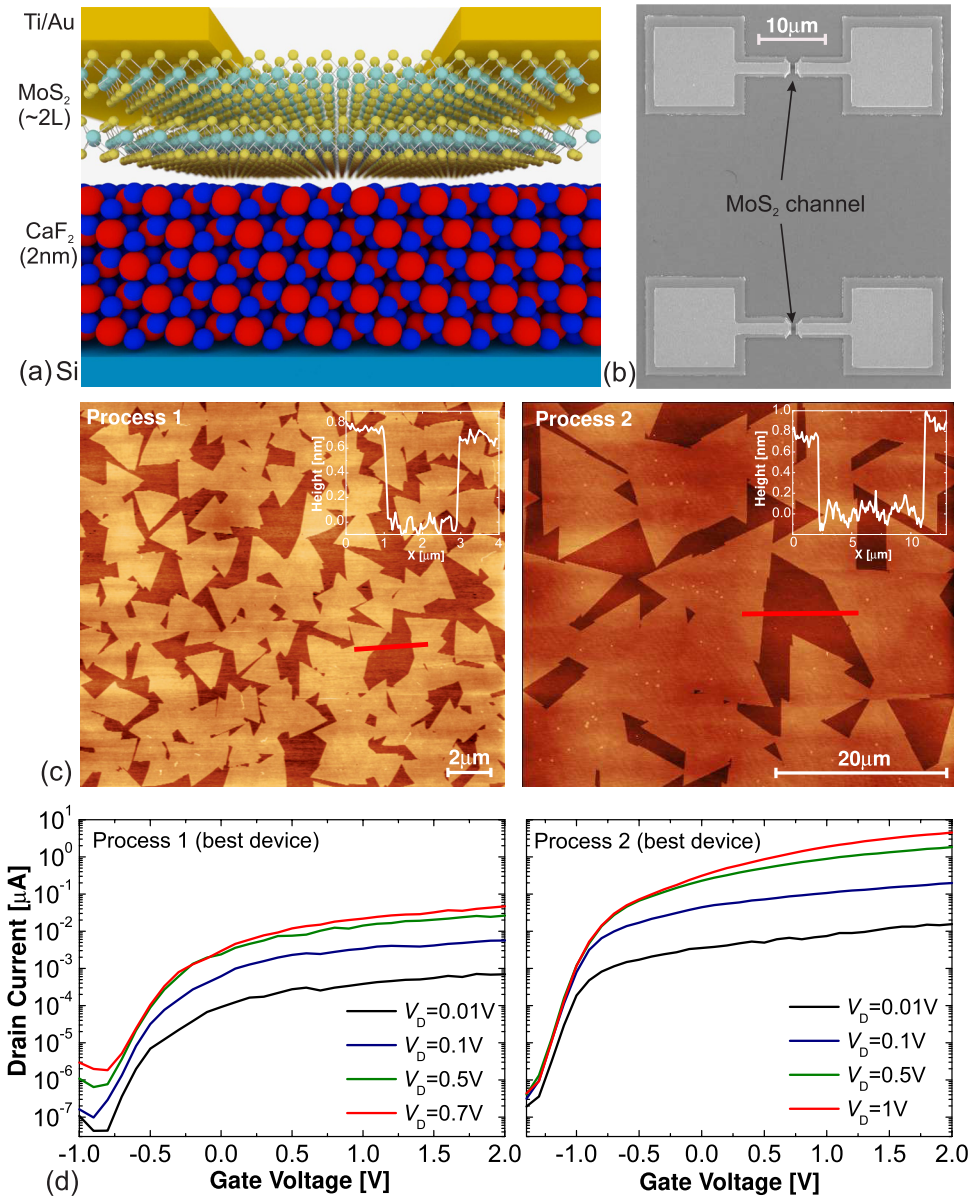

Figure 1. (a) Atomistic structure of the channel area of our CaF_2/MoS_2 FETs with the quasi van der Waals interface between F-terminated CaF_2(1 1 1) and MoS_2. (b) SEM image of two devices. (c) AFM images of the MoS_2 films grown by CVD on sapphire obtained from the substrate areas where the growth remains in the nucleation stage and the film is not formed completely. The insets show height profiles measured along the red lines, indicating monolayer structure of triangular MoS_2 grains. For a more optimized growth (Process 2) MoS_2 grains are nearly ten times larger than those of Process 1, which results in a considerable improvement of the film quality. Note that in the areas with continuous MoS_2 layer the grains are slightly smaller for both processes [30]. (d) The $I_D - V_G$ characteristics of the two best devices fabricated using both processes from several tens each. The device with the MoS_2 channel of Process 2 exhibits a considerably better performance.

because with channel dimensions between 400 and 800 nm, some devices are located relatively far away from the grain boundaries of 10–15 μm sized MoS_2 grains, which is barely possible for the Process 1 films with MoS_2 grains of only about 1 μm.

2. Results and discussion

In figure 2 we compare the performance characteristics of the best FETs at different drain voltages. For the Process 2 devices the best values of the on/off current ratio, field-effect mobility and SS are respectively 10^7, 0.7 $cm^2 V^{-1}s^{-1}$ and 93 mV dec^{-1}, which is considerably better than the maximum values of their Process 1 counterparts. At the same time, the performance of the Process 1 device starts to degrade already for V_D above 0.1 V, while the Process 2 device reaches the performance maximum at higher V_D. Since both devices were fabricated using nearly identical CaF_2 layers, all these results allow us to conclude that, owing to a defect-free nature of CaF_2 surface, in our CaF_2/MoS_2 FETs the major performance limitations are coming from the quality of the MoS_2 channel. Especially strong improvement is achieved in SS, which is mainly degraded by defects in the MoS_2 channel. Therefore, for CaF_2/MoS_2 FETs with defect-free MoS_2 films we expect SS to be more close to 60 mV dec^{-1}.

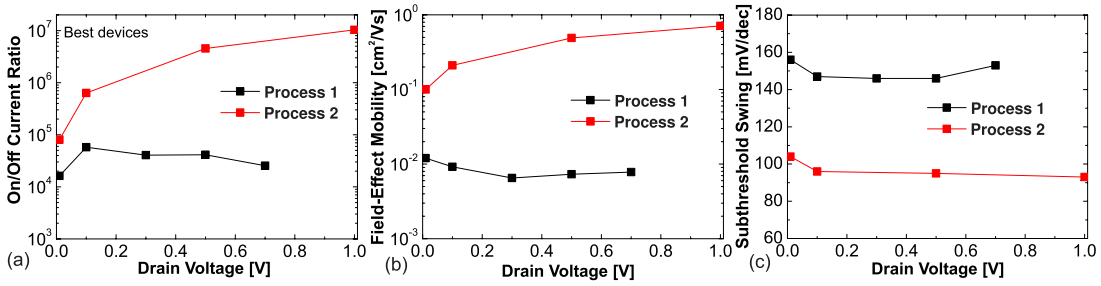

Figure 2. The on/off current ratio (a), field-effect mobility (b) and subthreshold swing (c) of the devices from figure 1(c) versus the drain voltage. For the device from Process 2 all values are considerably better. An increase of the on/off current ratio versus V_D confirms both the high quality of the MoS_2 channel, which allows to achieve a high degree of current control, and good insulator properties of CaF_2, which suppress the gate leakage even for higher V_D.

Next we proceed with the reliability characterization of Process 1 transistors. From about fifty of these devices, not more than five exhibited a distinctively better performance. As shown in figure 3, the best CaF_2/MoS_2 FETs fabricated using small grain MoS_2 films already exhibit a competitive reliability. For instance, the hysteresis width in these devices does not exceed 0.15 V (figure 3(a)) even for sweep times t_{sw} of several kiloseconds. As suggested previously [21], we normalize the hysteresis widths measured using different t_{sw} by the insulator field factor $K = \Delta V_G/d_{ins}$, with ΔV_G being the width of the sweep range and d_{ins} the insulator thickness, and plot them versus the measurement frequency $f = 1/t_{sw}$. As shown in figure 3(b), the hysteresis in our CaF_2/MoS_2 FETs is smaller than that of SiO_2(25 nm)/MoS_2 transistors reported in our previous work [6]. This is quite remarkable since in the latter devices the MoS_2 films were grown directly on the SiO_2 substrate [55] and were thus of much higher quality [7] with grain size exceeding 100 μm. Also note that these reference devices used a high-quality Al_2O_3 encapsulation which has been shown to reduce the hysteresis width.

The small hysteresis observed is fully consistent with the weak positive BTI (PBTI) degradation seen in these devices. In figures 3(c) and (d) we show that even after PBTI stress at a gate voltage of $V_S = 1.5$ V (corresponding to an insulator field of 7.5 MV cm^{-1}) the degradation is fully recoverable within a maximum tens of seconds. This is in contrast to encapsulated SiO_2/MoS_2 FETs, where the recovery at a certain recovery voltage V_R takes up to a kilosecond after a weaker 4.8 MV cm^{-1} stress (figure 3(d)). The latter suggests that while in SiO_2/MoS_2 FETs with its amorphous oxide charge trapping is due to oxide defects with widely distributed time constants [56], in crystalline CaF_2 a similar distribution of defects is missing. As such, in CaF_2/MoS_2 devices the main contribution likely comes from the defects in MoS_2 and adsorbates (e.g. water molecules) bonded at the CaF_2/MoS_2 interface, which are known to be very fast [42]. However, stressing of CaF_2 at even higher electric fields (up to 15 MV cm^{-1}) sometimes leads to activation of other failure mechanisms, which are also present in MoS_2 FETs with about 4 nm thick hBN insulators and in our Process 2 devices with CaF_2 (see figures S1–S3 in the supporting information (SI) (stacks.iop.org/TDM/6/045004/mmedia)). These issues are likely associated with the creation of new defects in tunnel-thin gate insulators subjected to strong electrical stress and not related to the channel quality.

In order to further understand the impact of the MoS_2 channel quality on the performance and reliability of our CaF_2/MoS_2 FETs, we analyze more typical devices of Process 1. In contrast to the best devices, these devices likely contain several grain boundaries within their channel, which results in degraded performance. As shown in figure 4(a), in typical Process 1 devices a considerable hysteresis is observed. Although this hysteresis is not sizably reduced at $T = 100$ °C, no increase is observed either. This would be in contradiction with thermally activated charge trapping by insulator defects and suggests that the contribution comes from adsorbates interacting with channel defects [41], which serve as energetically favorable attachment sites. These channel defects are likely S vacancies, which in these devices should be mostly concentrated near the grain boundaries [57]. At the same time, the hysteresis considerably increases after 5 h at $T = 100$ °C. Also, we observe a transformation of the $I_D - V_G$ characteristics and a negative shift of the threshold voltage V_{th}, which can be explained by thermally enhanced creation of S vacancies in MoS_2 [57–59] (for more details about the measurement history of this device see figure S4 in the SI). These S vacancies can be created either by chemical reaction of bare MoS_2 with residual H_2 in the vacuum chamber [58] or by intrinsic mechanism catalyzed by the grain boundaries, which can be involved in complex reaction pathways [57]. As such, we identify the interaction of preexisting and newly created S vacancies in MoS_2 with adsorbed water molecules [41] as the most possible reason for the hysteresis. As was reported previously [41], the typical time constants of these processes are tens of seconds. While being consistent with our results (figure 4), these values are considerably larger than the time constants of a direct charge trapping of carriers by channel defects, which therefore can not contribute to the

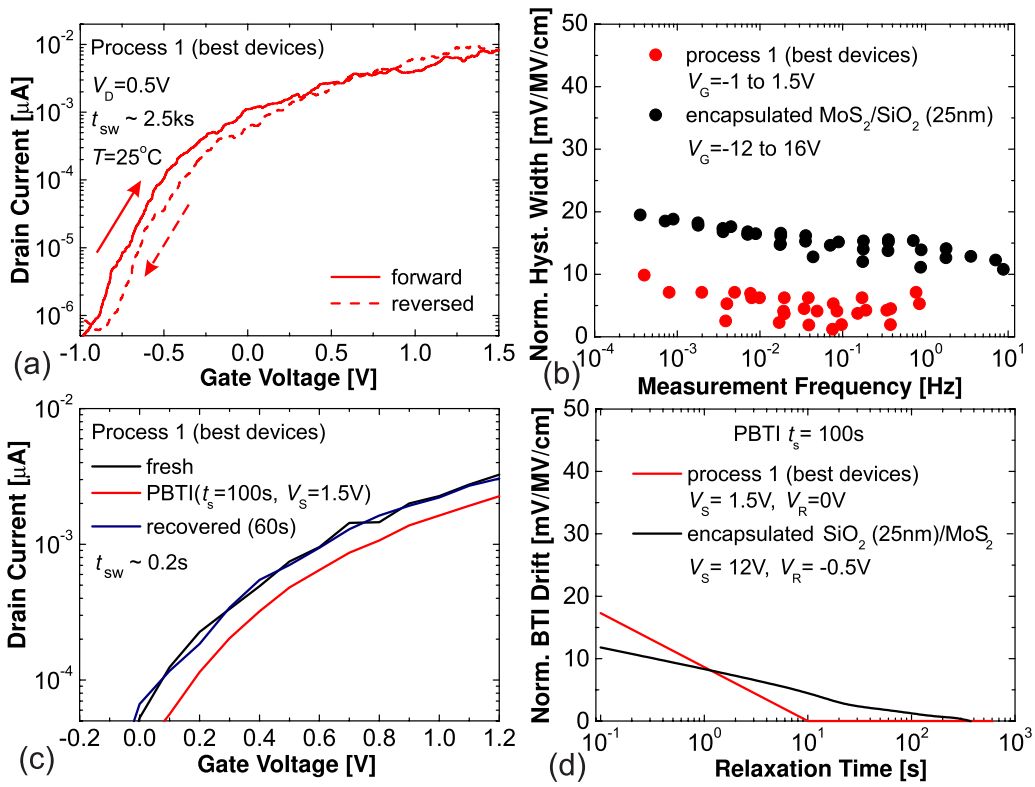

Figure 3. (a) The slow sweep $I_D - V_G$ characteristic measured for one of the best Process 1 devices. (b) The normalized hysteresis widths for our bare channel CaF_2/MoS_2 FETs are even smaller than for Al_2O_3 encapsulated SiO_2/MoS_2 FETs reported in our previous work [6]. (c) The fast sweep $I_D - V_G$ characteristics measured before and after a $t_s = 100$ s PBTI stress. (d) In contrast to SiO_2/MoS_2 FETs, the degradation is completely recoverable already within the first ten seconds. The measured BTI drifts are normalized by the insulator fields.

hysteresis and BTI [42]. Interestingly, air exposure of a previously baked device for several minutes leads to an improvement of the device performance and suppression of the hysteresis, which suggests that created S vacancies become substituted (e.g. by oxygen atoms [60]) and thus excluded from the processes causing the hysteresis.

In figure 4(b) we show the hysteresis width plotted versus the measurement frequency as measured for a baked device prior to air exposure. We observe a clear maximum as predicted in our previous work [21], where a similar behaviour has been also observed for MoS_2 FETs with hBN insulators. While this feature has been also predicted for charge trapping by oxide defects [21], for oxide/2D FETs the maximum is typically not observable in experiments because of the very broad distribution of time constants. In contrast, the interaction of MoS_2 (and probably hBN [21]) defects with adsorbates should be a much faster process compared to charge trapping by slow oxide traps, which leads to a clear maximum already at moderate sweep frequencies. Interestingly, a decrease of the hysteresis width for slow sweeps is accompained by a strong transformation of the $I_D - V_G$ characteristics (see figure S5 in the SI). After baking this issue is observed even for the best devices discussed above, which indicates an overall poor thermal stability of the MoS_2 film with small grain size (see figure S6 in the SI).

PBTI and negative BTI (NBTI) in these devices appear to be due to the same fast MoS_2 defects as the hysteresis. In figures 4(c) and (d) we show that the dynamics of these issues are dominated by the fast trapping component, which is rather strong (especially after baking) but tends to recover completely even after a 10 MV cm^{-1} stress for 10 ks. Following the work of [41], we suggest that during NBTI stress (or negative V_G during the hysteresis sweep) the S vacancies become occupied by positive H^+ ions of water molecules, and during PBTI (or positive V_G during the hysteresis sweep) by negative O^{2-} ions. As soon as the stress is removed, the number of S vacancies occupied by O^{2-} and H^+ ions quickly returns to the equilibrium at the recovery voltage $V_R = 0$.

We proceed with the analysis of the reliability of our Process 2 CaF_2(2 nm)/MoS_2 FETs and compare our results with those obtained for sandwiched hBN/MoS_2/hBN devices with exfoliated channel and gate insulator thickness of about 4 nm. In figure 5(a) we show that the hysteresis in both devices is negligible even for kilosecond sweep times, while the performance of the devices with CaF_2 is considerably better (for more details see figure S1 in the SI). At the same time, a more negative threshold voltage of the devices with CaF_2 is likely because of their bare channel, which allows accumulation of positive fixed charges (e.g. adsorbates on top of the channel or passive S vacan-

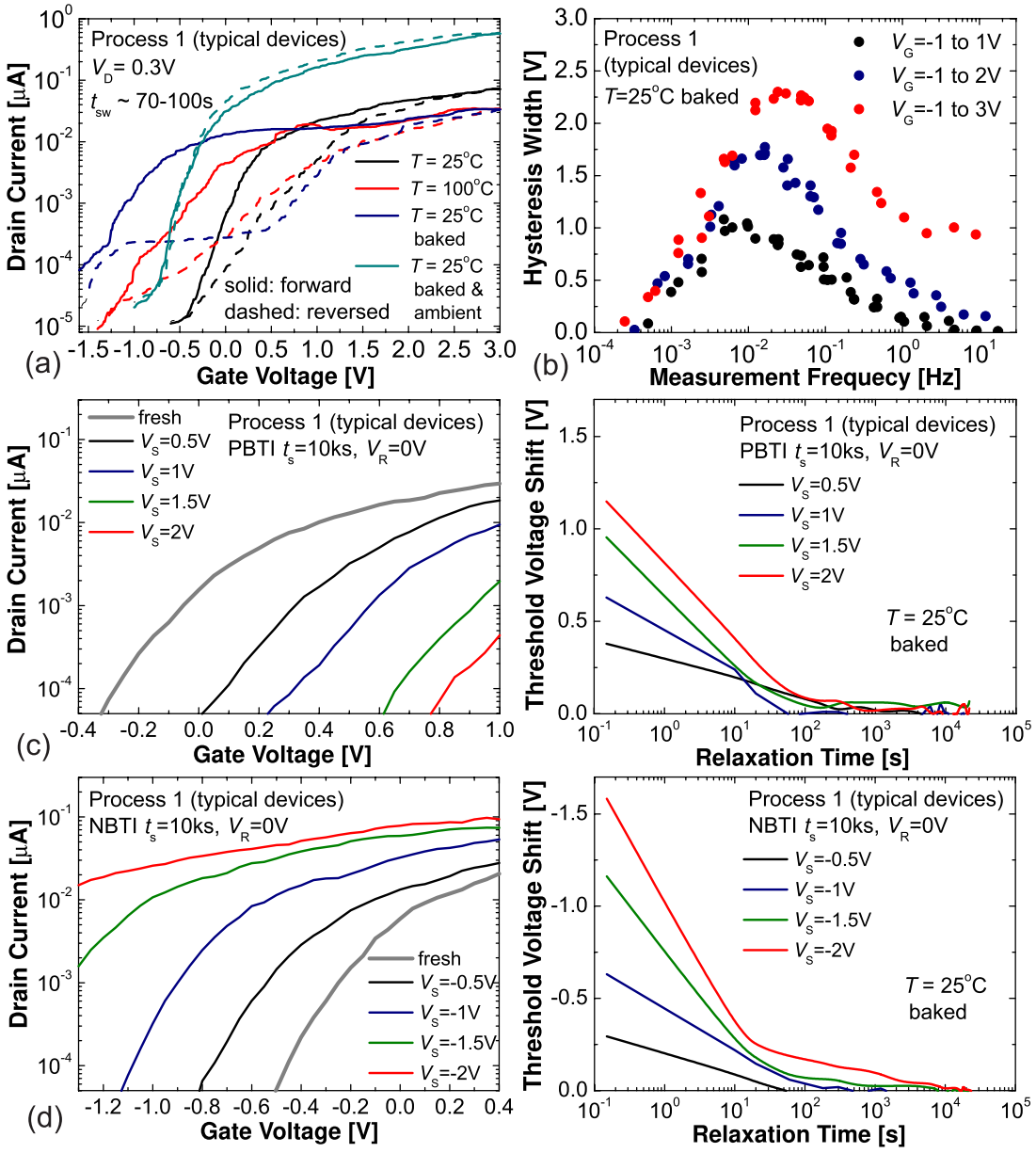

Figure 4. (a) The $I_D - V_G$ characteristics measured for a typical Process 1 device before, during and after baking at $T = 100$ °C. The hysteresis increases after baking and becomes suppressed by subsequent ambient exposure. (b) The hysteresis width measured after baking at $T = 100$ °C exhibits a clear maximum versus f. (c) Evolution of the $I_D - V_G$ characteristics after subsequent PBTI stresses with increasing V_S and corresponding recovery traces. (d) Related results for NBTI measured on the same device. In both cases the degradation is dominated by fast defects which are likely located in MoS_2 and interact with water adsorbates.

cies). As shown in figure 5(b), the hysteresis in our CaF_2/MoS_2 FETs is not observed even for faster sweeps, while the device with hBN exhibits some signs of fast trap contribution which agrees well with our previous observations [21]. These results confirm the high quality of both the CaF_2/MoS_2 interface and the large grain MoS_2 film of our Process 2.

In figure 5(c) we show the evolution of the $I_D - V_G$ characteristics of our Process 2 devices under different bias stress conditions. If the applied insulator field is less than 5 MV cm^{-1}, both NBTI and PBTI degradations are weak. This further confirms the defect-free nature of the CaF_2/MoS_2 interface and the absence of active fast defects in the Process 2 MoS_2 films, which is different from their Process 1 counterparts discussed above. However, a PBTI stress at 7.5 MV cm^{-1} leads to a recoverable negative shift of the threshold voltage, which can be attributed to the creation of new defects in CaF_2 while approaching the typically assumed breakdown field of about 10 MV cm^{-1}. As soon as the insulator field and/or the stress time are further increased, this kind of degradation becomes stronger and is also observed to be weakly recoverable (see figures S2 and S3 in the SI). However, the insulator fields and stress times required to observe such a negative shift can be different for different devices and are likely given by the local CaF_2 thickness and quality. A similar degradation with a negative shift after PBTI stress has been observed also for our devices with Process 1 MoS_2 films and hBN(~4 nm)/MoS_2/hBN FETs.

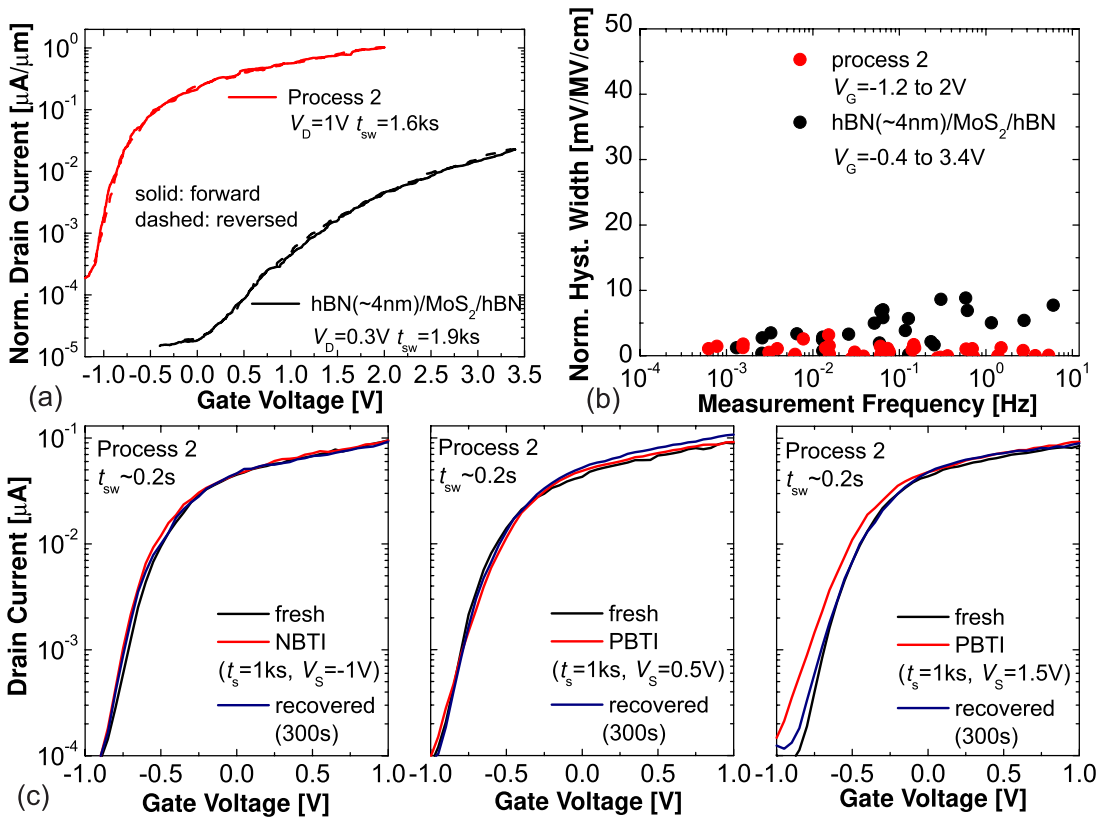

Figure 5. (a) The $I_D - V_G$ characteristics of our Process 2 CaF_2(2 nm)/MoS_2 and hBN(~4 nm)/MoS_2/hBN FETs (I_D is normalized by the channel width) exhibit a negligible hysteresis even for kilosecond sweep times. (b) The hysteresis widths normalized by the insulator field factor are also small for both technologies, though some fast traps are likely present in the hBN layer. (c) BTI degradation and recovery in our Process 2 CaF_2(2 nm)/MoS_2 FETs. NBTI stressing at $V_S = -1$ V (insulator field of -5 MV cm^{-1}) and PBTI at $V_S = 0.5$ V (insulator field of 2.5 MV cm^{-1}) result in negligible degradation. PBTI at $V_S = 1.5$ V (insulator field of 7.5 MV cm^{-1}) causes a small negative shift of the device characteristics, which is fully recoverable at $V_R = -0.5$ V.

This allows us to conclude that this issue is common for all devices with scaled gate insulators. Remarkably, CaF_2 appears to be more stable with respect to strong electrical stress than hBN (see figure S3 in the SI). It is worth noting that the results of figure 5 are the closest to the reliability thresholds expected for mature CaF_2/MoS_2 FETs, while figures 3 and 4 show that the potential of these devices can be concealed by the dominating impact of channel defects and adsorbates. The latter can be addressed by further improvement of the MoS_2 growth techniques and the use of suitable encapsulation schemes.

Next we examine the thermal stability of our Process 2 CaF_2/MoS_2 FETs. Similarly to their Process 1 counterparts, at high temperature these devices exhibit a negative shift of V_{th} (figure 6(a)). After 14 h at 165 °C, V_{th} becomes more close to the critical stress voltages allowed for 2 nm CaF_2 films, and partially recovers when the temperature is returned to 25 °C. This negative V_{th} shift is very similar to that studied previously in our SiO_2(25 nm)/MoS_2 FETs [6, 61] (figure 6(b)). The latter devices have been baked even at 300 °C, which was possible due to the more stable MoS_2 films with 100 μm grain size (against 10–15 μm in our Process 2) grown by CVD directly on top of the SiO_2 substrate [7, 55]. As has been shown for the SiO_2/MoS_2 devices (see figure S7 in the SI), a weakly recoverable negative shift of V_{th} is a typical feature of bare channel devices. In contrast, encapsulated devices exhibit a fully reversible transformation of the $I_D - V_G$ characteristics at higher temperatures. This further confirms that the origin of this negative shift is the creation of S vacancies acting as positive charges, which might be more efficient when bare MoS_2 is interacting with the environment of the vacuum chamber [58, 59] and catalyzed by the grain boundaries [57].

Nevertheless, baking of our Process 2 devices does not lead to a considerable increase of the hysteresis (figure 6(c)). One possible reason for this is that in large grain size MoS_2 films the penetration of adsorbates to the CaF_2/MoS_2 interface is less efficient, owing to the lack of grain boundaries. As such, newly created S vacancies are not able to interact with these adsorbates as described in [41] and remain passive, which is very different from Process 1 devices with small grain MoS_2 films. On the other side, channel defects are known to be very fast to contribute to the hysteresis by direct charge trapping of carriers [42]. As a result, in baked Process 2 devices the normalized hysteresis is nearly an order of magnitude smaller than in their SiO_2(25 nm)/MoS_2 counterparts (figure 6(d)). This is despite the fact that the overall quality of the directly grown MoS_2 with at least 100 μm grains used in the latter case is obviously better [7], which is confirmed by the absence of

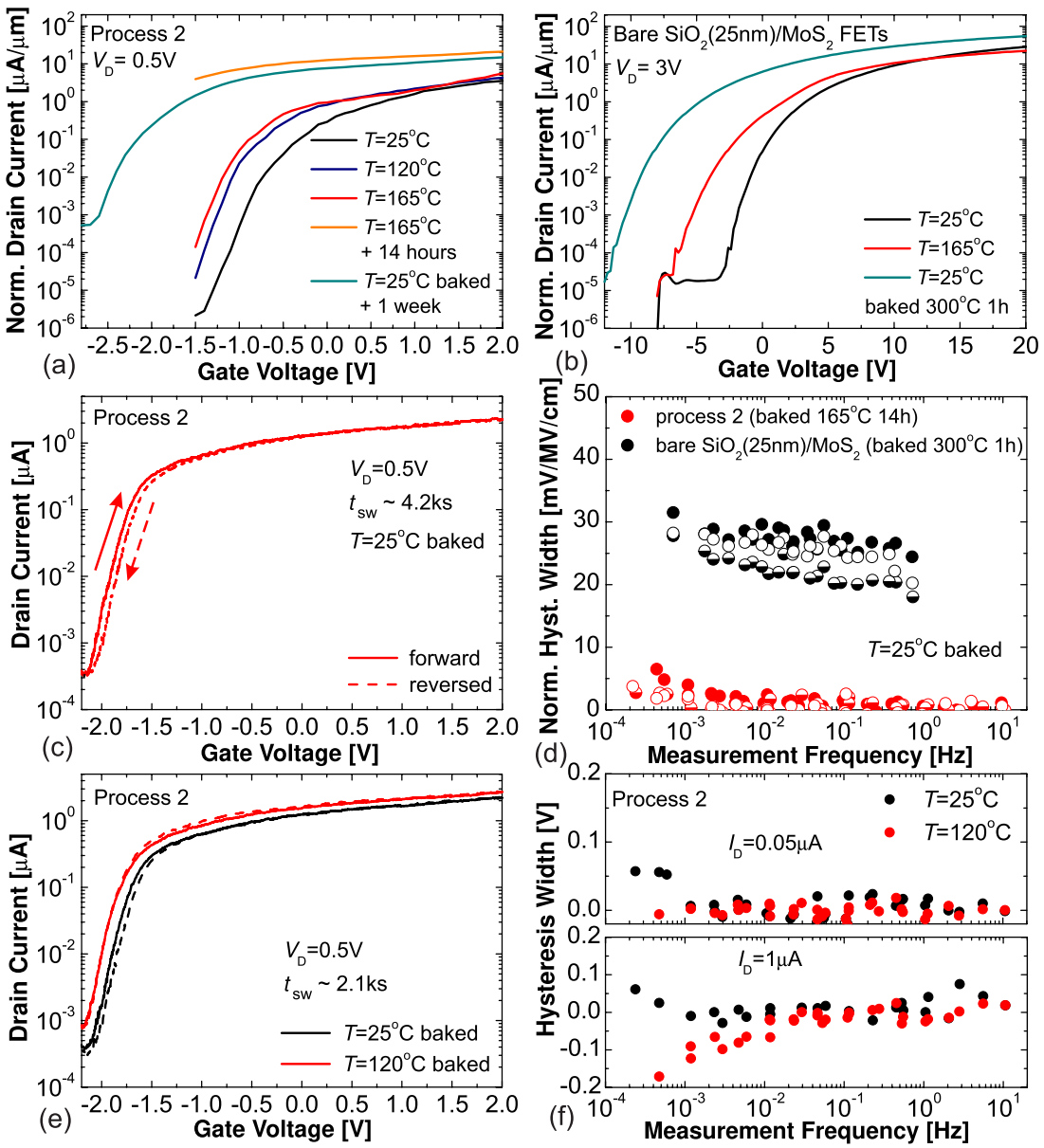

Figure 6. Evolution of the $I_D - V_G$ characteristics of our Process 2 CaF_2(2 nm)/MoS_2 FETs (a) and bare channel SiO_2(25 nm)/MoS_2 FETs [6, 61] (b) during and after high temperature treatment (I_D is normalized by the channel width). In both cases a negative threshold voltage shift is observed. (c) For the Process 2 devices the hysteresis remains small even after baking at 165 °C. (d) The hysteresis widths normalized by the insulator field factor for our Process 2 devices with CaF_2 are considerably smaller than for bare channel SiO_2(25 nm)/MoS_2 FETs. For both technologies the measurements have been performed on baked devices with negatively shifted V_{th}, and the results for three different devices are plotted. (e) Subsequent heating of baked Process 2 devices up to 120 °C leads to switching of the hysteresis towards the counterclockwise direction. (f) While the standard clockwise hysteresis around V_{th} becomes annealed (top), the counterclockwise hysteresis appears for slower sweeps and starts to be localized above V_{th} (bottom).

the fast trapping issues discussed above for our Process 1 devices even after baking at 300 °C. This allows us to conclude that even in bare channel devices the hysteresis dynamics may be strongly dependent on the gate insulator used. At the same time, virtually defect-free crystalline CaF_2 is superior compared to amorphous SiO_2 with its numerous oxide defects, which makes devices with CaF_2 more competitive even if the MoS_2 growth process is less optimized.

Finally, we examine the temperature dependence of the hysteresis in our Process 2 CaF_2/MoS_2 devices. As shown in figure 6(e), subsequent heating of baked devices up to 120 °C leads to a switching of the hysteresis from clockwise towards counterclockwise, which becomes more pronounced at 165 °C (see figure S8 in the SI) until the device fails at slower sweeps. This is again similar to our observations on bare channel SiO_2/MoS_2 FETs [61]. Since in the latter devices this issue was found to be suppressed after encapsulation (see figure S8 in the SI), we suggest that counterclockwise hysteresis observed at higher temperatures originates from thermally and bias enhanced chemical interaction between bare MoS_2 channel and the environment. For instance, one possible reason might be the creation/substitution of S vacancies, though this requires further investigation. In fact, the clockwise hysteresis observed around V_{th} at 25 °C completely disappears at 120 °C and becomes substituted by the counter-

clockwise hysteresis localized above V_{th} (figure 6(f)). Annealing of the clockwise hysteresis with no thermal activation further confirms that this issue is mostly due to adsorbates attached to the CaF_2/MoS_2 interface, even though in Process 2 devices their concentration is rather small. At the same time, the absence of slow thermally activated charge trapping in CaF_2 prevents non-volatile memory switching [62] of the hysteresis at higher temperatures, which is also known for our previously studied bare channel SiO_2/MoS_2 FETs [61] (see figure S8 in the SI). Namely, in devices with CaF_2 this switching is substituted by simple counterclockwise hysteresis at higher temperatures, owing to no interplay between different hysteresis mechanisms.

3. Conclusions

We have reported a detailed performance and reliability study of bilayer CVD-grown MoS_2 FETs with only 2 nm thick crystalline CaF_2 insulators. We have found that in these devices the hysteresis and long-term drifts of the gate transfer characteristics are mainly due to fast intrinsic defects in the MoS_2 channel interacting with adsorbates, while the CaF_2 insulator itself contains much lower amount of defects. As a result, we have demonstrated that the performance, reliability and thermal stability of devices with CaF_2 strongly depend on the quality of the MoS_2 channel which is directly related to the grain size of the film. We also compared our results for CaF_2/MoS_2 FETs with our previous observations on MoS_2 devices with SiO_2 and hBN. This allowed us to clearly show that crystalline CaF_2 is currently the most promising insulator for 2D devices. On the other side, the major performance- and reliability-related limitations of CaF_2/MoS_2 FETs can be addressed by using higher quality MoS_2 films and protecting them with suitable encapsulation layers. Finally, for the first time we observed a special degradation mechanism which arises in devices with tunnel-thin gate insulators and found that CaF_2 outperforms hBN with respect to this issue as well. As such, we conclude that our CaF_2/MoS_2 FETs present a route towards competitive and fully scalable 2D nanoelectronics.

4. Methods

4.1. Device fabrication

Fabrication of our devices consists of MBE growth of 2 nm thick CaF_2 films, CVD growth of bilayer MoS_2, transfer of the MoS_2 films onto the CaF_2 surface and e-beam lithography steps to shape the devices.

CaF_2 layers were grown on n-Si(1 1 1) substrates with $N_D = 10^{15}$ cm^{-3} and small miscut (5 to 10 angular minutes). These substrates were carefully cleaned by using a chemical treatment. Then, a protective oxide layer was formed using the method of Shiraki [63] and subsequently removed by annealing for 2 min at 1200 °C under ultra-high vacuum conditions ($\sim 10^{-8}$–10^{-7} Pa). After this, the CaF_2 film was grown on this atomically clean 7 × 7 Si(1 1 1) surface using an MBE process with the optimal growth temperature of 250 °C and deposition rate of about 1.3 nm min^{-1}. The crystalline quality of the formed CaF_2 layers was examined using reflection high-energy electron diffraction (RHEED) [64] with an electron energy of 15 keV.

Bilayer MoS_2 films were grown on c-plane sapphire substrates using the CVD process of [49] with sulfur and MoO_3 as powder precursors and ultra-high-purity Ar as the carrier gas. The growth was performed at atmospheric pressure and a temperature of 750 °C. While adjusting the control of the sulfur concentration in the reaction chamber during growth, we obtained two different kinds of MoS_2 films. These are the Process 1 MoS_2 films, which are one of the first grown using this setup, and Process 2 films obtained already after some tuning of the control of the sulfur concentration. At the nucleation stage Process 1 films were found to consist of relatively small grains of about 1–2 μm, while in the Process 2 films the grain size was about 10–15 μm indicating a better quality. As soon as the layer is formed completely, the grain size in both cases becomes slightly smaller [30].

In order to shape the devices, we applied several e-beam lithography steps. First we sputtered 15–20 μm sized SiO_2(5–10 nm)/Ti/Au contact pads for the probes, with this additional SiO_2 layer required to minimize possible parasitic leakage currents. After this, 7 × 7 mm MoS_2 film was transferred onto the CaF_2/Si(1 1 1) substrate using a polystyrene film as a carrier polymer which was then dissolved in toluene, following the method of [50]. The transferred MoS_2 film was subsequently etched by reactive ion etching, in order to define the channels with L and W varied between 400 and 800 nm. Finally, the channels were contacted by e-beam evaporated Ti/Au pads deposited on top of MoS_2 in pre-shaped contact areas. This second layer of Ti/Au was slightly extended out of the first metal layer to contact MoS_2 on top of the bare CaF_2 surface in order to finally shape MoS_2 FETs with 2 nm CaF_2 gate insulator.

4.2. Electrical characterization

Electrical characterization of our CaF_2/MoS_2 FETs consisted in the measurements of the performance parameters, hysteresis and long-term BTI drifts of the $I_D - V_G$ characteristics. These measurements were performed using a Keithley 2636 parameter analyzer in the chamber of a Lakeshore probestation either in a vacuum ($\sim 5 \times 10^{-6}$ Torr) or in ambient conditions, in complete darkness and at temperatures ranging from 25 °C to 165 °C. When characterizing the device performance, we used the autorange measurement

mode to correctly resolve the on/off current ratio. The hysteresis of the $I_D - V_G$ characteristics was studied using our established measurement technique [21] based on double sweeps with varied sweep times. For a convenient comparison of the data for different devices and measurement conditions, we plot the extracted hysteresis widths versus the measurement frequency $f = 1/t_{sw}$, with t_{sw} being the total sweep time, and normalize them by the insulator field factor $K = \Delta V_G/d_{ins}$, where ΔV_G is the width of the sweep range and d_{ins} is the insulator thickness. The BTI drifts were measured using subsequent stress/recovery rounds with fast ($t_{sw} \sim 0.2$ s) $I_D - V_G$ sweeps performed at different recovery stages [21, 45]. We express the obtained results using the recovery traces of the threshold voltage shift versus the relaxation time. For convenient comparison of the results for different devices, we normalize the measured threshold voltage shifts by the stress insulator fields.

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Competing interests

The authors declare no competing interests.

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