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Engineering Field Effect Transistors with 2D Semiconducting Channels: Status and Prospects

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The continuous miniaturization of field effect transistors (FETs) dictated by Moore's law has enabled continuous enhancement of their performance during the last four decades, allowing the fabrication of more powerful electronic products (e.g., computers and phones). However, as the size of FETs currently approaches interatomic distances, a general performance stagnation is expected, and new strategies to continue the performance enhancement trend are being thoroughly investigated. Among them, the use of 2D semiconducting materials as channels in FETs has raised a lot of interest in both academia and industry. However, after 15 years of intense research on 2D materials, there remain important limitations preventing their integration in solid-state microelectronic devices. In this work, the main methods developed to fabricate FETs with 2D semiconducting channels are presented, and their scalability and compatibility with the requirements imposed by the semiconductor industry are discussed. The key factors that determine the performance of FETs with 2D semiconducting channels are carefully analyzed, and some recommendations to engineer them are proposed. This report presents a pathway for the integration of 2D semiconducting materials in FETs, and therefore, it may become a useful guide for materials scientists and engineers working in this field.

1. Introduction

The field effect transistor (FET) is the most important electronic device in modern integrated circuits for information processing and storage[1,2] and modern electronic chips contain billions of FETs per square millimeter.[3] An FET is an electronic device with four terminals (i.e., gate, drain, source, and bulk; see **Figure 1**a), in which the current flowing between drain and source (I_{DS}) can be controlled by tuning the voltage between gate and bulk (V_G). Mass-production of FETs started in the late 1970s using silicon-related materials, i.e., a polysilicon gate, silicon dioxide (SiO_2) as a gate dielectric, and silicon as the channel material in the bulk.[4,5] The adjustment of I_{DS} is caused by the modulation of the electrical resistance of the Si material between the drain and source electrodes due to the electrical field generated by V_G, which forms a channel of minority charge carriers in the Si material right beneath the gate dielectric. The main figures of merit of an FET are the transfer characteristic (I_{DS} vs V_G, for a specific V_{DS}; see Figure 1b) and the output characteristic (I_{DS} vs V_{DS}, for various V_G; see Figure 1c). From the transfer characteristic one can extract several important operational parameters of the FET:

i) The OFF state current (I_{OFF}), which should be as low as possible to minimize standby power consumption, and the ON state current (I_{ON}), which should be high to ensure enough power supply to the circuitry connected at the output.[1,6]
ii) The current ratio between ON and OFF states (I_{ON}/I_{OFF}), which in switches for digital logic applications is required to be larger than 10^5.[6–8]

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iii) The threshold voltage (V_{th}), which is the value of V_G at the transition from OFF state to ON state in the transfer characteristic.[1,6]

iv) The subthreshold slope (SS), which is the slope of the log-linear regime of the transfer characteristic in the subthreshold region. This parameter can be calculated using Equation (1)

$$SS = \frac{d(\log I_{DS})}{dV_G} = \left[\frac{dV_G}{d(\log I_{DS})}\right]^{-1} \quad (1)$$

Its inverse value (S = 1/SS), called subthreshold swing, is also often used in the literature. Both of them indicate how well the FET can be switched with respect to the applied V_G; a low SS (large S) is desired.

v) The field effect mobility, which is used to estimate the drift velocity of the carriers throughout the channel at a given (relatively low) electric field. Its value can be evaluated using the FET transconductance as shown by Equation (2)[10,11]

$$\mu = \left[\frac{dI_{DS}}{dV_G}\right] \times \left[\frac{L}{WC_G V_{DS}}\right] \quad (2)$$

in which L is the channel length, W is the channel width, and C_G is the capacitance between the channel and the gate per unit area. It is worth noting that the value of C_G may change depending on the structure of the device (see Section 2.2 and **Figure 2**), and this has produced important mobility overestimations in the past.[10,12]

On the other hand, from the output characteristic it is possible to evaluate the quality of the contact between the semiconducting channel and electrodes. Ideally, this contact should be Ohmic in order to facilitate charge transfer, which should be manifested with clear linear dependence of I_{DS} at low V_{DS} in the output characteristic (as displayed in Figure 1c).

The rapid development of modern electronic technologies has been strongly linked to the continuous enhancement of the performance of FETs, which has been mainly related to its miniaturization, according to the Moore's law.[13,14] However, as the scaling down of the FET is reaching nanometric sizes, the devices face fundamental limitations—critical parts of the device cannot scale down below few atoms in length—and some reliability problems (e.g., leakage current[15] and poor heat dissipation[16]) become more and more severe. Consequently, new strategies to enhance their performance are required. Among all of them, the introduction of new materials with better properties (i.e., higher dielectric constant and

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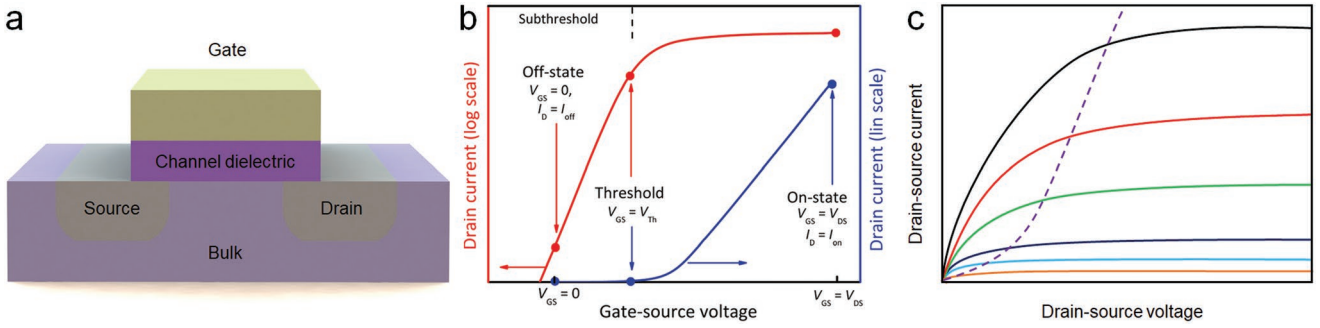

Figure 1. a) Schematic of a traditional FET. b) Typical transfer characteristics (I_{DS} vs V_{GS}) of an n-type 2D material channel FET device. Note that the scale of the red curve is logarithmic and the blue one is linear. Reproduced under the terms and conditions of the Creactive Commons CC BY 3.0 Unported License.[1] Copyright 2015, Royal Society of Chemistry. c) Typical shape of the output characteristics (I_{DS} vs V_{DS}) of an n-type 2D material channel FET device. Saturation of I_{DS} can be observed with larger gate voltage (V_g). Reproduced with permission.[9] Copyright 2018, Royal Society of Chemistry.

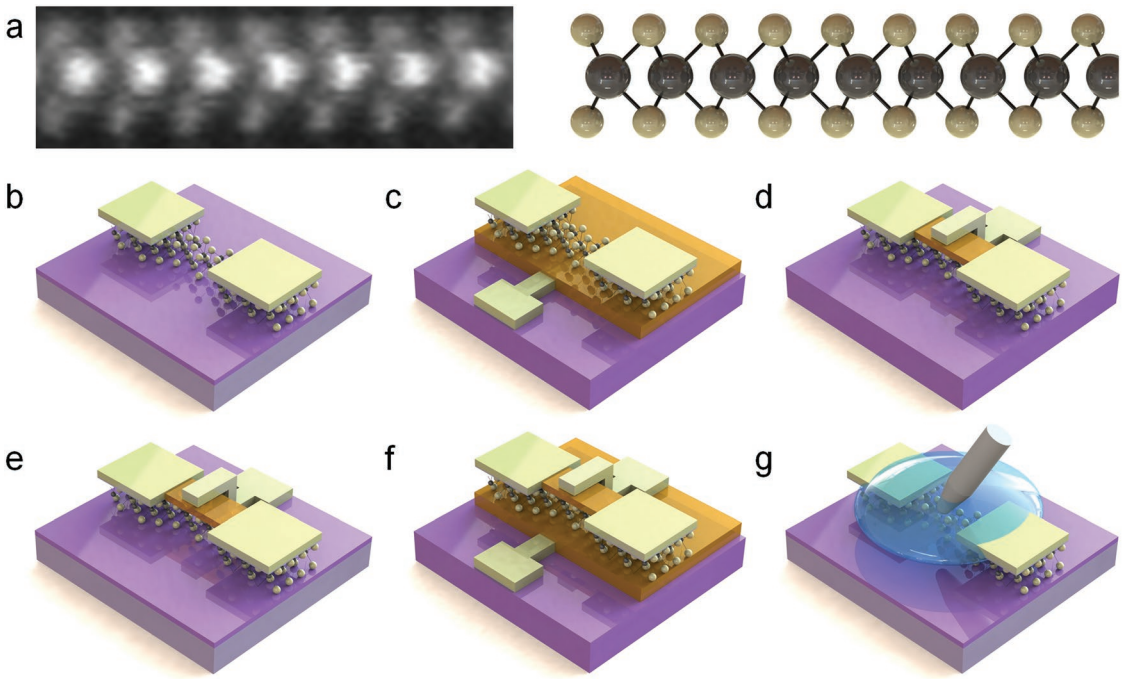

Figure 2. a) Atomic-resolution TEM image of monolayer WSe_2 (2.45 nm × 0.73 nm) and corresponding schematic. Reproduced with permission.[35] Copyright 2018, Springer Nature. Basic 2D material–based FET structures (using MoS_2 as example): b) back-gated FET with Si as gate. Reproduced with permission.[75] Copyright 2016, Elsevier Ltd; c) back-gated FET with manufactured metal gate electrode; d) top-gated FET; dual gate FET structure with Si back gate e) and patterned back gate f); g) liquid-gated FET structure.

larger carriers mobility) appears to be one of the most promising. As an example, in the early 2000 the SiO_2 gate dielectric of FETs became extremely thin, which dramatically increased the leakage currents flowing from/to the gate electrode. This remarkably increased the power consumption of the FETs and, more importantly, reduced their reliability (lifetime).[15] This problem was temporarily mitigated using alternative gate dielectric materials with a higher dielectric constant, which allow generating the same gate capacitance (i.e., necessary to form the channel)[17] using much thicker stacks, contributing to reduce the leakage current orders of magnitude. These materials, referred to as high-*k* dielectrics, have become now the standard in advanced FETs.[18] Another example is the use of materials with higher carrier mobility as channel of the FET (i.e., InSb, InAs, InP, GaAs, and GaN),[19] so that their operation speed can be further enhanced. However, these materials are more expensive and form a poor interface with traditional insulators, and for these reasons thy have still not been implemented in commercial FETs for mass production.

One recent strategy to enhance the performance (i.e., operation speed, I_{ON}/I_{OFF}, and SS) of FETs is the introduction of 2D materials as channel between the source and the drain. This strategy was first proposed in 2004.[20] In that work graphene was synthesized by mechanical exfoliation (repeated peeling) of highly oriented pyrolytic graphite (HOPG), and used as channel in FET devices patterned on 300 nm SiO_2/Si substrates using electron beam lithography (EBL). The devices exhibited remarkably high carrier concentration, high room temperature carrier mobility (3000–10 000 $cm^2\ V^{-1}\ s^{-1}$ for few-layer graphene[20]), and record cutoff frequencies (f_T = 26 GHz)—this is the frequency at which the current gain becomes unity.[21] After that, the mobility of graphene-based FETs was further enhanced to 350 000 $cm^2\ V^{-1}\ s^{-1}$,[22] and nowadays the best values of cutoff frequency reported for such type of devices is 427 GHz.[23] Despite these promising developments, graphene FETs show a very poor I_{ON}/I_{OFF} ratio (<10)[24] due to its absence of a bandgap, which makes their power consumption in standby mode very high.[25]

In 2011, a semiconducting 2D layered material, molybdenum disulfide (MoS_2) was used to fabricate FETs following the same procedure previously used for graphene,[10] and despite the mobility of the resulting devices (2–7 $cm^2\ V^{-1}\ s^{-1}$[12]) was remarkably lower than that of graphene FETs, the currents in standby mode were effectively reduced by up to six orders of magnitude.[10] After this pioneering work, many other groups fabricated FETs using MoS_2 and other 2D semiconductors, most of them from the family of transition metal dichalcogenides (TMDs) with the general formula of MX_2 (being M = transition metal and X = chalcogen) such as $MoSe_2$,[26] $MoTe_2$,[27] WSe_2,[28] and WS_2,[29] and reported cutting-edge device performances. In addition to TMDs, single-element 2D semiconductors such as phosphorene, i.e., black phosphorous (BP) in the single-layer limit, have also been used to fabricate FETs with even higher mobility than 2D-TMDs.[30] Nowadays, MoS_2 FETs exhibiting I_{ON}/I_{OFF} current ratios $>10^9$[31] and subthreshold swings down to 62 mV $decade^{-1}$ for monolayer device[32] have been readily fabricated by many groups. However, so far the mobilities measured in FETs using 2D semiconducting materials are still behind that of Si-based transistors,[1] meaning that it is not expected that this technology can be used for applications that require a higher

mobility. However, FETs with channels made of 2D semiconducting materials can still provide many other exotic properties (e.g., flexibility and transparency) which can make them very attractive for several optoelectronic and straintronic applications.

Despite this progress, developing FETs with channels made of 2D semiconducting materials at wafer level for industrial applications remains a big challenge, due to the complex growth and manipulation of the 2D material, and also due to important reliability problems appeared during device fabrication (e.g., poor interface with other materials). In this paper, the status of FETs with channels made of 2D semiconducting materials is reviewed in depth providing critical opinions on the real usefulness and industrial applicability of the prototypes constructed. In section 2, we review the methods to synthesize the 2D materials and the existing 2D-FET device configurations. Sections 3–6 discuss the effect of electrode/channel contact resistance, dielectric environment, channel length, and channel thickness (respectively) on the performance of the 2D-FETs. Finally, in Section 7 the effect of the temperature is discussed for different channel thicknesses, device structures and dielectric environments.

2. Device Fabrication

2.1. Materials Synthesis

In order to be compatible with typical transistor requirements for logic applications—defined in the technology roadmap for semiconductors (ITRS)[3]—the 2D semiconducting materials implemented as channels in FETs need to have a large enough bandgap (>0.4 eV) and a high carriers mobility (>500 $cm^2\ V^{-1}\ s^{-1}$).[6,33] The synthesis methods used need to ensure large lateral (wafer scale) size, uniform thickness (along the entire wafer) and low density of defects (e.g., $\approx 8 \times 10^{12}\ cm^{-2}$ in MoS_2[34]). Since the first isolation of graphene via mechanical exfoliation in 2004,[20] more and more techniques have been developed to synthesize monolayer and few-layer-thick 2D materials, including liquid phase exfoliation (LPE), chemical vapor deposition (CVD), physical vapor deposition (PVD), and molecular beam epitaxy.

2.1.1. Mechanical Exfoliation

Almost all 2D materials can be obtained by mechanical exfoliation from a raw crystal source, which is formed by particles containing many layers stacked on top of each other. While in each layer the atoms are strongly linked to each other by covalent bonds, the layers adhere to each other by van der Waals forces, which are relatively small. Consequently, these layers can be easily separated (i.e., exfoliated) by applying low mechanical stresses. If this exfoliation process is repeated several times, the thickness of the raw material can be reduced down to a few (<20) layers, and sometimes even to one single layer. It is worth noting that the term 2D used in most literature is not strictly correct when talking about multilayer materials and/or single layer materials with more than one plane, such as WSe_2 in which one layer is formed by three planes that are not vertically aligned (see Figure 2a).[35] However, for consistency with the existing literature, in this review paper all these materials will be encompassed by the term 2D.

Mechanical exfoliation was the first (and is still the most frequently used) method to synthesize 2D materials for fundamental scientific studies. By repeated folding and unfolding of a scotch tape containing the raw material in solid crystal form, the stacked layers can be separated from each other, and when the resulting flakes are thin enough, they can be adhered to the target substrate by applying perpendicular pressure and removing the tape. For TMDs this process can be carried out under normal air atmosphere, but in the case of black phosphorous and other air-sensitive 2D materials a nitrogen glove box or other an environmental chamber filled with another inert gas is required.[36,37] Conventional mechanical exfoliation normally gives rise to contamination on the surface of exfoliated 2D materials, such as the residual polymers from the tape, which can produce undesired performance alterations in the FETs (mobility degradation and hysteresis) during normal operation.[38] So after mechanical exfoliation of 2D materials, some researchers washed the surface of exfoliated 2D materials using acetone (or other solvents) for some minutes or hours[39,40] or thermal annealing.[41]

Although many FET prototypes have been constructed using 2D materials synthesized by this method, the very small lateral size of the flakes (<50 μm) and their inhomogeneous and uncontrollable thicknesses are preventing its industrial use. Apart from the physical limitations, mechanical exfoliation is also a very slow process that requires human labor, which is thus expensive. Therefore, when studying research articles on 2D material–based FETs produced by this method, readers need to be aware that these are fundamental research papers with zero applicability at the industrial level.[42]

In order to fabricate 2D materials at an industrial scale, methods different from mechanical exfoliation are currently under development and their main properties will be summarized in the following sections.

2.1.2. Liquid Phase Exfoliation

The LPE method consists of separating the layers by applying a gentler shear stress to the raw powder material (instead of the extreme mechanical force used during mechanical exfoliation), by immersing it in a liquid solvent exposed to ultrasonication.[11,43] Depending on the interplane van der Waals forces of each material and the thickness desired, the power, time and type of solvent used during the sonication process should be adjusted.[44–46] After sonication, a centrifugation step is necessary to separate thin flakes from bigger (useless) particles. The resulting product, which is offered by several manufacturers worldwide,[47] is a solution containing a given density of 2D flakes with specific lengths and thicknesses; these solutions sometimes require an additional polymer stabilizer to avoid flakes agglomeration. However, a recent report warned that most manufacturers tend to advertise too optimistic (fake) information about the thickness and lateral size of their product.[47,48] This indicates that producing high-quality monolayer 2D materials using this method is very difficult. Then, the 2D flakes can be deposited onto target substrates by

drop-and-dry,[49] inkjet printing,[50] or spray methods,[44,51] which in the best cases lead to a few-nanometer-thick layer made of many micrometric 2D flakes with random orientations and defective flake-to-flake bonding. Although this method might in principle be suitable for industrial applications (because it can easily cover entire wafers by spin coating) it results in electrons/holes scattering in the film, which degrades the mobility and overall performance of the FETs.[11] Nevertheless, solving this challenge seems to be much more feasible than developing a scalable mechanical exfoliation approach, and in the past few years the LPE method has been improved remarkably. One common strategy in this direction is to use an electrochemical treatment to intercalate different species into gap between layers (i.e., lithium[52] and tetraheptylammonium bromide[53]), which facilitates their separation during sonication. In October 2018, one breaking report[53] presented the fabrication of wafer-scale electrical circuits based on FETs with channels made of MoS_2 films synthesized via LPE method, and for the first time exhaustive (and useful) device-to-device variability information was reported. It is worth noting that even in this work none of the transistors had monolayer channels as all of them were based on mixed MoS_2 thicknesses; interestingly, the thickness fluctuations observed in that work did not seem to be a significant problem in terms of device performance and variability.

2.1.3. Chemical Vapor Deposition

CVD synthesis method has recently attracted a considerable amount of attention because it can produce different 2D materials with controllable thicknesses at the wafer scale. In general, the precursors (in gas, liquid, or solid state) are inserted into a tube furnace containing a catalyst substrate. When nanoparticles from the precursor reach the surface of the catalyst substrate, a chemical reaction takes place at those locations (also named seeds). With the time, these seeds expand/grow laterally on the surface of the catalyst substrate until nucleating to each other, resulting in a continuous polycrystalline film.[54,55] For example, the first synthesis of MoS_2 via the CVD method was reported by inserting MoO_3 powder (as Mo source) and sulfur powder (as S source) into a tube furnace containing a piece of SiO_2/Si using N_2 as carrier gas.[56]

The main challenge of this method for scalable FET production is that the density of point defects (i.e., lattice distortions) in the MoS_2 sheets is much larger than inside exfoliated nanoflakes, especially at the nucleation sites (i.e., grain boundaries). Although this can degrade the mobility of the charge carriers (as in the LPE method), decent mobilities have been reported (i.e., ≈24 $cm^2\ V^{-1}\ s^{-1}$ for CVD-grown monolayer top-gated MoS_2 FETs at room temperature,[57] 56 $cm^2\ V^{-1}\ s^{-1}$ for CVD-grown back-gated MoS_2 FETs[58]). Consequently, several companies started to commercialize large-area 2D materials grown via CVD approach.[59–61]

One particular issue is that the diameter of the tube furnace needs to be small in order to keep a homogeneous atmosphere that results in small thickness fluctuations of the 2D material, which considerably limits the size of the substrates that can be loaded. Some woks reported the use of large tube furnaces to produce large-area films,[62] but most scientists still prefer to use small tubes in order to achieve higher quality. To solve this problem, industrial facilities use systems where entire wafers can be loaded, and where their chambers use shower-like technology with hundreds of microtubes for homogeneous carrier gas and precursor injection (like the Black Magic from Aixtron[63]). In addition, these systems allow using plasma during the growth of the 2D material, which provides a better temperature control and avoids substrate de-wetting.

Another challenge facing the CVD approach is that it uses high temperatures up to 1100 °C, which (unlike in LPE method) impedes the deposition of the 2D material directly on the target wafers. To solve this problem, two potential solutions have been suggested. The first potential solution is to reduce the growth temperature, which so far has resulted in very poor material quality (i.e., prohibitive amount of lattice distortions and thickness fluctuations). In fact, one can find in the literature plenty of manuscripts claiming that they managed to grow graphene and other 2D materials at low temperatures (<450 °C) via CVD, but the quality of the material is never correctly characterized (via statistical analysis of cross-sectional TEM images), the carriers' mobility is always much lower, the performance of the devices shown are never proved statistically, and (more importantly) there is no company in the world offering 2D materials grown via CVD at low temperatures (<450 °C). Consequently, this approach is still not reliable and several important voices in the field indicated that solving this problem may be extremely complex, as using a high temperature is necessary to produce the chemical reactions. And the second potential solution is to grow the 2D material on an independent substrate and transfer it on the target wafer using a low temperature process. Although this may introduce some polymer contamination and may result in the generation of cracks (which are larger and more abundant in monolayers due to their lower mechanical strength), this second route seems to be much more feasible, and sophisticated wafer-scale transfer methods have been already developed.[64] It is also worth noting that some 2D semiconducting materials, such as phosphorene, have so far never been synthesized by CVD approach. In the best case, ≈40 nm thick BP films that exhibited typical p-type semiconductor behavior[65] was synthesized from red phosphorus thin films initially deposited on the substrate. Recent reports claimed the synthesis of phosphorene via CVD,[66] however, the quality demonstrated is still very far from that of exfoliated phosphorene (i.e., barely invisible A_g^1 Raman peak at 365 cm^{-1}).

2.1.4. Physical Vapor Deposition

PVD is another bottom-up synthesis method that has also been employed to prepare 2D materials. Within the category of PVD, different subtechniques have been developed. Ultrathin films of TMD materials have been deposited on a substrate by sputtering approach,[67] which uses high energy ions to vaporize the raw (powder source) 2D material. This method is attractive because it requires relatively low working temperatures (room temperature to 400 °C), and offers high deposition rates (≈1 Å s^{-1}).[67–70] Other PVD-related methods used to prepare 2D materials are local heating by pulsed laser[71] (which evaporates

target locally and form 2D materials on substrate), and general heating by a furnace (which physical transport MoS_2 from powder source to substrate).[72] So far, the 2D semiconducting films grown via PVD-related methods show much lower grain size than those grown via CVD approach,[73] which results in a much larger density of defects at the grain boundaries and reduces the performance of the FETs. Despite some works using PVD-related methods claimed the growth of 2D materials films with supreme quality, in fact there is still no company offering 2D materials grown using this method. In the case of phosphorene, it has been suggested that pulsed laser deposition can be used to deposit ultrathin amorphous BP (a-BP) films (with a highly disordered structure) using a bulk BP crystal source,[74] and the resulting devices exhibited p-type semiconducting behavior—but one should keep in mind that such a-BP material does not hold the genuine properties of real exfoliated phosphorene.

Table 1 summarizes the most relevant synthesis methods used to prepare MoS_2, WSe_2, WS_2, and BP (see Table 1). While top-down methods (mechanical exfoliation, LPE) have been widely adopted for the preparation of both TMDs and phosphorene in research labs, the limited lateral size and large thickness fluctuations will result in large device-to-device variability and thus impede their application in industry. On the other hand, bottom-up methods (CVD, PVD) have been studied in sufficient detail and have already been successfully used for the synthesis of TMDs, but still require more time and effort before they can be adopted for phosphorene synthesis. In particular, the CVD method results in uniform 2D material films with large lateral size and decent device performance, which makes it the most promising for future solid-state microelectronic devices fabrication; although the recent report in ref. [46] on MoS_2-based circuits fabricated via LPE also put again the eyes of the community on this method.

2.2. Device Configuration

The device structure of 2D-FETs is very similar to that of traditional silicon on insulator (SOI) FETs, although different configurations have been studied for research purposes. Among them, the most common are as follows:

i) Back-gated 2D-FET (Figure 2b).[75] This is the easiest way to build 2D-FET prototypes and most often used in basic studies. In this configuration the 2D material is directly grown or transferred on a conductive or semiconducting substrate with a dielectric layer on top. After that, the source and drain electrodes are deposited and the 2D material is selectively etched to form the channel. Some groups have studied the field effect without patterning a channel,[76] which is not ideal as it results in difficulties regarding estimations of the mobility (the channel width, W, in Equation (2) is unknown) and device-to-device variability problems. By using this configuration, there is no need to pattern a gate electrode, as the bulk material of the wafer below the superficial dielectric acts as gate. It is also worth noting that this gate is common for all devices on the wafer.

ii) Back-gated 2D-FET with patterned (individual) metal gate electrode (Figure 2c). This method can provide much higher controllability of the electrical field, compared to the single-back (common) gate FET. Some authors split the channel by patterning two gate electrodes (one next to each other) with different voltage control, and managed to form a p–n junction for ambipolar conduction.[77]

iii) Top-gated 2D-FET (Figure 2d). This structure is similar to the previous one, with the main difference that the patterned gate electrode is placed above the 2D channel.[78] In this configuration the top gate insulator can also work as encapsulating layer covering the entire channel, which can considerably improve the mobility of the FET, as a cleaner interface is created.[10,79,80]

iv) Dual-gated 2D-FET. This device configuration, which can use a substrate (Figure 2e) or patterned back-gate (Figure 2f), provides the highest degree of controllability of the charge carriers in the 2D channel.

v) Liquid-gating 2D-FET structure (Figure 2f). This is not a real device structure but a test structure only suitable for scientific purposes to explore the conduction limits of 2D-FETs, as the liquid gate cannot be implemented at the circuit level. However, we wanted to include it in this section because it has been widely used for several studies. In this test structure an ionic liquid is used as gate to create electric double layers at the liquid/channel interface, which acts as an

Table 1. Methods used to prepare or synthesize the most common 2D materials used as channel in FETs.

Materials	Top-down		Bottom-up	
	Mechanical exfoliation	Liquid phase exfoliation	Chemical vapor deposition	Physical vapor deposition
MoS_2	Yes Demonstrated in ref. [10]	Yes Demonstrated in ref. [11]	Yes, Reaction of component precursor vapors[56] Chalcogenization of a predeposited layer [210]	Yes, Sputter deposition[67] Pulsed laser deposition [71] Thermal evaporation deposition[72]
WSe_2	Yes Demonstrated in ref. [28]	Yes Demonstrated in ref. [211]	Yes Reaction of component precursor vapors[212] Chalcogenization of a predeposited layer [213]	Yes, Thermal evaporation deposition[214]
WS_2	Yes Demonstrated in ref. [29]	Yes Demonstrated in ref. [43]	Yes Reaction of component precursor vapors[215] Chalcogenization of a predeposited layer [216]	Yes, Thermal evaporation deposition[217]
BP	Yes Demonstrated in ref. [30]	Yes Demonstrated in ref. [218]	No, Suggested p-type semiconductor behavior[65] claimed successful growth, but the performances is far form exfoliated ones[66]	No, Attempt of pulsed laser deposition[74]

ultrathin dielectric for minimal screening of electric field. This strategy resulted in a higher performance because the strong band-bending caused by the liquid gate effectively reduces the Schottky barrier thickness at the MoS_2/metal contacts.[81]

For all these different device configurations it is extremely important to select a good dielectric material compatible with the 2D channel to reduce charge impurity scattering, which is known to be a key factor limiting the mobility of devices.[82] The dielectric materials traditionally used in CMOS technologies, i.e., SiO_2 and high-k dielectrics (e.g., HfO_2, Al_2O_3), have resulted in a low quality interface with the 2D material. The main reason is that 2D materials have very smooth interfaces without dangling bonds, and hence oxides tend to poorly nucleate on their surface. Often a nucleation layer is needed, such as a thin Al layer before the deposition of Al_2O_3.[83] Such nucleation layers may introduce damage to the interface and generate interfacial states that result in trapping and scattering of charge carriers. To solve this problem, one promising solution is to use 2D insulating materials, such as hexagonal boron nitride (h-BN), as gate dielectric for the 2D-FET.[84–87] This is because these 2D insulators ideally also have no dangling bonds and can adhere to the 2D semiconductors by van der Waals attraction, resulting in a minimized amount of interface states. Moreover, h-BN dielectric stacks have shown a very high reliability when exposed to electrical fields,[88–91] and have been already implemented in FETs,[87] resistive switching based nonvolatile memories,[92–98] and electronic synapses.[99,100] Other wide bandgap 2D layered materials that may adhere to the 2D semiconducting channel by van der Waals attraction may also work well as gate dielectric in 2D-FETs. More intense research in this direction should result in a higher performance and faster development of this technology.

After device construction, postprocessing (e.g., vacuum annealing) is often employed to remove impurities at the metal/2D material interface (i.e., polymer residues, water and/or oxygen molecules on the channel[28,101–103]), improve the adhesion of the metallic contacts,[104] and reduce metal/2D materials contact resistance.[105] The contact resistance of metal/2D materials is considered one of the factors that most degrades the performance of 2D-FETs (i.e., reduce effective mobility, produce hysteresis, limit max current).[106,107] Although there are some known strategies to reduce it, such as patterning edge contacts,[108] using metallic 2D layers[109] and introducing heavy doping,[110] it remains a key bottleneck to the performance of 2D devices.

It is important to emphasize that all the processes involved in the fabrication of the devices should be scalable (not only the synthesis of the 2D material). Up to now, most investigations in this field used EBL to pattern the electrodes and/or channel of the devices.[111,112] In situ metallic electrode deposition within the vacuum chamber of focused ion beam (by metal gas decomposition using ion gun) has also been often employed.[113] However, these methods do not allow patterning several devices in parallel, and consequently they are not scalable. Furthermore, this represents a very strong limitation in terms of characterization, as very few devices can be fabricated and this does not allow collecting statistical information about the devices (i.e., yield, device-to-device variability). This is by far the main criticism to nearly all academic publications in this field: they only show one, two, three, few devices, and consequently their findings may not be reliable/trustable. Using scalable processes for metal deposition (i.e., electron beam evaporator, sputtering) and device shape patterning (photolithography), plus collecting statistical information (i.e., yield, variability) of the devices is really the way to go. Refs. [53,114,115] may be taken as good examples of 2D material–based FET fabrication using only scalable approaches.

Overall, there is nothing impeding scientists the use of scalable processes to fabricate their devices. The methods are there, and they have been already used in some investigations.[53,114,115] The problem is that fabricating hundreds of devices in a scalable manner and provide statistical information about their performance is much more complex, expensive and time consuming than fabricating one single transistor via mechanical exfoliation and EBL, plus the data obtained using scalable approaches are normally not so spectacular. Therefore, many academics prefer to get nice data for their papers, even if they have to use unrealistic fabrication approaches that are useless for the development of real 2D material–based FET technology. Only a more technology-oriented mentality would lead to remarkable improvements in this field.

3. Effect of the Electrode/Channel Contact Resistance

When semiconducting 2D materials are connected to metal electrodes, a Schottky barrier is formed at the interface due to the misalignment energy levels of the two materials, which results in an effective contact resistance that limits the device performance. The Schottky barrier will absorb a non-negligible amount of the voltage applied, reducing the real potential difference at the channel region, and thus producing a lower effective charge carrier mobility. This results in the degradation of the electrical performance of the 2D-FET (i.e., I_{DS}, V_{th}, μ).

The Schottky barrier at the metal/channel interface can be lowered by introducing a postprocessing annealing step (i.e., vacuum, inert gas), although this always increases the complexity and cost of the fabrication process. Another option would be to simply use a material for the electrodes with a work function that matches the electron affinity of the semiconducting channel. However, even in that case a Schottky barrier may still exist due to strong Fermi level pinning.[79] This effect has been extensively investigated in devices with metal–MoS_2 contacts, but seems to be potentially less pronounced in other TMDs[116,117]—because the forming energy of chalcogen vacancies (e.g., S, Se) in other TMDs (i.e., $MoSe_2$, WS_2) is larger than that of sulfur vacancies in MoS_2, which may reduce the number of vacancies in such TMDs compared to MoS_2. Doping the metal/channel interface with substoichiometric oxides (MoO_x,[118,119] TiO_x,[120] and AlO_x[110]) and/or NO_2[121] can efficiently lower the Schottky barrier, due to the suppression of Fermi level pinning at the interface of 2D materials and metal electrodes. Another option is to insert a buffer layer between the metal and the 2D channel, such as graphene[122] or a thin insulating dielectric layer (such as 2 nm MgO,[123]

1 nm TiO_2,[124] or 1–2 layer 2D insulating h-BN[85,125]), to form a tunneling buffer layer resulting in a metal–insulator–semiconductor (MIS) structure, which has shown a remarkable reduction of the Schottky barrier with small tunneling resistance.

4. Effect of the Dielectric Environment

4.1. Gate Dielectric

In early studies, back-gated MoS_2 FETs on SiO_2 dielectric wafers were commonly used; however, the performance of these devices does approach to that theoretically predicted. This is most likely due to random charged impurities or Coulomb impurities within the 2D semiconducting channels[126] or on their surfaces, which can cause Coulomb scattering—that is the dominant scattering effect reducing the performance of 2D-FETs.[7,127] Charged impurities originate from a variety of impurity sources, such as residual metal ions in the dielectric, impurities at the 2D material/substrate interface, and residual solvent or adsorbed gas molecules during the device fabrication. These nonidealities act as point charges and interact with electrons/holes in the 2D material through long range Coulomb interactions. Intrinsic electrical properties of monolayer MoS_2 are known to be affected by charged impurities.[128,129] A promising avenue to improve the mobility of 2D-FET devices is the effective reduction and screening of extrinsic scattering centers. In addition, the carrier transport in the 2D material channel of the FETs can be degraded by remote interaction between the electrons and the optical phonons at the surface of the substrate.

These unfavorable interactions can be weakened by using a proper dielectric environment,[10,129] a solution that has also been proposed for graphene FETs.[130,131] By more effectively suppressing Coulomb scattering effects from charged impurities at the channel/dielectric interface, a monolayer MoS_2 device on a high-k dielectric environment has exhibited high room temperature mobility up to ≈150 $cm^2\ V^{-1}\ s^{-1}$.[129] Large dielectric constant of high-k material contributes to the reduction of effective size of Coulomb impurities.[129] Moreover, the room temperature mobility of MoS_2 channels in FETs is theoretically predicted to increase with increasing dielectric constant of the dielectric film in contact with it ($k_{HfO2} > k_{Al2O3} > k_{SiO2}$).[129]

Until now, a large number of dielectrics have been experimentally used to get better device performance, including high-k materials,[129] polymers,[132] self-assembled organic insulator and 2D insulator h-BN.[133] However, little attention has been paid to the scaling of the insulators toward sub-1 nm equivalent oxide thickness (EOT) as required for modern electronic devices, which would fully exploit the scaling potential of 2D materials. In particular, standard dielectrics such as SiO_2 and high-k oxides (e.g., Al_2O_3 and HfO_2) are amorphous, especially when grown in thin layers, and thus contain numerous defects. These defects severely degrade the reliability of 2D-FETs and make them problematic for further integration. Charge exchange between oxide defects and trap states in the channel leads to the ubiquitous hysteresis[134–137] and long-term drifts of the gate transfer characteristics[135,138,139]—often referred in Si technologies as bias-temperature instabilities (BTI).[140,141] Recently, an attempt to improve the quality of comparably thin (10 nm) HfO_2 films has been undertaken by crystallizing them using rapid thermal annealing (RTA),[142] but this methodology appears to be unsuitable to improve the performance of the devices due to the limited thermal stability of most TMDs.

In order to reduce these imperfections, the use of 2D layered dielectric films has been considered as dielectric candidate for 2D-FET devices, as they present an atomically flat surface free of dangling bonds.[133] Devices with h-BN dielectrics have recently exhibited considerably improved channel mobility,[133] as well as reduced hysteresis and BTI drifts.[135,143] Additionally, the fact that the lateral thermal conductivity of h-BN is very high (360 $W\ m^{-1}\ K^{-1}$) compared to SiO_2 (0.69–1.4 $W\ m^{-1}\ K^{-1}$), HfO_2 (0.3–2.55 $W\ m^{-1}\ K^{-1}$) and Al_2O_3 (0.49–2.3 $W\ m^{-1}\ K^{-1}$),[144] is also very attractive from a reliability point of view, as it can slow down the dielectric breakdown process.[88] It is worth noting that h-BN has a low dielectric constant of 5.06 and a small bandgap of about 6 eV,[145] which from a theoretical point of view might raise concerns regarding excessive gate leakage currents[146] (and consequently low ON/OFF current ratios) in devices requiring sub-1 nm EOT scaling. However, sub-1 nm (<3 layers thick) h-BN stacks have exhibited good ability to block leakage current—the I–V curves collected via CAFM in monolayer (0.33 nm thick) h-BN show that the voltage needed to raise current above the noise level (also named onset voltage, V_{ON}[88]) is ≈0.75 V,[88,144] which is similar to that observed in 0.4 nm Al_2O_3.[147] More investigations on the leakage current of sub-1 nm h-BN compared to traditional dielectrics are required. The combination of different insulating materials stacked one of each other (i.e., Al_2O_3 on h-BN)—a solution widely employed by the industry[148]—may be a potential solution that also deserves further exploration.

As an alternative to high-k oxides and h-BN, crystalline calcium fluoride (fluorite and CaF_2) has recently been suggested as a gate insulator in MoS_2 FETs.[146] This material has a higher bandgap of 12.1 eV and dielectric constant of 8.43, which makes tunnel leakages negligible even for sub-1 nm EOT. At the same time, the F-terminated surface of CaF_2 epitaxially grown on Si (111) is inert and contains a very low amount of defects, and can form a quasi van der Waals gap interface with MoS_2. First prototypes of bare-channel back-gated MoS_2 FETs with only 2 nm thick CaF_2 insulators have already shown ON/OFF current ratios up to 10^7, subthreshold swings down to 90 mV $decade^{-1}$, and a hysteresis as small as that of conventional Si/high-k FETs[146] (see **Figure 3**).

It should be noted that this section mainly concentrated on different gate dielectrics in contact with MoS_2 material. The results using other 2D semiconducting materials with TMD structure should lead to similar results. However, reliability studies using phosphorene and silicene should are very scarce, and more work in this direction is required.

4.2. Encapsulating Dielectric for Stability Purposes

Dielectric films can be also used to fully surround (i.e., encapsulate) the 2D semiconducting channel of the 2D-FETs, protecting them from adsorbates coming from the ambient. So far, the performance of 2D-FET transistors with channels made

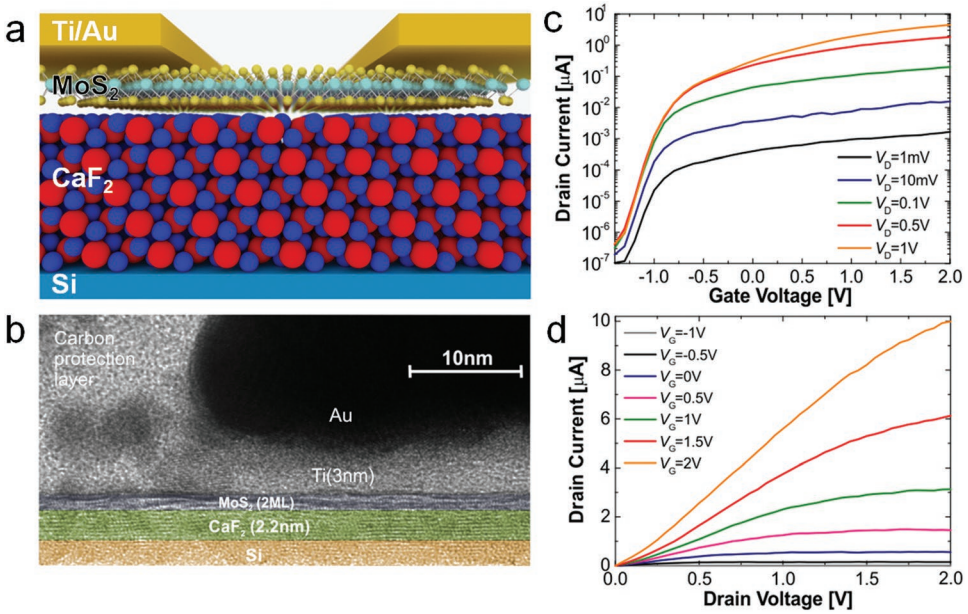

Figure 3. a) Atomic structure of the quasi van der Waals interface between F-terminated CaF_2(111) and MoS_2. b) Transmission electron microscope image confirms MoS_2 channel on about 2–2.5 nm CaF_2 insulator. The gate transfer c) and output b) characteristics confirm reasonable performance of the CaF_2(2 nm)/MoS_2 FETs. Reproduced with permission.[146] Copyright 2019, Springer Nature.

of TMDs, such as MoS_2, WS_2, and WSe_2, has not been ideal. However, the relatively low mobility of TMD channels is considered to be a limit for some FET based applications. As such, an intensive search for alternative 2D materials is currently in progress. The most interesting options among them are 2D counterparts of conventional materials, such as silicene[149] and phosphorene.[150] The narrow bandgaps of these materials are between the zero bandgap of graphene and the larger bandgap of TMDs (i.e., 1.8 eV for monolayer MoS_2[151] and 2.0 eV for WSe_2[152]), which makes them attractive due to their (theoretically) higher carriers mobility. However, in addition to the poor quality when synthesized with scalable bottom-up methods, the main problem of these materials is their poor air stability.

At the moment, studies on silicene FETs are very rare due to the extremely poor air stability of this material, i.e., in ref. [153] it was demonstrated that silicene dissolves in air after about 2 min. As such, the fabrication of silicene FETs requires very complicated processing techniques in which the channel has to be encapsulated by a metallic substrate (in the bottom) and a dielectric (on the top), and the electrodes need to be created by patterning this metallic substrate after flipped transfer.[153] These techniques are currently not available to a wide research community, and they do not allow fabrication of multiple devices in parallel. In contrast, phosphorene FETs have been successfully fabricated by many groups. Phosphorene is also very sensitive to the ambient but allows air exposure up to several hours, though this should be minimized during device fabrication. After extended air exposure, the performance of phosphorene FETs would be degraded by physical changes (i.e., volume expansion, uneven surfaces) or chemical changes (i.e., alteration of electronic structure, generation of large Schottky barrier heights) which result from surface degradation.[2] In order to solve this problem, several attempts of encapsulation of phosphorene FETs with an AlO_x layer,[154–156] polymers[154,157] and 2D h-BN[158,159] have been reported. An efficient solution has been found only using conformal encapsulation schemes (see **Figure 4**).[160] Recently, at least 17 months of phosphorene FETs stability has been achieved using conformal Al_2O_3 and Al_2O_3/Teflon-AF encapsulation, with the latter scheme also leading to an improved device performance and reliability.[160,161] However, it is shown that the performance of phosphorene could be significantly degraded by Al_2O_3 capping, resulting in a 5 times lower ON-state current and 3 times lower ON/OFF ratios, likely due to the moisture introduced during the ALD encapsulation process.[162] Recently, He et al.[163] demonstrated that van der Waals passivation of phosphorene FETs with dioctylbenzothienobenzothiophene (C_8-BTBT) thin films allows to efficiently preserve the intrinsic properties of phosphorene. In addition, phosphorene FETs with ultraclean interfaces have been obtained by sandwiching the channel between two h-BN layers, and these devices exhibited a higher mobility of up to ≈1350 $cm^2\ V^{-1}\ s^{-1}$ and ON/OFF ratio exceeding 10^5 at room temperature. However, long-term stability of phosphorene FETs encapsulated with layered materials still has to be proven, since some of these materials can be partially transparent. For instance, the devices from ref. [163] exhibit some signs of degradation already after about two weeks.

In **Table 2**, we list the performance of phosphorene based FETs, including structural information (channel length, width and thickness, device structure, including gate position, gate insulator thickness and contacts metal), measuring conditions, ON/OFF ratios and mobilities. It should be highlighted that, for research purposes, measuring in vacuum condition can be considered as another kind of dielectric environment, as the gaseous adsorbates (such as humidity and oxygen molecules) can be desorbed from surface of the 2D channel. This methodology results in higher device current measured in vacuum as compared to air.[102,103,164,165]

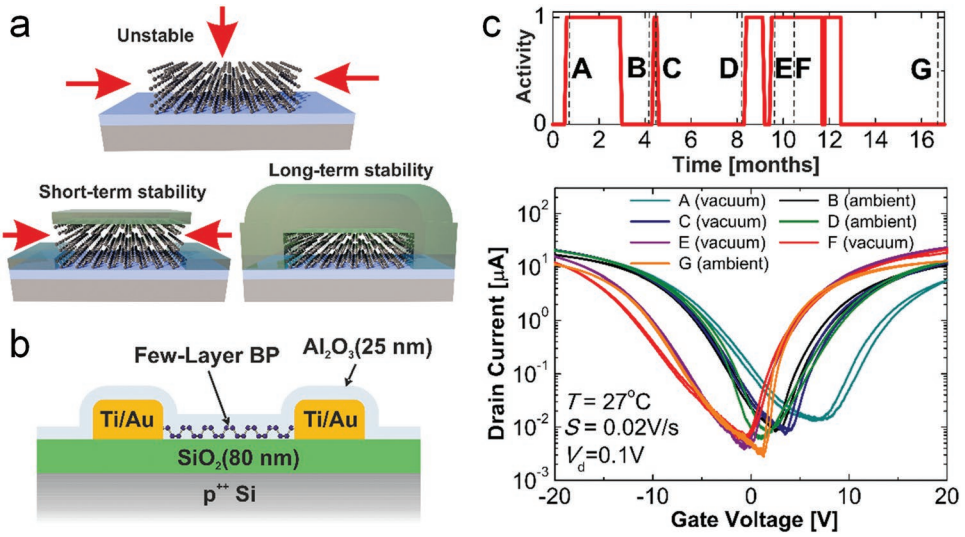

Figure 4. a) Encapsulation schemes typically used for BP FETs. Only conformal encapsulation has been found to guarantee long-term stability. b) Encapsulation with 25 nm Al_2O_3 leads to at least 17 months stability of BP FETs even if the devices are intensively stressed and alternatively stored in the ambient c). Reproduced under the terms and conditions of the Creative Commons CC BY 4.0 International License.[160] Copyright 2017, The Authors, published by Springer Nature.

In any case, it is important to highlight that performance degradation with the time due to poor stability introduces one uncontrollable variable more that can alter the reliability of the devices. This is important when considering device-to-device variability, a piece of information that is lacking in most 2D material–based FET reports.

5. Effect of the Channel Length

In order to achieve a better performance of the FETs (e.g., higher operation speed) and increase the amount of devices per chip (which also results in a higher performance at the circuit level), one common strategy consist on reducing the length of its semiconducting channel. However, this can produce some undesired phenomena, such as severe decrease of the ON/OFF current ratio, as well as a sharp increase in drain induced barrier lowing (DIBL) was observed during the scaling down of the channel length. These phenomena, also known as short channel effects, have been also observed in earliest reports, which used nonoptimized metal/2D material interface junctions.[166] Similar observations have also been reported in refs. [167,168]. Liu et al.[166] observed that the degradation of the electrostatic control from the gate could be more severe when the channel length is smaller than a limiting value (see **Figure 5**a). This characteristic length for the onset of short channel effects for planar transistors can be calculated by[169]

$$\lambda = \sqrt{\frac{\varepsilon_s}{\varepsilon_{ox}} t_s t_{ox}} \tag{3}$$

where λ is the characteristic length, ε_s and ε_{ox} are the permittivities of the 2D material semiconducting channel and the gate dielectric layer, and t_s and t_{ox} are the thicknesses of 2D materials semiconducting channel and gate dielectric layer. Following this formula, the characteristic channel length for 2D material transistor can be optimized to a smaller value by using a thinner channel, a thinner gate dielectric layer or a gate dielectric layer with higher ε_{ox}. Consequently, by optimizing the dielectric layer (e.g., replacing by HfO_2 or other materials with a higher permittivity), the predicted limiting or characteristic channel length for MoS_2 can be reduced down to ≈1–2 nm.[166,168] As shown in Figure 5a, for FETs using 5 nm thick MoS_2 channels, the degradation rate of the ON/OFF ratio for short channel lengths is slower than for FETs using 12 nm thick MoS_2 channels.[166] It was also observed that the mobility of the 2D material decreases severely when thinning the MoS_2 channel (see also Section 6). Experimental evidence of the influence of the channel thickness together with the channel length dependence has been reported in ref. [170]. The appearance of short channel effects in air as a function of channel length and channel thickness is shown in Figure 5b. In principle, short channel effect could be excluded by using longer channel or thinner channel (see Equation (3)).[79,170] In other words, thinning the channel is one possible way to make the device work when its channel has to be short.

In addition to these geometrical parameters, the quality of the electrode/channel junction and the intrinsic dielectric constant of the material selected for the channel need to be carefully engineered to suppress short channel effects in the 2D-FET. Ideally, the ON-current (or ON-resistance) of a device is supposed to be linearly dependent on the channel length; however, as shown in Figure 5c, a deviation typically occurs due to the additional metal–2D material contact resistance,[166,171] which results in a degraded lateral electrical field in the channel. In addition, the ON-resistance could be smaller when the channel is made of a 2D material with smaller dielectric constant.

Besides that, the mobility of MoS_2 decreases with decreasing channel length in both back-gated (see Figure 5d) and top-gated configuration,[166,172,173] which may be attributed to two reasons. First, in 2D-FETs with metal/2D material contact resistance (which do not scale with channel length), the negative effect of the contact resistance would become more and more obvious

Table 2. Summary of BP FETs' structural parameters, measurement, and performance.

Ref.	L/W [μm]	T [nm]	Preparation	Gate, Gate dielectric	Metal	Annealing	Encapsulation	Measurement condition	Ohmic contact	ON/OFF ratio	h mobility [$cm^2 V^{-1} s^{-1}$]	e mobility [$cm^2 V^{-1} s^{-1}$]
[219]	8.7/7	8	ME	Back, 285 nm SiO_2	5 nm Ti	No	No	Dark, 10^{-5} mbar	Yes			
										$>10^3$ (h), 10 (e)	0.5	
[220]	0.45/1.85	12	ME	Back, 285 nm SiO_2	5 nm Ti	No	No	300 K		600	35	12
								4 K		40 000	31	14
	0.15/2							300 K		50	10	4
								4 K		10 000	8	4
[107]	3/-	18.7	ME	Back, 90 nm SiO_2	30 nm Ni	No	No	Ambient	Yes	$\approx 10^2$	170.5	
					30 nm Pd					–	186.5	
[221]	17.3/5.9	8	ME	Back, 290 nm SiO_2	5 nm Ti	No	No	10^{-6} Torr, 295 K	Yes	10^4	103 (positive sweep), 38 (negative sweep)	
[30]	1.6/4.8	5	ME	Back, 90 nm SiO_2	5 nm Cr	No	No		Yes	$\approx 10^5$		
	4.5/2.3	5			(Or Ti)				Yes		55	
		8									197	
		10									984	
[40]	1/–	5	ME	Back, 90 nm SiO_2	20 nm Ti	No	No		Yes	$\approx 10^4$	286	
[222]	1.1/2.6	7.5	ME	Back, 300 nm SiO_2	100 nm Au	Yes	Yes	5×10^{-5} Tor, RT	Yes			
[223]	1/–	5	ME	Back, 300 nm SiO_2	1 nm Ti	No	No	RT	Yes	$>10^5$	205	
[158]		8	ME	Back, 300 nm SiO_2 + h-BN	2 nm Cr	Yes (before putting electrodes)	Yes	1.7 K	Yes			
		≈15						300 K		10^5	1350 (FET mobility)	
											790 (Hall mobility)	
								1.7 K		10^8	2700 (FET mobility)	
											1500 (Hall mobility)	
[224]		5.7	ME	Back, 300 nm SiO_2	5 nm Ti	No	Yes by BN	Vacuum, 300 K			>10	
		4.5					No	Vacuum				10 to 100
		5.7					Yes by BN	Vacuum, 200 K	No (h), Yes (e)	10^5	86	62
							No		No (h) and (e)		118	< 5
[218]		<10	LE	Back, 300 nm SiO_2	20 nm Ni	No	No	$<5 \times 10^{-4}$ Torr, RT	Yes	10^4	25.9	
[225]		20	ME	Liquid	5 nm Cr	Yes	No	220 K		$\approx 5 \times 10^3$	≈190	≈20
[226]		14–28	ME	Back, 200 nm SiO_2	8 nm Cr	No	No		Yes	10^4-10^5	247 (Zigzag), 392 (Armchair)	
[227]		4.5	ME	Back, 300 nm SiO_2	5 nm Cr	No	No	405 nm laser, $\approx 10^{-7}$ mbar, RT	Yes	10^5	142	

Table 2. Continued.

Ref.	L/W [μm]	T [nm]	Preparation	Gate, Gate dielectric	Metal	Annealing	Encapsulation	Measurement condition	Ohmic contact	ON/OFF ratio	h mobility [$cm^2 V^{-1} s^{-1}$]	e mobility [$cm^2 V^{-1} s^{-1}$]
[228]		4.8	ME	Back, 300 nm SiO_2	5 nm Cr	No	No	405 nm laser with 40 mV, ≈10^{-8} mbar, RT	Yes		214.8	1
[49]		7.4	LE	Back, 270 nm SiO_2	15 nm Ti	Material and device anneal	No	Ambient	No	10^3	0.58	
[229]		11.5	ME	Top, 20 nm Al_2O_3 (ALD)	5 nm Ti	No	Yes	Ambient, RT	Yes (e), No (h)	500		
[230]	10.6/2.7	15	ME	Back, 25 nm Al_2O_3 (ALD)	1.5 nm Ti	No	Yes	Ambient	Yes	$>10^3$	310	89
[231]	≈150/5		EE	Back, 300 nm SiO_2	3 nm Ti	Yes	No	Ambient	Yes	10^4	≈7.3	
[36]	1 μm	8	ME	Back, 90 nm SiO_2	Ni	No	No	Dark, 2×10^{-4} mbar, 300 K	Yes			
								633 nm with 250 mW cm^{-2}, 2×10^{-4} mbar, 300 K				
								Dark, 2×10^{-4} mbar, 20 K	No			
								633 nm with 250 mW cm^{-2}, 2×10^{-4} mbar, 20 K				
[232]	1.5 μm		ME	Back, 200 nm SiO_2	50 nm Au	Yes	Yes	Ambient, RT	Little barrier	4		
[233]			ME	Back, 300 nm SiO_2	10 nm Cr	No	No		Yes	<10	721	

Note: L: channel length; W: channel width; T: channel thickness; ME: mechanical exfoliation; LE: liquid exfoliation; EE: electrochemical exfoliation.

when it becomes more comparable to the channel resistance during downscaling. And second, it could be possible that the velocity of the charge carriers almost/completely saturates at shorter channel lengths.[166] Based on the simulation results from ref. [174] (which studied MoS_2 and FinFET transistors with channel lengths down to 10 nm), even though 2D MoS_2 channels showed better suppression of short channel effects than Si channels, their ON-state currents are lower than in commercial FinFETs (>1 mA μm^{-1} based on ITRS) due to the low carrier saturation velocity of MoS_2. Nevertheless, current density >400 μA μm^{-1} was already demonstrated in monolayer MoS_2 with 10 nm top gates.[175]

However, we note that all the literature reports discussed above have studied short channel effects on experimental 2D-FET technologies that have not been fully optimized. For instance, further development of recently reported devices using 2 nm CaF_2[146] and even 10 nm HfO_2[142] might allow further minimization short channel effects for channel lengths in the several nanometer regime.

6. Effect of the Channel Thickness

Since mobility and ON/OFF current ratio are important performance benchmarks of 2D material FETs for logic applications, their dependence on the thickness of the MoS_2 channel has been discussed in several reports.[79,176–181] Although the reported mobility values show large dispersion, two observations are quite repetitive: i) there is an obvious trend suggesting that thicker MoS_2 channels produce a higher mobility in the thin few-layer regime and ii) the increase of the mobility will slow down when the thickness reaches a critical value or range. Alternatively, the mobility might decrease in thicker channels because of the finite interlayer conductivity and accumulation of interlayer resistance.[79]

Das et al.[79] investigated room temperature mobility values of back-gated SiO_2-supported MoS_2 FETs with channel thicknesses range from 2 to 70 nm (see **Figure 6**a). Based on their results, the channel thickness that provides the highest performance is in the range of 6–12 nm, the mobility increases monotonically with increasing channel thickness before this range (6–12 nm). The nonmonotonic trend after this range can be readily explained with a resistor network model (see the inset of Figure 6a). As the source and drain electrodes are connected only directly to the top MoS_2 layer, additional interlayer resistance contributions (σ_{int} is the interlayer conductivity) are involved when charges flow along the lower layers, which means that the total access resistance will largely increase in 2D-FETs with thicker channels. Moreover, the gating has a higher impact in the 2D layer in contact with the gate dielectric, and screening results in a decreasing number of charges for the top MoS_2 layers.[79] These two factors can

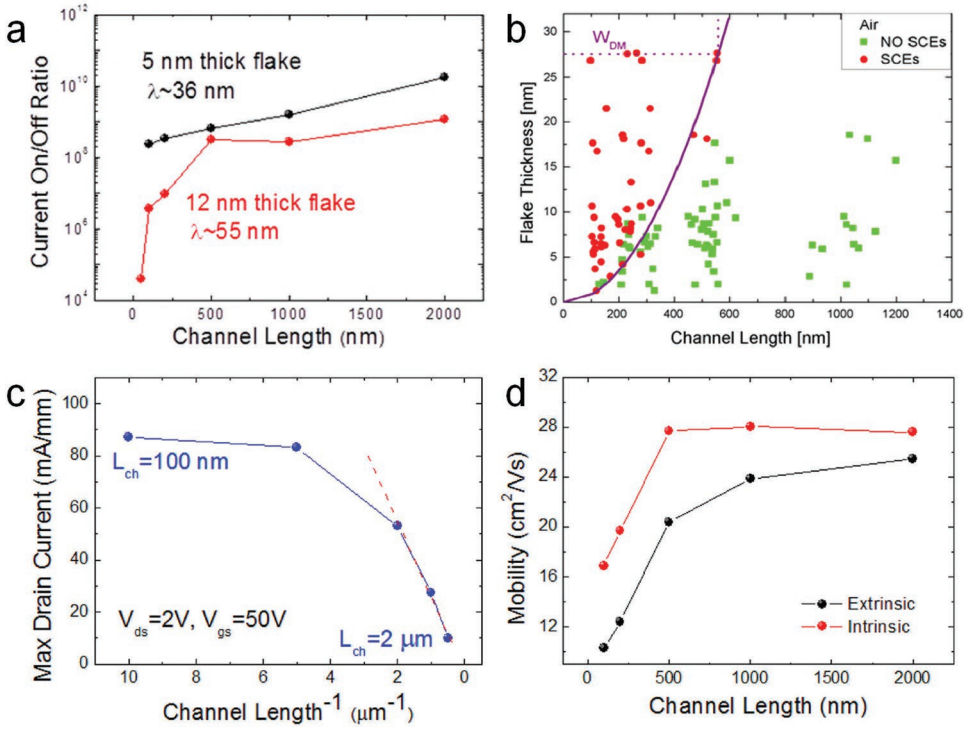

Figure 5. a) Channel length dependent on/off ratio of 5 and 12 nm thick MoS_2 channel Reproduced with permission.[166] Copyright 2012, American Chemical society. b) Appearance of short channel effects in air as a function of MoS_2 channel length and thickness. Reproduced with permission.[170] Copyright 2014, American Chemical society. c) Channel length dependent ON current of on 5 nm thick MoS_2 channel. Reproduced with permission.[166] Copyright 2012, American Chemical society. d) The mobility of a set of 5 nm thick MoS_2 channel with various channel length. Reproduced with permission.[166] Copyright 2012, American Chemical society.

seriously restrict the effective mobility of thicker 2D channels, in agreement with the observation of a decreased mobility after this 6–12 nm range. This phenomenon has also been observed by Chang et al.[176] In ref. [177] the authors observe that higher mobilities are generally observed in thicker MoS_2 channels, consistent with their model based on the Boltzmann transport equation, which considers phonons, charged impurities, boundary and other nonidealities impacting the performance of the 2D-FETs (see Figure 6b). In addition, the ON/OFF current ratio dependence on the channel thickness (as shown in Figure 6b) illustrates that the ON/OFF current ratio decreases with increasing channel thickness in MoS_2 FETs, which was also reported in ref. [171]. So, in order to achieve the desired performance, an optimum channel thickness needs to be carefully chosen. Moveover, the no observation of mobility reduction in thicker stacks may be related to the edge contact used in the multilayer MoS_2 FETs,[177] which effectively improves the current injection to each single layer of multilayer MoS_2, overcoming the interlayer resistance in the model in ref. [79].

Li et al.[178] carried out a deeper experimental analysis, and the relationship between carriers' mobility and number of layers is summarized in Figure 6c. The highest mobility is achieved with 14-layers thick channels, which is consistent with the results of ref. [79]. In addition, the decrease of mobility after a certain number of layers can also be explained with the model developed in ref. [79]. In addition, the mobility versus number of layers dependence has been simulated using a model with Coulomb and phonon scattering.[178] A similar trend can also be found in ref. [179] and ref. [171]. By using the generalized theoretical model in ref. [178], it has been concluded that few-layer-thick (14 layers) MoS_2 channels are less sensitive to extrinsic scattering and they can achieve more favorable mobility values compared to extremely thin monolayers. Therefore, the charged impurity dominated mobility increases with the number of layers in this ultrathin regime. This monotonic increase of the mobility in the few-layer regime is also reported in refs. [133,180]. It is noted that the interfacial Coulomb impurities (gaseous absorbates on both the bottom and top surfaces of the channel, as well as dangling bonds on the supporting SiO_2 surface) are responsible for scattering events in the ultrathin MoS_2 channel. This is due to the reduced Coulomb interaction distance, which dominates the degradation of mobility in ultrathin MoS_2 channels. As a consequence, the performance of MoS_2 thin channel FETs can be improved by interfacial cleanliness. As shown in Figure 6d,[133] using hexagonal boron nitride as supporting dielectric layer can lead to higher extracted mobility values than those of SiO_2 supported FET devices. Similar enhancement enabled by a better dielectric environment has been observed in refs. [132,181].

7. Effect of the Temperature

The transfer characteristics of 2D-FETs measured at different temperatures reveal that I_{DS} can increase or decrease with temperature depending on the transport regime (**Figure 7**a,b).

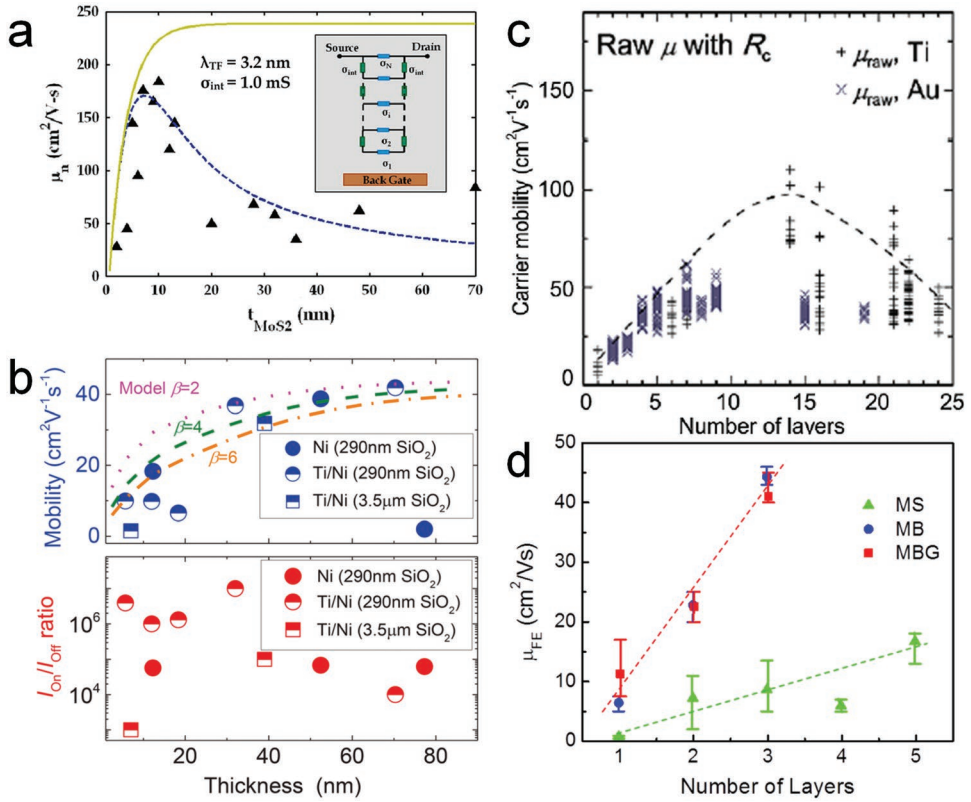

Figure 6. Dependence of the performance on the thickness of the MoS_2 channel: a) the extracted effective field effect mobility as a function of the MoS_2 layer thickness. The dotted line is a fit to the experimental data using a model (inset). The solid line shows the simulated field effect mobility without any interlayer resistance; Reproduced with permission.[79] Copyright 2013, American Chemical Society. b) Mobility and on/off ratio of devices with different MoS_2 thickness. Reproduced with permission.[177] Copyright 2014, Royal Society of Chemistry. c) Room temperature mobility versus various MoS_2 channel thickness. Reproduced with permission.[178] Copyright 2013, American Chemical Society. d) Mobility of MoS_2 FET channels on different dielectric substrates as a function of the number of MoS_2 layers, MS refers to MoS_2 on SiO_2, MB refers to the channel on h-BN, MBG denotes the MoS_2 channel on h-BN with graphene as back gate. Reproduced with permission.[133] Copyright 2013, American Chemical Society.

The changes with temperature can be related to changes in carrier concentration, threshold voltage, or mobility. For example, Figure 7b shows that in the low carrier density regime (i.e., $-2\ V < V < 1\ V$), the conductivity of monolayer MoS_2 (with dual gate[182]) channels measured with four contacts decreases with decreasing temperature. Conversely, in the high conductivity regime (i.e., gate voltage >1 V in Figure 7b), the conductivity increases with decreasing temperature. Similar trends have been reported for single gate multilayer MoS_2 channels.[102,179,183,184]

Although the lattice phonons play an insignificant or moderate role in the thickness dependence of the mobility, the channel mobility of MoS_2 devices at various temperatures is mainly affected by phonons scattering, which can be rapidly enlarged at higher temperatures. Generally, acoustic phonon scattering and charged impurities dominate the performance of monolayer MoS_2 channels at low temperatures ($T < 100$ K). On the contrary, the performance of monolayer MoS_2 at higher temperatures is determined by the optical phonons. By using first-principles methods, Kaasbjerg et al.[185] calculated that the phonon-limited mobility at $T > 100$ K (see Figure 7c) follows an inverse power-law relation with the temperature

$$\mu \propto T^{-\gamma} \tag{4}$$

where γ is the phonon damping factor (which typically ranges between 1 and 2, e.g., it is 1.69 at room temperature[185]). As a result, the mobility of monolayer MoS_2 channels at room temperature is expected to be limited to ≈410 cm^2 V^{-1} s^{-1}, primarily owing to optical phonons. The mobility at low temperatures ($T < 100$ K) can reach a few thousand cm^2 V^{-1} s^{-1}. This value has been almost achieved in monolayer MoS_2 with h-BN encapsulation,[186] indicating the existence of other scattering mechanisms due to defects and charged impurities.

7.1. Effect of the Temperature for Different Thicknesses

In FETs with monolayer MoS_2 channels, the exponents γ fitted in Equation (4) according to empirical measurements result in values of 1.7 (in exfoliated samples)[81,101] and 1.6 (in CVD-grown samples),[114] which is consistent with the theoretical values (1.69). When using MoS_2, smaller γ (<1.69) can be achieved in FETs with bilayer[101] or in thick channels (4–26 layers)[179] due to the more active quenching of the homopolar phonon mode. However, thicker MoS_2 channels have shown γ values larger than 1.9 (see Figure 7d)[186] which

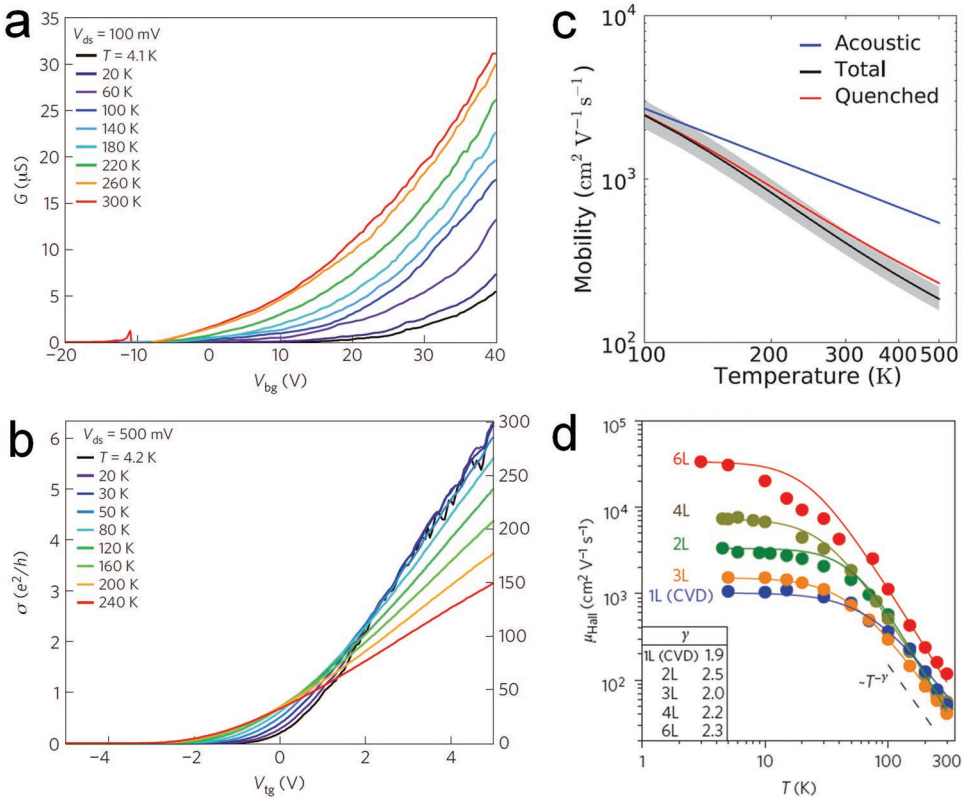

Figure 7. Conductivity as a function of a) back-gated voltage and b) top-gated voltage for various measuring temperature. Reproduced with permission.[182] Copyright 2013, Macmillan Publishers limited. c) The mobility in the presence of only acoustic deformation potential scattering (blue). The (gray) shaded area shows the variation in mobility associated with a 10% uncertainty in the calculated deformation potentials. Reproduced with permission.[185] Copyright 2012, American Physical Society. d) Mobility of different numbers of layers of MoS_2 channel as a function of temperature. Reproduced with permission.[186] Copyright 2015, Macmillan Publishers limited.

may be due to the different electron–phonon coupling in the monolayer due to a shift of the band valley from Γ–K to K and K′.[187] The broadly distributed values of γ demonstrate that charge transport at room temperature may not only be dominated by lattice phonon scattering.[188]

7.2. Effect of the Temperature for Different Device Structures

Based on the simulations in ref. [185], a slight decrease of the exponent γ in Equation (4) can happen for monolayer FETs with a top-gated structure exhibiting a larger mobility in the channel region, which is produced by the effect of quenching the out-of-plane homopolar mode. The experimental observation of a γ decrease has been reported in dual-gate devices (ranging from 0.55 to 0.78 for top gating, and 1.4 for only back-gating).[182] However, compared to the screening effect of impurities by the top-gate encapsulating dielectric, the enhancement due to quenching of the out-of-plane homopolar mode is not very dominant. In addition, Perera et al.[81] also reported that liquid gating devices show relatively higher overall mobility from 77 to 180 K (≈1.2 for liquid gating, ≈1.7 for without liquid gating; see **Figure 8**a), which can be attributed to both extrinsic scattering screening and phonon mode quenching by liquid gating.[81]

7.3. Effect of the Temperature for Different Dielectric Environments

Computational studies[129] revealed that the value of γ will change with different dielectric environments. 2D-FETs with monolayer or multilayer MoS_2 channels encapsulated with h-BN dielectrics show a higher γ value than nonencapsulated ones.[187] The mobility of monolayer devices keeps increasing with decreasing the temperature, suggesting that scattering from charged impurities has been largely suppressed by the top h-BN encapsulation.[187] When both the bottom and top h-BN encapsulation layers are used with a sandwiched structure, the mobility of multilayer MoS_2 in the low temperature regime does not saturate (compare Figure 8c,d), because the scattering from the substrate is screened by the inserted h-BN stack. This proves that extrinsic scattering effects dominate the mobility of the MoS_2 channel in the low temperature regime (T < 100 K). With better dielectric environment (for effective screening of extrinsic scattering), the increase of mobility will not stop at lower (<100 K) temperatures. In addition, Bhattacharjee et al.[189] experimentally studied different degradation rates of mobility with different dielectric supporting films in the high temperature regime (>100 K). It was found that the value of γ in Equation (4) is heavily dependent on the optical phonon energy of the dielectric environment (see Figure 8b).

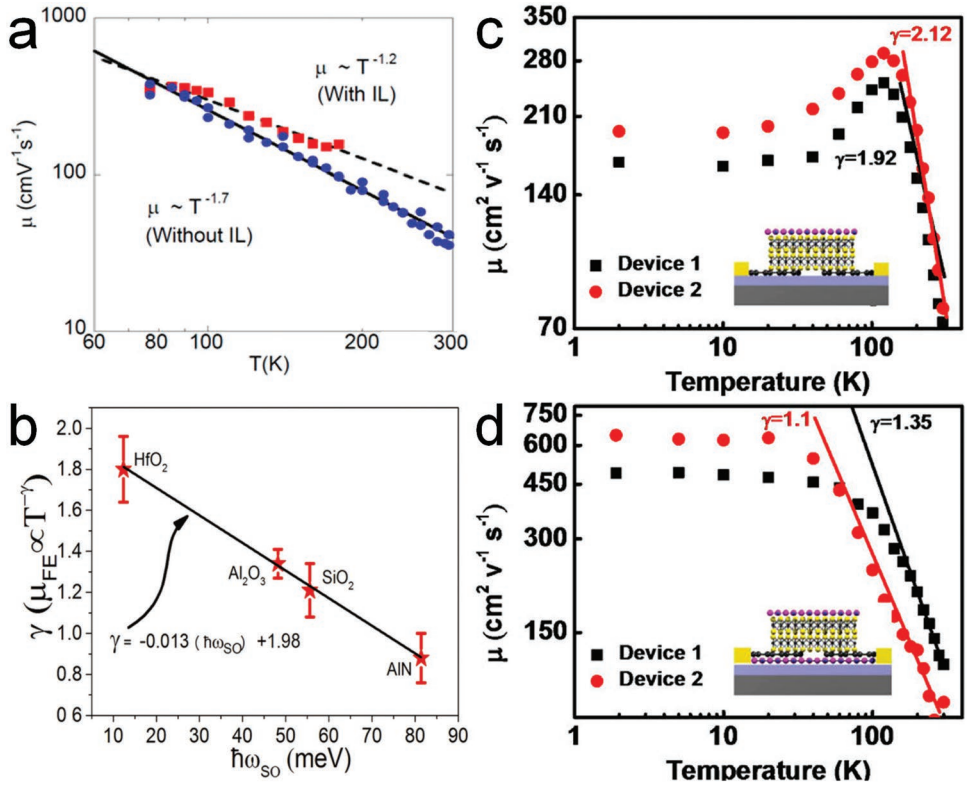

Figure 8. a) Temperature dependence of the MoS_2 channel in the presence or absence of liquid gating. Reproduced with permission.[81] Copyright 2013, American Chemical Society. b) Degradation parameter (γ) versus the optical phonon energy of the underlying substrate with an excellent linear fit. Reproduced with permission.[189] Copyright 2016, Wiley-VCH. Temperature dependent mobility of multilayer MoS_2 devices with c) only top h-BN encapsulation and d) both top and bottom h-BN encapsulation. Reproduced with permission.[187] Copyright 2015, American Chemical Society.

At temperatures >300 K the mobility decreases.[190–192] This can be explained by the limiting factor of optical phonons and the creation of Sulfur vacancies in MoS_2,[193,194] which takes place in bare channel devices. The latter causes a negative shift of the threshold voltage, which is not observed in protected channel devices. Therefore, it has been suggested that a proper dielectric environment encapsulation is essential for the high-temperature operation of 2D-FETs.[190]

7.4. High-Field and High Current

A key requirement for high-performance FET is the ability to carry high current density (≈1 mA μm^{-1}). At high electric field, the mobility is no longer a good figure of merit since the drift velocity starts to saturate as follows[195]

$$v_d = \frac{\mu_{LF} \cdot E}{\left[1+\left(\frac{\mu_{LF} \cdot E}{v_{sat}}\right)^{\gamma}\right]^{1/\gamma}} \quad (5)$$

where μ_{LF} is the low-field mobility, E is the electric field, γ is an empirical fitting parameter, and v_{sat} is the velocity saturation - note that in Equation (4) the symbol γ was used to refer to phonon damping factor, but in equation (5) and section 7.4 it refers to an empirical fitting parameter. For consistency with the previous literature, we preferred not to replace this symbol by a different one. Measurements of v_{sat} show that it is severely limited by temperature and self-heating effects in monolayer MoS_2.[195] The heat dissipation to the substrate in 2D semiconductors is dominated by their large thermal boundary resistance.[196,197] The required current density is yet to be demonstrated but can be potentially achieved by: i) applying fast switching transients, shorter than the thermal transient, ii) reduction of electrical contact resistance (e.g., by doping to reduce the large power density at the contacts), iii) using short-channel devices where more of the heat can be dissipated laterally to the contacts, and iv) finding new strategies to reduce the thermal boundary resistance.

8. Conclusions

2D semiconducting materials can be used as channels in FETs in order to enhance their performance (i.e., mobility, sub-threshold swing, threshold voltage, electrostatic gate control, short-channel immunity, back-end-of-the-line integration). MoS_2 was the first 2D semiconducting material used as channel in an FET (in 2011). After that, many other materials from the TMD family, with the general formula of MX_2 (being M = transition metal and X = chalcogen), such as $MoSe_2$, $MoTe_2$, WSe_2 and WS_2, have been also used. Other 2D semiconducting materials like silicene and phosphorene have also shown promising properties, although they are unstable in air and require a more sophisticated encapsulation.

The performance of 2D-FETs can be enhanced using different strategies, such as modifying the material lattice (i.e., doping the 2D materials,[198–200] alloying different TMD materials which results in hybrid lattices,[201,202] formation of vacancies[203,204]), constructing 2D material heterostructures,[205–207] and optimizing the device structure[32,184] (i.e., vertical FET structure,[183] various p–n junctions[208,209]). The main factors to consider when engineering FETs with 2D semiconducting channels are as follows:

i) Metal/channel contact resistance. The performance of 2D materials FET is dominated by the resistance at this interface. Annealing and other interfacial engineering methods (such as doping) provide a possible route to minimize its effects.
ii) Dielectric environment. Traditional insulators (used either as gate dielectric or encapsulating dielectric) form a low quality interface with the 2D channel that is full of point defects. One potential alternative is to replace them by layered dielectrics such as h-BN or CaF_2.
iii) Channel length. The scaling of the channel length is affected by the thickness of the 2D material and the permittivity and thickness of the dielectric. By optimizing the dielectric environment, the short channel effect can be nearly suppressed for channel lengths of less than several nanometers.
iv) Channel thickness. Thinnest monolayer 2D materials are highly susceptible to scattering from extrinsic charged impurities. The performance of MoS_2 FETs with thin channels can be improved by interfacial cleanliness.
v) Temperature. Generally, the mobility of 2D materials channel decrease in the temperature range of 100–300 K. To achieve best room temperature performance, the thickness of the channel, the device structure and the dielectric environment are essential factors that need to be considered.

More research in these areas could accelerate the integration of 2D semiconductors into commercial FETs. Finally, we would like to emphasize that research papers that synthesize and manipulate 2D materials following scalable approaches compatible with the industry (such as CVD) will have a much higher impact on this technology.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

2D, field effect transistors, MoS_2, reliability, transition metal dichalcogenide

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