

Stochastic Modeling of the Impact of Random Dopants on Hot-Carrier Degradation in n-FinFETs

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Abstract— Using the deterministic version of our hot-carrier degradation (HCD) model, we perform a statistical analysis of the impact of random dopants (RDs) on the HCD in n-FinFETs. For this, we use an ensemble of 200 transistors with different configurations of RDs. Our analysis shows that changes in the linear drain currents have broad distributions, thereby resulting in broad distributions of device lifetimes. While lifetimes are nearly normally distributed at high stress biases, under voltages close to the operating regime, the distribution has a substantially different shape. This observation considerably complicates extrapolation from accelerated stress conditions, thereby suggesting that a comprehensive statistical treatment of the impact of RDs is required.

Index Terms— Hot-carrier degradation, random dopants, physical modeling, FinFETs, carrier transport, interface traps.

I. INTRODUCTION

ONE of the most detrimental reliability concerns in ultra-scaled field effect transistors (FETs) is hot-carrier degradation (HCD). Along these lines, HCD has been reported to be the main failure mode in the most recent FinFET node developed by Intel [1]. As a result, precise evaluation of device lifetime should include predictive modeling of HCD. Nevertheless, most HCD modeling approaches are empirical (i.e. rely on oversimplified expressions) and do not reveal the complex physical picture behind HCD. Herewith, they can only rely on backward extrapolation of device lifetime and fail when the physical mechanism driving HCD changes between stress and operating conditions. However, it is exactly this change that occurs in practice when the multiple-carrier (MC) mechanism of Si-H bond rupture becomes dominant at lower stress voltages, in contrast to higher voltages where the single-carrier (SC) process governs HCD [2]–[4].

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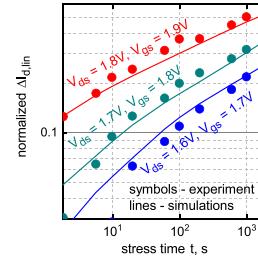


Fig. 1. The deterministic version of the model can accurately represent experimental $\Delta I_{d,\text{lin}}(t)$ traces. The data are from our previous publication [25].

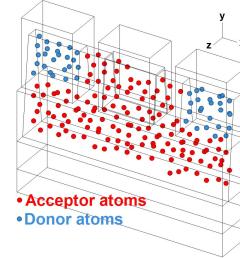


Fig. 2. A sketch of the FinFET with random dopants.

Another aspect which complicates modeling of reliability issues in modern FETs is the effect of random dopants (RDs). A nano-size transistor has just a handful of doping atoms with stochastically distributed locations [5]. Therefore, different samples from the same node inevitably have different configurations of RDs and the characteristics of pristine devices show substantial variability. Although nowadays some manufacturers (e.g. Intel [6], [7]) use significantly reduced channel doping to suppress RD induced fluctuations of device parameters, some other leading companies (such as IBM [8] and TSMC [9]) still employ FinFETs with “conventional” channel doping and therefore RD related variability still remains an issue.

Since HCD is driven by the interaction of hot and cold carriers [4], [10], [11] and is thus determined by the carrier energy distribution function (DF), degradation proceeds with different rates in various samples. This issue has been addressed experimentally [12]–[15] and in simulation approaches [16]–[19] by different groups. However, all previous simulation approaches only provide a statistical description of HCD based on some phenomenological models which do not reveal the complex physical picture behind HCD which includes also the impact of RDs. The only model so far which attempts to capture RD induced variability of HCD has been published by

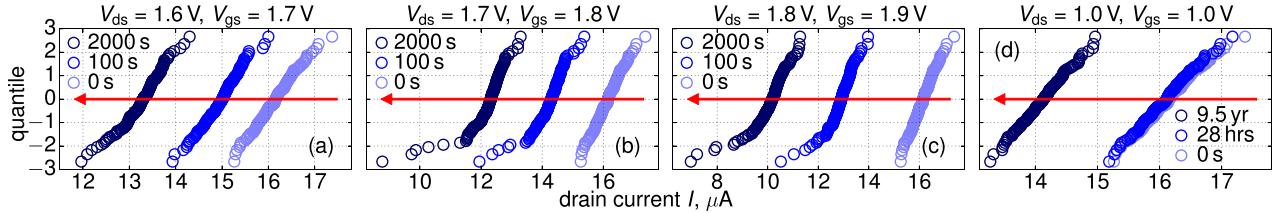


Fig. 3. The evolutions of the linear drain current distribution with time shown as probit plots for all four combinations of stress voltages. Data for $t = 0$ s correspond to pristine devices. Arrows correspond to increase of stress time.

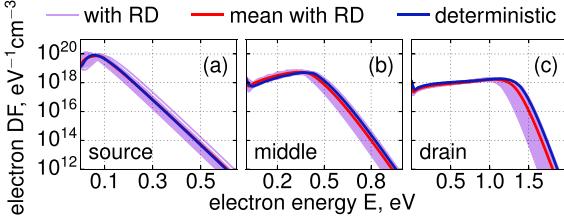


Fig. 4. Carrier DFs calculated for 200 RD configurations ($V_{ds} = 1.8$ V, $V_{gs} = 1.9$ V) and shown at the source (a), in the middle of the channel (b), and at the drain (c). For comparison deterministic and mean DFs are also depicted.

Bottini *et al.* [20]. This model, however, does not consider the interplay between SC and MC mechanisms of Si-H bond dissociation, which is of crucial importance for lifetime prediction.

To bridge this gap, we apply our physical HCD model which is based on a thorough carrier transport treatment [21], [22] to cover the effect of RDs on HCD. Preliminary results of such a statistical description of HCD have already been presented in our recent paper [23]. However, in the current work the analysis will be performed over a wider set of stress conditions and more detailed explanations will be given.

II. THE MODELING FRAMEWORK

Stochastic modeling of the effect of RDs on HCD will rely on the deterministic HCD model which has been shown to capture HCD in planar FETs [22], in high-voltage transistors [24], and in n-FinFETs [25]. This model (and the corresponding results) is referred to as “deterministic” because it employs continuous doping profiles (obtained by Sentaurus Process and labeled as “nominal”) for computing carrier energy DFs and does not consider RD related variability. The calculated DFs are used to describe the interplay of the SC and MC mechanisms of Si-H bond rupture and evaluate changes in device characteristics during stress (e.g. the normalized change of the linear drain current $\Delta I_{d,\text{lin}}$) as a function of stress time t (more details are given in [21], [22]).

In this study, we use n-channel FinFETs with a channel length $L_{ch} = 28$ nm (the corresponding gate length is $L_g = 40$ nm) and a high- k gate stack containing SiO₂ and HfO₂ layers with an equivalent oxide thickness of 1.2 nm. The operating voltage is $V_{dd} = 0.9$ V. Our deterministic HCD model has been shown in our recent publication [25] to accurately capture $\Delta I_{d,\text{lin}}(t)$ changes measured up to 2 ks under three stress conditions ($I_{d,\text{lin}}$ corresponds to $V_{ds} = 0.05$ V and $V_{gs} = 0.9$ V, where V_{ds} and V_{gs} are drain and gate voltages, respectively): $V_{ds} = 1.6$ V, $V_{gs} = 1.7$ V; $V_{ds} = 1.7$ V, $V_{gs} = 1.8$ V; and $V_{ds} = 1.8$ V, $V_{gs} = 1.9$ V (see Fig. 1 which presents data from [25]).

Based on the nominal architecture we generated a set of 200 devices with each of them having a unique configuration of RDs (see Fig. 2). To achieve this goal, for each

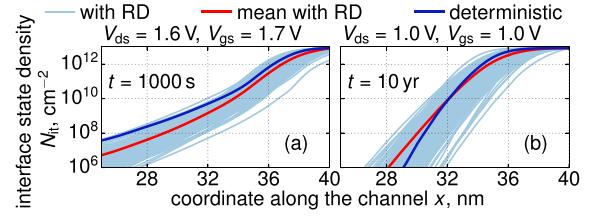


Fig. 5. N_{it} profiles for all 200 devices computed for $V_{ds} = 1.6$ V, $V_{gs} = 1.7$ V at $t = 1000$ s (a) and $V_{ds} = V_{gs} = 1.0$ V at 10 years (b).

mesh cell the continuous doping concentration is converted into the absolute number of doping atoms contained in that cell; this value is then used as the mean value for a Poisson random number generator which randomly draws the number of dopants in each of device realizations. For the entire set of pristine FinFETs we evaluated linear drain currents and binned them into probit plots (see Fig. 3) which show that currents are roughly normally distributed. These 200 configurations were used to calculate carrier energy DFs, interface state density (N_{it}) profiles, $\Delta I_{d,\text{lin}}(t)$ traces, and device lifetimes (τ). To obtain the DFs we solved the Boltzmann transport equation using the simulator ViennaSHE [26] which employs the spherical harmonics expansion method (for more details see [27], [28]). Note that all calculations have also been performed for stress voltages $V_{ds} = V_{gs} = 1.0$ V, which are close to the operating regime, in addition to the aforementioned high stress biases.

III. RESULTS AND DISCUSSIONS

The carrier DFs for the source, middle of the channel, and the drain obtained for all 200 RD configurations (at $V_{ds} = 1.8$ V, $V_{gs} = 1.9$ V) are summarized in Fig. 4. One can see that the nominal DFs have higher population numbers than the average over the ensemble. This trend is especially pronounced in the drain area (exactly where the damage is most severe) thereby suggesting that the deterministic model should result in overestimated HCD.

As for the N_{it} profiles, they are summarized for two regimes with $V_{ds} = 1.6$ V, $V_{gs} = 1.7$ V ($t = 1000$ s) and $V_{ds} = V_{gs} = 1.0$ V ($t \sim 10$ years) in Fig. 5. Note that for the sake of visibility the concentration N_{it} is shown near the drain peak (the drain corresponds to the lateral coordinate of $x = 40$ nm). From Fig. 5 we conclude that the deterministic model leads to N_{it} concentrations higher than average N_{it} values which is in accordance with the tendency visible in Fig. 4.

Fig. 3 shows evolutions of $I_{d,\text{lin}}$ distributions with stress time. One can see that for short stress times and/or lower voltages currents are approximately normally distributed. For example, in the case of $V_{ds} = 1.6$ V, $V_{gs} = 1.7$ V a deviation from the Gaussian distribution appears only after ~ 2 ks, while for higher V_{ds} , V_{gs} this non-normality is clearly visible already at $t = 100$ s. As for $V_{ds} = V_{gs} = 1.0$ V, the currents remain very closely normally distributed even after 10 years of stress.

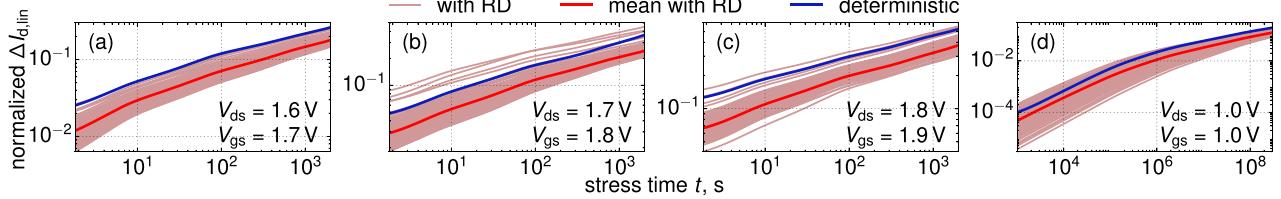


Fig. 6. Sets of $\Delta I_{d,\text{lin}}(t)$ traces show very broad distributions for all combinations of stress voltages. One can see that average (over the device ensemble) $\Delta I_{d,\text{lin}}$ values are significantly lower than those predicted with the deterministic version of our HCD model.

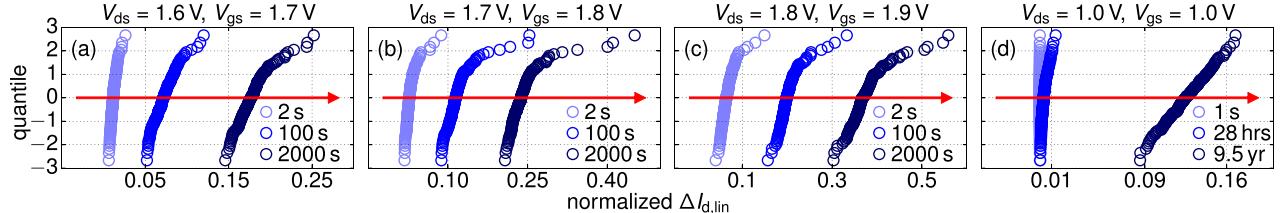


Fig. 7. Probit plots for $\Delta I_{d,\text{lin}}$ evaluated at three different stress time steps.

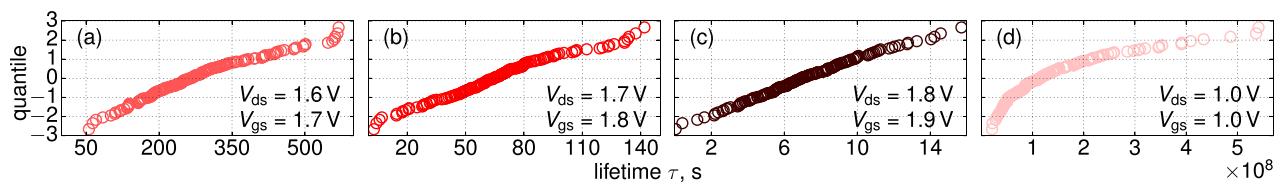


Fig. 8. Probit plots for device lifetimes extracted (based on the $\Delta I_{d,\text{lin}} = 10\%$ criterion) from degradation traces data shown in Fig. 6.

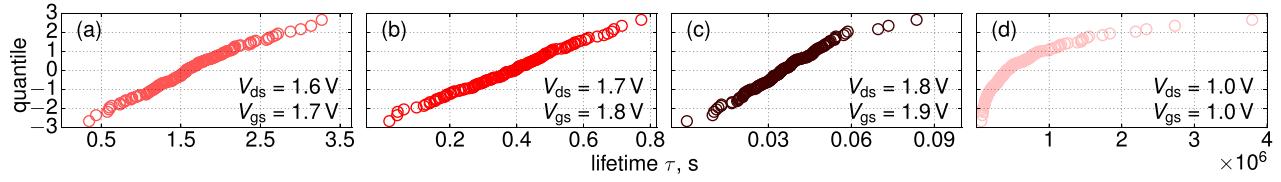


Fig. 9. Probit plots for device lifetimes extracted based on the $\Delta I_{d,\text{lin}} = 1\%$ criterion.

The sets of $\Delta I_{d,\text{lin}}(t)$ degradation traces are depicted in Fig. 6 which clearly shows that in these scaled FinFETs HCD cannot be simply described by a single degradation curve but by an entire set of $\Delta I_{d,\text{lin}}(t)$ dependences which can be very broad, thereby reflecting the impact of random dopants. Again, the mean $\Delta I_{d,\text{lin}}$ values are lower than the nominal ones. Fig. 7 shows $\Delta I_{d,\text{lin}}$ distributions evaluated for all V_{ds} , V_{gs} combinations at three stress time steps. For all regimes, $\Delta I_{d,\text{lin}}$ values are non-normally distributed (for $V_{ds} = V_{gs} = 1.0\text{ V}$ this non-normality becomes pronounced only at long t). This peculiarity is probably related to the fact that samples with low time-zero currents $I_{d,\text{lin}}(t=0)$ degrade slower and long t can result in smaller $\Delta I_{d,\text{lin}}$ values than with higher $I_{d,\text{lin}}(t=0)$ values. However, investigation of this hypothesis requires more studies which will be published elsewhere. The data presented in Fig. 6 allowed us to extract device lifetimes τ (determined as the time at which $\Delta I_{d,\text{lin}}$ reaches 10%) and bin them into distributions. Probit plots of these distributions (Fig. 8) show that for stress biases they are nearly normally distributed, while for $V_{ds} = V_{gs} = 1.0\text{ V}$ the distribution is significantly non-normal. For comparison, the τ distributions extracted based on the criterion of $\Delta I_{d,\text{lin}} = 1\%$ (instead of $\Delta I_{d,\text{lin}} = 10\%$ employed for Fig. 8) are summarized in Fig. 9. One can see that – although τ from Fig. 9 are shifted towards shorter values – the distributions from Fig. 8 and 9 have the same shapes at all combinations of V_{ds} , V_{gs} .

The trend that the deterministic HCD model results in HCD stronger than what is expected from the average over the FET ensemble is consistent with findings from [29], [30]. Studies of the impact of RDs on the drain current, mobility, and threshold voltage in unstressed devices showed that the

characteristics obtained for devices with continuous doping profiles significantly deviate from the mean values of these characteristics calculated taking the impact of RD into account. This effect is caused by the strong local perturbation of the device electrostatics by certain dopants. In the context of HCD, this perturbation depopulates the hot fraction of the carrier ensemble and thus weakens HCD.

IV. CONCLUSIONS

To analyze the effect of random dopants on hot-carrier degradation we generated a set of 200 n-channel FinFETs with different configurations of doping atoms. For each of these transistors we solved the Boltzmann transport equation and obtained carrier energy distribution functions. Then these DFs have been used to calculate ensembles of linear drain currents for each stress time step to extract degradation traces and device lifetimes. Our analysis has shown that $\Delta I_{d,\text{lin}}(t)$ traces have broad distributions and the deterministic version of the model (which considers only the continuous doping profiles without RD variations) results in $\Delta I_{d,\text{lin}}$ values higher than average (over the device ensemble) current changes. As for linear drain currents, they are normally distributed in the pristine device and at short stress times, showing substantial deviations from the normal distribution at longer t and/or higher voltages. Finally, lifetime distributions evaluated for stress conditions are close to normal, while for biases near the operating voltage the lifetime distribution has a completely different shape. This significantly complicates backward lifetime extrapolation and suggests that for a comprehensive HCD description which captures the effect of RD a full stochastic analysis is required.

REFERENCES

- [1] A. Rahman, J. Dacuna, P. Nayak, G. Leatherman, and S. Ramey, "Reliability studies of a 10 nm high-performance and low-power CMOS technology featuring 3rd generation FinFET and 5th generation HK/MG," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, pp. 6F.4-1–6F.4-6. doi: [10.1109/IRPS.2018.8353648](https://doi.org/10.1109/IRPS.2018.8353648).
- [2] W. McMahon and K. Hess, "A multi-carrier model for interface trap generation," *J. Comput. Electron.*, vol. 1, no. 3, pp. 395–398, Oct. 2002. doi: [10.1023/A:1020716111756](https://doi.org/10.1023/A:1020716111756).
- [3] A. Haggag, M. Lemanski, G. Anderson, P. Abramowitz, and M. Moosa, "Realistic projections of product Fmax shift and statistics due to HCI and NBTI," in *Proc. 45th Annu. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2007, pp. 93–96. doi: [10.1109/RELCPHY.2007.369874](https://doi.org/10.1109/RELCPHY.2007.369874).
- [4] A. Bravaix, C. Guerin, V. Huard, D. Roy, J. M. Roux, and E. Vincent, "Hot-carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2009, pp. 531–548. doi: [10.1109/IRPS.2009.5173308](https://doi.org/10.1109/IRPS.2009.5173308).
- [5] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: A 3-D density-gradient simulation study," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 722–729, Apr. 2001. doi: [10.1109/16.915703](https://doi.org/10.1109/16.915703).
- [6] S. Ramey, C. Prasad, and A. Rahman, "Technology scaling implications for BTI reliability," *Microelectron. Rel.*, vol. 82, pp. 42–50, Mar. 2018. doi: [10.1016/j.microrel.2018.01.004](https://doi.org/10.1016/j.microrel.2018.01.004).
- [7] C.-Y. Su, M. Armstrong, L. Jiang, S. A. Kumar, C. D. Landon, S. Liu, I. Meric, K. W. Park, L. Paulson, K. Phoa, B. Sell, J. Standfest, K. B. Sutaria, J. Wan, D. Young, and S. Ramey, "Transistor reliability characterization and modeling of the 22FFL FinFET technology," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, pp. 6F.8-1–6F.8-7. doi: [10.1109/IRPS.2018.8353652](https://doi.org/10.1109/IRPS.2018.8353652).
- [8] S. R. Stiffler, R. Ramachandran, W. K. Henson, N. D. Zamdmer, K. McStay, G. La Rosa, K. M. Boyd, S. Lee, C. Ortolland, and P. C. Parries, "Process technology for IBM 14-nm processor designs featuring silicon-on-insulator FinFETs," *IBM J. Res. Develop.*, vol. 62, nos. 2–3, pp. 11:1–11:7, Mar./May 2018. doi: [10.1147/JRD.2018.2800518](https://doi.org/10.1147/JRD.2018.2800518).
- [9] J. H. Lee, Y. M. Sheu, C. C. Wu, Y. M. Liu, Y. C. Chou, and S. C. Chin, "An electrical failure analysis (EFA) flow to quantitatively identify invisible defect on individual transistor: Using the characterization of random dopant fluctuation (RDF) as an example," in *Proc. IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, Jul. 2018, pp. 1–5. doi: [10.1109/IPFA.2018.8452513](https://doi.org/10.1109/IPFA.2018.8452513).
- [10] K. Hess, A. Haggag, W. McMahon, K. Cheng, J. Lee, and J. Lyding, "The physics of determining chip reliability," *IEEE Circuits Devices Mag.*, vol. 17, no. 3, pp. 33–38, May 2001. doi: [10.1109/101.933789](https://doi.org/10.1109/101.933789).
- [11] S. Tyaginov and T. Grasser, "Modeling of hot-carrier degradation: Physics and controversial issues," in *Proc. IEEE Int. Integr. Rel. Workshop Final Rep.*, Oct. 2012, pp. 206–215. doi: [10.1109/IIRW.2012.6468962](https://doi.org/10.1109/IIRW.2012.6468962).
- [12] P. Magnone, F. Crupi, N. Wils, H. P. Tuinhout, and C. Fiegna, "Characterization and modeling of hot-carrier-induced variability in subthreshold region," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2093–2099, Aug. 2012. doi: [10.1109/TED.2012.2200683](https://doi.org/10.1109/TED.2012.2200683).
- [13] E. R. Hsieh, S. S. Chung, C. H. Tsai, R. M. Huang, C. T. Tsai, and C. W. Liang, "New observations on the physical mechanism of V_{th}-variation in nanoscale CMOS devices after long term stress," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2011, pp. XT.9.1–XT.9.2. doi: [10.1109/IRPS.2011.5784610](https://doi.org/10.1109/IRPS.2011.5784610).
- [14] S. S. Chung, "The process and stress-induced variability issues of trigate CMOS devices," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, Jun. 2013, pp. 1–2. doi: [10.1109/EDSSC.2013.6628181](https://doi.org/10.1109/EDSSC.2013.6628181).
- [15] B. Kaczer, J. Franco, M. Cho, T. Grasser, P. J. Roussel, S. Tyaginov, M. Bina, Y. Wimmer, L. M. Procel, L. Trojman, F. Crupi, G. Pitner, V. Putcha, P. Weckx, E. Bury, Z. Ji, A. De Keersgieter, T. Chiarella, N. Horiguchi, G. Groeseneken, and A. Thean, "Origins and implications of increased channel hot carrier variability in nFinFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2015, pp. 3B.5.1–3B.5.6. doi: [10.1109/IRPS.2015.7112706](https://doi.org/10.1109/IRPS.2015.7112706).
- [16] S. J. Bae, S. J. Kim, W. Kuo, and P. H. Kvam, "Statistical models for hot electron degradation in nano-scaled MOSFET devices," *IEEE Trans. Rel.*, vol. 56, no. 3, pp. 392–400, Sep. 2007. doi: [10.1109/TR.2007.903232](https://doi.org/10.1109/TR.2007.903232).
- [17] Y. Li, S.-M. Yu, J.-R. Hwang, and F.-L. Yang, "Discrete dopant fluctuations in 20-nm/15-nm-gate planar CMOS," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1449–1455, Jun. 2008. doi: [10.1109/TED.2008.921991](https://doi.org/10.1109/TED.2008.921991).
- [18] L. Ma, X. Ji, Z. Chen, Y. Liao, F. Yan, Y. Song, and Q. Guo, "Physical understanding of hot carrier injection variability in deeply scaled nMOSFETs," in *Proc. Jpn. J. Appl. Phys.*, vol. 53, no. 4S, Jan. 2014, Art. no. 04EC15. doi: [10.7567/JJAP.53.04EC15](https://doi.org/10.7567/JJAP.53.04EC15).
- [19] T. Hillebrand, N. Hellwege, N. Heidmann, S. Paul, and D. Peters-Drolshagen, "Stochastic analysis of degradation and variations in CMOS-Transistors," in *Proc. ZuE GMM/ITG/GI-Symp. Rel. Design*, Sep. 2015, pp. 1–8.
- [20] R. Bottini, A. Ghetti, S. Vigano, M. G. Valentini, P. Murali, and C. Mouli, "Non-poissonian behavior of hot carrier degradation induced variability in MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, pp. 6E.7-1–6E.7-6. doi: [10.1109/IRPS.2018.8353645](https://doi.org/10.1109/IRPS.2018.8353645).
- [21] S. Tyaginov, M. Bina, J. Franco, D. Osintsev, O. Triebel, B. Kaczer, and T. Grasser, "Physical modeling of hot-carrier degradation for short-and long-channel MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2014, pp. XT.16-1–16-8. doi: [10.1109/IRPS.2014.6861193](https://doi.org/10.1109/IRPS.2014.6861193).
- [22] S. Tyaginov, M. Jech, J. Franco, P. Sharma, B. Kaczer, and T. Grasser, "Understanding and modeling the temperature behavior of hot-carrier degradation in SiON nMOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 84–87, Jan. 2016. doi: [10.1109/LED.2015.2503920](https://doi.org/10.1109/LED.2015.2503920).
- [23] A. Makarov, B. Kaczer, P. Roussel, A. Chasin, A. Grill, M. Vandemaele, G. Hellings, A.-M. El-Sayed, T. Grasser, D. Linten, and S. Tyaginov, "Modeling the effect of random dopants on hot-carrier degradation in FinFETs," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2019, pp. 6C.3.1–6C.3.6.
- [24] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.-M. Park, R. Minixhofer, H. Ceric, and T. Grasser, "Modeling of hot-carrier degradation in nLDMOS devices: Different approaches to the solution of the Boltzmann transport equation," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1811–1818, Jun. 2015. doi: [10.1109/TED.2015.2421282](https://doi.org/10.1109/TED.2015.2421282).
- [25] A. Makarov, S. E. Tyaginov, B. Kaczer, M. Jech, A. Chasin, A. Grill, G. Hellings, M. Vexler, D. Linten, and T. Grasser, "Hot-carrier degradation in FinFETs: Modeling, peculiarities, and impact of device topology," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.1.1–13.1.4. doi: [10.1109/IEDM.2017.8268381](https://doi.org/10.1109/IEDM.2017.8268381).
- [26] ViennaSHE. (2014). [Online]. Available: <http://viennashe.sourceforge.net/>
- [27] K. Rupp, T. Grasser, and A. Jüngel, "On the feasibility of spherical harmonics expansions of the Boltzmann transport equation for three-dimensional device geometries," in *IEDM Tech. Dig.*, Dec. 2011, pp. 34.1.1–34.1.4. doi: [10.1109/IEDM.2011.6131667](https://doi.org/10.1109/IEDM.2011.6131667).
- [28] M. Bina, K. Rupp, S. Tyaginov, O. Triebel, and T. Grasser, "Modeling of hot carrier degradation using a spherical harmonics expansion of the bipolar Boltzmann transport equation," in *IEDM Tech. Dig.*, Dec. 2012, pp. 30.5.1–30.5.4. doi: [10.1109/IEDM.2012.6479138](https://doi.org/10.1109/IEDM.2012.6479138).
- [29] A. Asenov, R. Balasubramaniam, A. R. Brown, J. H. Davies, and S. Saini, "Random telegraph signal amplitudes in sub 100 nm (decanano) MOSFETs: A 3D 'Atomistic' simulation study," in *IEDM Tech. Dig.*, Dec. 2000, pp. 279–282. doi: [10.1109/IEDM.2000.904311](https://doi.org/10.1109/IEDM.2000.904311).
- [30] A. Asenov, F. Adamu-Lema, X. Wang, and S. M. Amoroso, "Problems with the continuous doping TCAD simulations of decanometer CMOS transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2745–2751, Aug. 2014. doi: [10.1109/TED.2014.2332034](https://doi.org/10.1109/TED.2014.2332034).