

Bi-Modal Variability of nFinFET Characteristics During Hot-Carrier Stress: A Modeling Approach

Alexander Makarov¹, Ben Kaczer¹, Adrian Chasin, Michiel Vandemaele¹, Erik Bury, Markus Jech¹, Alexander Grill, Geert Hellings¹, Al-Moatasem El-Sayed, Tibor Grasser¹, *Fellow, IEEE*, Dimitri Linten, and Stanislav Tyaginov

Abstract— We present a statistical analysis of the cumulative impact of random traps (RTs) and dopants (RDs) on hot-carrier degradation (HCD) in n-channel FinFETs. Calculations are performed at three combinations of high stress voltages and for conditions close to the operating regime. We generate 200 different configurations of devices with RDs and subsequently solve the Boltzmann transport equation to obtain the continuous interface trap concentration N_{it} . These deterministic densities N_{it} for each individual configuration are randomized and converted to 200 different configurations of RTs, yielding a total amount of 40,000 samples in our study. The analysis shows that at high stress voltages (with both RTs and RDs taken into account) probability densities of linear drain currents and device lifetimes are close to a bi-modal normal distribution, while in the operating regime such a trend is not visible.

Index Terms— Hot-carrier degradation, random traps, random dopants, variability, physical modeling, FinFETs, carrier transport, interface traps.

I. INTRODUCTION

IN SCALED field-effect transistors (FETs) with dimensions shrunk beyond the sub-decananometer range, sample-to-sample variability of device characteristics becomes an important issue. Such statistical scatter can be due to various reasons, including fluctuations in the oxide thickness [1], [2], disorder at the semiconductor/dielectric interface [3], work-function variations [4], and random placement of doping atoms [5]. Although in mature technologies the first three concerns are mitigated, the problem of random dopant (RD) variability still persists and has been reported by semiconductor manufacturers [6], [7]. Moreover, a deterministic description of reliability issues in short-channel devices is not sufficient because degradation is driven by generation of discrete random

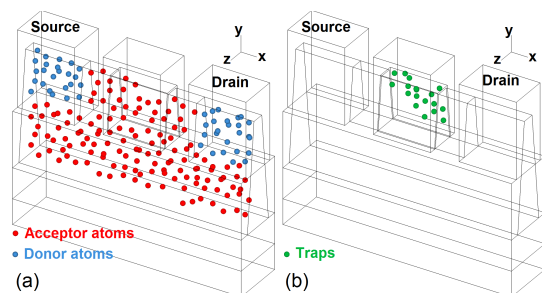


Fig. 1. A schematic representation of RDs (a) and RTs (b) in the FinFET.

traps (RTs) which results in time-dependent variability of device characteristics [8], [9].

Among reliability issues, hot-carrier degradation (HCD) has repeatedly been reported [10], [11] to be the most detrimental one. Nevertheless, there is a very limited number of letter presenting experimental investigations of variability induced by HCD [9], [12]–[14]. The few modeling approaches to HCD variability are limited to phenomenological descriptions and do not address the complex physical picture of HCD [15]–[18]. To the best of our knowledge, the only model which employs a physics-based description of HCD variability has been used in a recent letter by Bottini *et al.* [19]. However, this approach considers only the single-carrier (SC) mechanism of the reaction transforming neutral precursors (Si-H bonds) to electrically active traps (P_b centers). This is because the authors of [19] investigate HCD in devices stressed at high voltages where the SC-mechanism is dominant. However, in ultra-scaled devices, HCD is governed by a mixture of SC- and multiple-carrier (MC) processes [20]–[22] and therefore the MC-mechanism must also be considered.

In our recent publications we performed a statistical analysis of the impact of RDs on HCD in FinFETs [23], [24]. However, this analysis did not address RT induced variability and therefore the subject of this work is to extend our approach to capture also the impact of RTs on HCD.

II. THE MODELING FRAMEWORK

The statistical analysis of HCD is based on our deterministic model for HCD [21], [25]. This model assumes that HCD is driven by the reaction which converts Si-H bonds (neutral precursors) to Si dangling bonds (electrically active traps). Bond rupture is driven by two competing pathways, i.e. by MC- and SC-mechanisms, which are self-consistently modeled within

Manuscript received July 17, 2019; revised August 3, 2019; accepted August 5, 2019. Date of publication August 7, 2019; date of current version September 25, 2019. This work was supported in part by the European Union's Horizon 2020 Research and Innovation Programme through the Marie Skłodowska-Curie Grant 794950 and in part by the Austrian Science Fund (FWF) under Grant P31204-N30. The review of this letter was arranged by Editor E. A. Gutiérrez-D. (Corresponding author: Alexander Makarov.)

A. Makarov, M. Jech, A.-M. El-Sayed, and T. Grasser are with the Institute for Microelectronics, Technische Universität Wien, 1040 Vienna, Austria (e-mail: makarov@iue.tuwien.ac.at).

B. Kaczer, A. Chasin, A. Grill, M. Vandemaele, E. Bury, G. Hellings, D. Linten, and S. Tyaginov are with IMEC, Leuven 3001, Belgium.

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2019.2933729

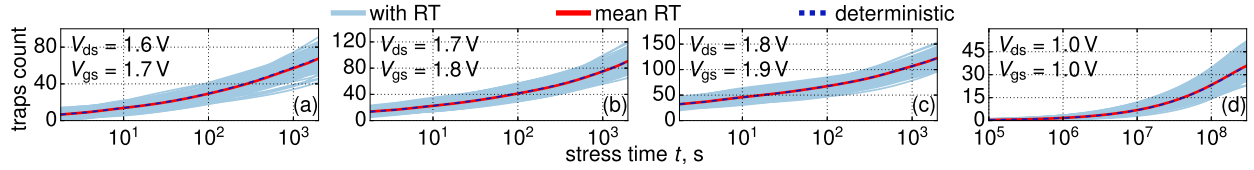


Fig. 2. The total number of interface traps generated during HC stress for all four combinations of stress voltages. Plotted are numbers for each particular “sample”, the average (over the ensemble) value, and the number of traps obtained with the continuous N_{it} (labeled deterministic).

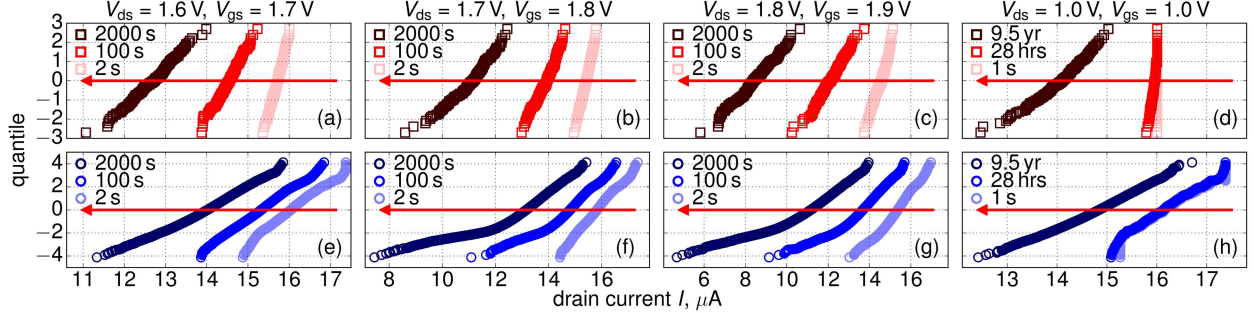


Fig. 3. Probit plots of $I_{d,lin}$ distributions for three stress time steps for all combinations of applied voltages computed with the impact of RTs only (upper row) and considering the cumulative impact of RTs and RDs (lower row).

our framework. The rates of these processes are calculated based on carrier energy distribution functions (DFs) [26]. The bonding energy is considered to be a normally distributed quantity with the mean value $\langle E_a \rangle$ of 2.56 eV and the standard deviation σ_E determined by the device fabrication process. Let us emphasize that this value of $\langle E_a \rangle$ corresponds to the stretching vibrational mode of the Si-H bond (more details are given in [25]) and is consistent with experimental data [27]. Note that we do not consider charge trapping by border traps. This is because our previous studies conducted using the same FinFETs as in this work [28] showed no recovery of the degradation traces after removal of HC stress, while charge capture by border traps results in recoverable damage [8].

This deterministic model was calibrated against HCD data over a wide class of devices including high-voltage transistors [29] and FinFETs [30]. The latter devices – nFinFETs with a channel length of 28 nm, high- k stack consisting of SiO₂ and HfO₂ layers with an EOT of 1.2 nm, and an operating voltage $V_{dd} = 1.0$ V – are used in the current study. The continuous doping profiles were obtained with the Sentaurus Process simulator; this device structure was used to calibrate the deterministic version of the model [30] (the corresponding results are labeled as “deterministic” or “nominal”).

In our previous publication [30] we showed that the deterministic model can accurately reproduce relative changes of the linear drain current $\Delta I_{d,lin}$ ($I_{d,lin}$ corresponds to the drain voltage V_{ds} of 0.05 V and the gate voltage V_{gs} of 1.0 V) recorded during HC stress at three combinations of stress voltages: $V_{gs} = 1.7$ V, $V_{ds} = 1.6$ V; $V_{gs} = 1.8$ V, $V_{ds} = 1.7$ V and $V_{gs} = 1.9$ V, $V_{ds} = 1.8$ V. Model calibration was performed by adjusting only four model parameters: the cross sections of the SC- and MC-mechanisms, the concentration of pristine Si-H bonds ($N_{Si-H}^{(0)}$) as well as the standard deviation σ_E . The values obtained are: $N_{Si-H}^{(0)} \sim 6 \times 10^{12} \text{ cm}^{-3}$ and $\sigma_E = 0.35$ eV; as for the cross sections, they are $\sim 10^{-17} \text{ cm}^2$ and $\sim 5 \times 10^{-19} \text{ cm}^2$ for the SC- and MC-mechanisms, respectively (these cross sections are close to those reported in [25]). In this study we use the aforementioned pairs of $\{V_{gs}, V_{ds}\}$ as well

as a milder “stress” regime at the expected operating V_{dd} , i.e. $V_{gs} = V_{ds} = 1.0$ V.

Then the structure with continuous doping profiles was subjected to randomization and 200 “samples” with different configurations of RDs were generated (Fig. 1a); more details are given in [23], [24]. For each of these samples we solved the Boltzmann transport equation, obtained carrier DFs and then calculated the continuous interface state densities N_{it} for each point at the Si/SiO₂ interface and each stress time step t . These concentrations were then converted to average numbers of traps contained in each mesh cell (evaluated as a product of local N_{it} and the 2D cell area) and randomized using a Poisson random number generator. An important aspect of this procedure was to ensure that the number of traps in each mesh cell does not decrease with time, i.e. traps which were created in a previous step do not further disappear due to randomization artifacts. Note that for each continuous density N_{it} , 200 “samples” with discrete traps were created resulting in a total of $200 \times 200 = 40,000$ “samples” (each with a unique configuration of RDs and RTs at each t).

III. RESULTS AND DISCUSSIONS

Fig. 2 shows the total numbers of interface traps (in the entire devices) plotted vs. t for each “sample”. One can see that the average (over the ensemble) number of interface traps coincides with the number evaluated with the continuous concentration N_{it} . Fig. 3 depicts distributions of the linear drain current $I_{d,lin}$ (corresponds to $V_{ds} = 0.05$ V and $V_{gs} = V_{dd}$) evaluated for three stress time steps ($t = 2, 100$, and 2000 s) with the impact of RTs only and with the combined impact of RDs and RTs. If only RTs are taken into account the currents are almost normally distributed with some deviations appearing at longer t or higher stress biases (note that the $I_{d,lin}$ distributions obtained with the impact of RDs show a similar behavior [24]). If the impact of RDs is also taken into account, the distributions demonstrate bi-modality, which is not pronounced at $V_{gs} = V_{ds} = 1.0$ V.

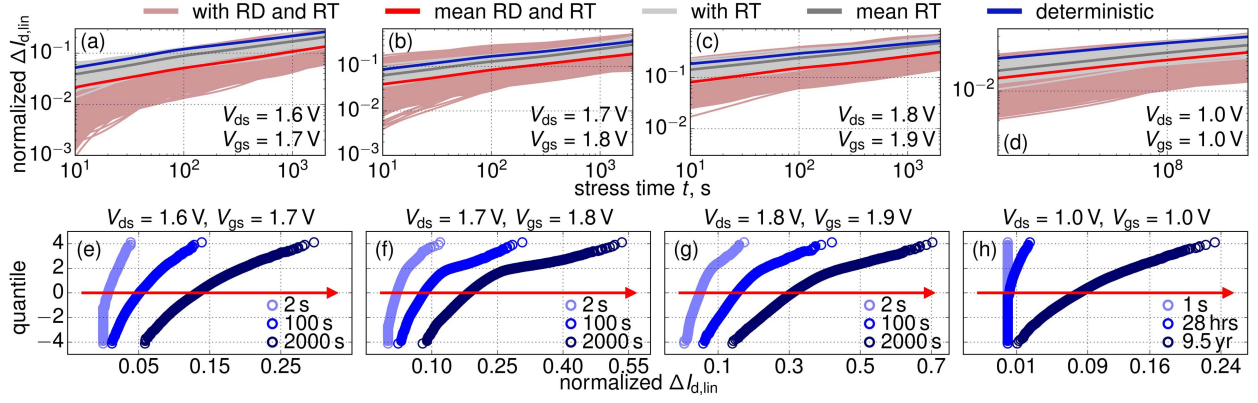


Fig. 4. Ensembles of $\Delta I_{d,lin}(t)$ traces (upper row) and evolutions of the $\Delta I_{d,lin}$ distributions (lower row) with time modeled for all combinations of applied voltages.

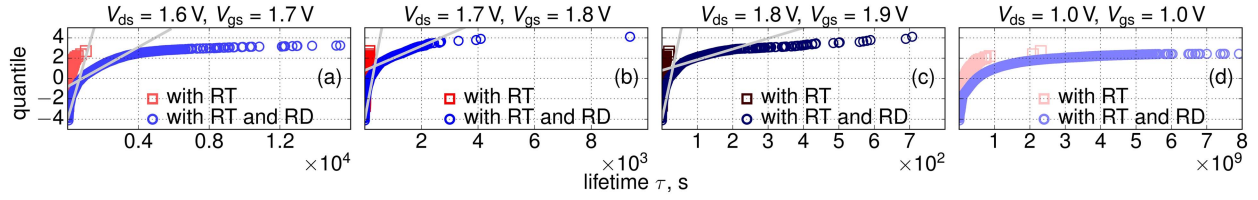


Fig. 5. Probit plots of device lifetime distributions obtained with the impact of RTs only (square symbols) and considering the cumulative effect of RTs and RDs (circles).

Another important feature visible in Fig. 3 is that the impact of RDs widens the distributions and shifts them towards higher $I_{d,lin}$ values. In other words, the impact of RDs weakens HCD and broadens statistical variations of degradation characteristics; such a behavior is consistent with our results reported in [23], [24], [31].

Fig. 4 shows the ensembles of normalized (to the $I_{d,lin}(t=0)$ value) changes in the linear drain current $\Delta I_{d,lin}$ with time as well as the probability densities of $\Delta I_{d,lin}$ calculated for the same stress time steps as in Fig. 3. From Fig. 4 one can see that considering RDs widens the ensembles of $\Delta I_{d,lin}(t)$ traces and leads to average (over the entire ensemble) $\langle \Delta I_{d,lin}(t) \rangle$ curves with values lower than predicted by the deterministic model (see [23], [24] for details). As for $\Delta I_{d,lin}$ distributions, they are close to a bi-modal normal distribution and this behavior becomes more prominent under more severe stresses; at $V_{gs} = V_{ds} = 1.0$ V the bi-modality is not pronounced.

The $\Delta I_{d,lin}(t)$ traces from Fig. 4 were used to extract device lifetimes (based on the criterion $\Delta I_{d,lin} = 0.1$) which are arranged into probit plots, Fig. 5. From the lifetime probability densities we conclude that the impact of RTs and RDs leads to two different slopes of the bi-modal normal distributions obtained at higher V_{ds} , V_{gs} . This tendency is consistent with recently published measurement results and with the multi-modal defect-centric framework [32]. However, at $V_{gs} = V_{ds} = 1.0$ V the lifetime distribution has a substantially different shape and the bi-modality is not pronounced. This significantly complicates backward lifetime extrapolation from stress conditions to the operating regime and confirms that a full stochastic treatment of HCD is required.

The bi-modality featured by the $I_{d,lin}$, $\Delta I_{d,lin}$, and lifetime distributions stems from the impacts of RDs and RTs. Indeed,

RDs are distributed throughout the device bulk and determine the electrostatics of the entire device. In contrast, RTs are located at the interface and their density N_{it} peaks near the device drain, thereby impacting the device electrostatics and the carrier mobility only locally. Let us emphasize that in all cases the bi-modality is pronounced only at high stress voltages or long stress times, i.e. during weak/short HC stress the impact of RTs on the aforementioned distributions is less pronounced. This is because at weak stress the MC-mechanism is dominant and creates damage which is less localized compared to the typical mixture of MC- and SC-mechanisms (N_{it} can be high even near the source [33]–[35]). This scenario is very similar to variability induced by bias temperature instability, which is reduced compared to HCD variability, as we discussed in [9].

IV. CONCLUSION

We performed a statistical analysis of the cumulative impact of randomly generated (during hot-carrier stress) traps and random dopants on n-channel FinFET characteristics. We showed that at higher V_{gs} , V_{ds} conditions, $I_{d,lin}$, $\Delta I_{d,lin}$, and device lifetimes obey bi-modal normal distributions, while at $V_{gs} = V_{ds} = 1.0$ V the bi-modality is not visible. This hinders projections to operating conditions and lifetime extrapolation and suggests that stochastic treatment of HCD is needed.

REFERENCES

- [1] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 112–119, Jan. 2002. doi: [10.1109/16.974757](https://doi.org/10.1109/16.974757).
- [2] S. E. Tyaginov, M. I. Vexler, A. F. Shulekin, and I. V. Grekhov, "Statistical analysis of tunnel currents in scaled MOS structures with a non-uniform oxide thickness distribution," *Solid-State Electron.*, vol. 49, no. 7, pp. 1192–1197, 2005. doi: [10.1016/j.sse.2005.04.007](https://doi.org/10.1016/j.sse.2005.04.007).

- [3] A. R. Brown, J. R. Watling, A. Asenov, G. Bersuker, and P. Zeitloff, "Intrinsic parameter fluctuations in MOSFETs due to structural non-uniformity of high- κ gate stack materials," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices*, Sep. 2005, pp. 27–30. doi: [10.1109/SISPAD.2005.201464](https://doi.org/10.1109/SISPAD.2005.201464).
- [4] H. Nam and C. Shin, "Study of high- k /metal-gate work-function variation using Rayleigh distribution," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 532–534, Apr. 2013. doi: [10.1109/LED.2013.2247376](https://doi.org/10.1109/LED.2013.2247376).
- [5] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D 'atomistic' simulation study," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2505–2513, Dec. 1998. doi: [10.1109/16.735728](https://doi.org/10.1109/16.735728).
- [6] S. R. Stiffler, R. Ramachandran, W. K. Henson, N. D. Zamdmer, K. McStay, G. La Rosa, K. M. Boyd, S. Lee, C. Ortoland, and P. C. Parries, "Process technology for IBM 14-nm processor designs featuring silicon-on-insulator FinFETs," *IBM J. Res. Develop.*, vol. 62, nos. 2–3, pp. 11:1–11:7, Mar./May 2018. doi: [10.1147/JRD.2018.2800518](https://doi.org/10.1147/JRD.2018.2800518).
- [7] J. H. Lee, Y. M. Shcu, C. C. Wu, Y. M. Liu, Y. C. Chou, and S. C. Chin, "An electrical failure analysis (EFA) flow to quantitatively identify invisible defect on individual transistor: Using the characterization of random dopant fluctuation (RDF) as an example," in *Proc. IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA)*, Jul. 2018, pp. 1–5. doi: [10.1109/IPFA.2018.8452513](https://doi.org/10.1109/IPFA.2018.8452513).
- [8] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," *Microelectron. Rel.*, vol. 52, no. 1, pp. 39–70, Jan. 2012. doi: [10.1016/j.microrel.2011.09.002](https://doi.org/10.1016/j.microrel.2011.09.002).
- [9] B. Kaczer, J. Franco, M. Cho, T. Grasser, P. J. Roussel, S. Tyaginov, M. Bina, Y. Wimmer, L. M. Procel, L. Trojman, F. Crupi, G. Pitner, V. Putcha, P. Weckx, E. Bury, Z. Ji, A. De Keersgieter, T. Chiarella, N. Horiguchi, G. Groeseneken, and A. Thean, "Origins and implications of increased channel hot carrier variability in nFinFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, Monterey, CA, USA, Apr. 2015, pp. 3B.5.1–3B.5.6. doi: [10.1109/IRPS.2015.7112706](https://doi.org/10.1109/IRPS.2015.7112706).
- [10] A. Rahman, J. Dacuna, P. Nayak, G. Leatherman, and S. Ramey, "Reliability studies of a 10nm high-performance and low-power CMOS technology featuring 3rd generation FinFET and 5th generation HK/MG," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, pp. 6F.4.1–6F.4.6. doi: [10.1109/IRPS.2018.8353648](https://doi.org/10.1109/IRPS.2018.8353648).
- [11] P. Paliwoda, Z. Chbili, A. Kerber, T. Nigam, K. Nagahiro, S. Cimino, M. Toledano-Luque, L. Pantisano, B. W. Min, and D. Misra, "Self-heating effects on hot carrier degradation and its impact on logic circuit reliability," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 2, pp. 249–254, Jun. 2019. doi: [10.1109/TDMR.2019.2916230](https://doi.org/10.1109/TDMR.2019.2916230).
- [12] P. Magnone, F. Crupi, N. Wils, H. P. Tuinhout, and C. Fiegna, "Characterization and modeling of hot carrier-induced variability in subthreshold region," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2093–2099, Aug. 2012. doi: [10.1109/TED.2012.2200683](https://doi.org/10.1109/TED.2012.2200683).
- [13] E. R. Hsieh, S. S. Chung, C. H. Tsai, R. M. Huang, C. T. Tsai, and C. W. Liang, "New observations on the physical mechanism of V_{th} variation in nanoscale CMOS devices after long term stress," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2011, pp. XT.9.1–XT.9.2. doi: [10.1109/IRPS.2011.5784610](https://doi.org/10.1109/IRPS.2011.5784610).
- [14] S. S. Chung, "The process and stress-induced variability issues of trigate CMOS devices," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, Jun. 2013, pp. 1–2. doi: [10.1109/EDSSC.2013.6628181](https://doi.org/10.1109/EDSSC.2013.6628181).
- [15] S. J. Bae, S. J. Kim, W. Kuo, and P. H. Kvam, "Statistical models for hot electron degradation in nano-scaled MOSFET devices," *IEEE Trans. Rel.*, vol. 56, no. 3, pp. 392–400, Sep. 2007. doi: [10.1109/TR.2007.903232](https://doi.org/10.1109/TR.2007.903232).
- [16] Y. Li, S.-M. Yu, J.-R. Hwang, and F.-L. Yang, "Discrete dopant fluctuations in 20-nm/15-nm-gate planar CMOS," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1449–1455, Jun. 2008. doi: [10.1109/TED.2008.921991](https://doi.org/10.1109/TED.2008.921991).
- [17] L. Ma, X. Ji, Z. Chen, Y. Liao, F. Yan, Y. Song, and Q. Guo, "Physical understanding of hot carrier injection variability in deeply scaled nMOSFETs," *Jpn. J. Appl. Phys.*, vol. 53, no. 4S, Jan. 2014, Art. no. 04EC15. doi: [10.7567/JJAP.53.04EC15](https://doi.org/10.7567/JJAP.53.04EC15).
- [18] T. Hillebrand, N. Hellwege, N. Heidmann, S. Paul, and D. Peters-Drolshagen, "Stochastic analysis of degradation and variations in CMOS-Transistors," in *Proc. ZuE GMM/ITG/GI-Symp. Rel. Design*, Sep. 2015, pp. 1–8.
- [19] R. Bottini, A. Ghetti, S. Vigano, M. G. Valentini, P. Murali, and C. Mouli, "Non-poissonian behavior of hot carrier degradation induced variability in MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2018, pp. 6E.7.1–6E.7.6. doi: [10.1109/IRPS.2018.8353645](https://doi.org/10.1109/IRPS.2018.8353645).
- [20] S. Tyaginov, M. Bina, J. Franco, D. Osintsev, O. Triebel, B. Kaczer, and T. Grasser, "Physical modeling of hot-carrier degradation for short- and long-channel MOSFETs," in *Proc. Int. Rel. Phys. Symp. (IRPS)*, 2014, pp. XT.16.1–XT.16.8. doi: [10.1109/IRPS.2014.6861193](https://doi.org/10.1109/IRPS.2014.6861193).
- [21] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, D. Osintsev, B. Kaczer, and T. Grasser, "A predictive physical model for hot-carrier degradation in ultra-scaled MOSFETs," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices (SISPAD)*, 2014, pp. 89–92. doi: [10.1109/SISPAD.2014.6931570](https://doi.org/10.1109/SISPAD.2014.6931570).
- [22] Y. M. Randriamihaja, X. Federspiel, V. Huard, A. Bravaix, and P. Palestri, "New Hot Carrier degradation modeling reconsidering the role of EES in ultra short N-channel MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2013, pp. XT.1.1–XT.1.5. doi: [10.1109/IRPS.2013.6532116](https://doi.org/10.1109/IRPS.2013.6532116).
- [23] A. Makarov, B. Kaczer, P. Roussel, A. Chasin, A. Grill, M. Vandemaele, G. Hellings, A.-M. El-Sayed, T. Grasser, D. Linten, and S. Tyaginov, "Modeling the effect of random dopants on hot-carrier degradation in FinFETs," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar./Apr. 2019, pp. 1–7. doi: [10.1109/IRPS.2019.8720584](https://doi.org/10.1109/IRPS.2019.8720584).
- [24] A. Makarov, B. Kaczer, P. Roussel, A. Chasin, A. Grill, M. Vandemaele, G. Hellings, A.-M. El-Sayed, T. Grasser, D. Linten, and S. Tyaginov, "Stochastic modeling of the impact of random dopants on hot-carrier degradation in n-FinFETs," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 870–873, Jun. 2019. doi: [10.1109/LED.2019.2913625](https://doi.org/10.1109/LED.2019.2913625).
- [25] S. Tyaginov, M. Jech, J. Franco, P. Sharma, B. Kaczer, and T. Grasser, "Understanding and modeling the temperature behavior of hot-carrier degradation in SiON nMOSFETs," *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 84–87, Jan. 2016. doi: [10.1109/LED.2015.2503920](https://doi.org/10.1109/LED.2015.2503920).
- [26] M. Bina, K. Rupp, S. Tyaginov, O. Triebel, and T. Grasser, "Modeling of hot carrier degradation using a spherical harmonics expansion of the bipolar Boltzmann transport equation," in *IEDM Tech. Dig.*, Dec. 2012, pp. 30.5.1–30.5.4. doi: [10.1109/IEDM.2012.6479138](https://doi.org/10.1109/IEDM.2012.6479138).
- [27] K. L. Brower, "Dissociation kinetics of hydrogen-passivated (111) Si-SiO₂ interface defects," *Phys. Rev. B, Condens. Matter*, vol. 42, no. 6, pp. 3444–3454, 1990. doi: [10.1103/PhysRevB.42.3444](https://doi.org/10.1103/PhysRevB.42.3444).
- [28] A. Chasm, J. Franco, R. Ritzenthaler, G. Hellings, M. Cho, Y. Sasaki, A. Subirats, P. Roussel, B. Kaczer, D. Linten, N. Horiguchi, G. Groeseneken, and A. Thean, "Hot-carrier analysis on nMOS Si FinFETs with solid source doped junction," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Pasadena, CA, USA, Apr. 2016, pp. 4B.4.1–4B.4.6. doi: [10.1109/IRPS.2016.7574535](https://doi.org/10.1109/IRPS.2016.7574535).
- [29] P. Sharma, S. Tyaginov, Y. Wimmer, F. Rudolf, K. Rupp, M. Bina, H. Enichlmair, J.-M. Park, R. Minixhofer, H. Ceric, and T. Grasser, "Modeling of hot-carrier degradation in nLDMOS devices: Different approaches to the solution of the Boltzmann transport equation," *IEEE Trans. Electron Devices*, vol. 62, no. 6, pp. 1811–1818, Jun. 2015. doi: [10.1109/TED.2015.2421282](https://doi.org/10.1109/TED.2015.2421282).
- [30] A. Makarov, S. E. Tyaginov, B. Kaczer, M. Jech, A. Chasin, A. Grill, G. Hellings, M. Vexler, D. Linten, and T. Grasser, "Hot-carrier degradation in FinFETs: Modeling, peculiarities, and impact of device topology," in *IEDM Tech. Dig.*, Dec. 2017, pp. 13.1.1–13.1.4. doi: [10.1109/IEDM.2017.8268381](https://doi.org/10.1109/IEDM.2017.8268381).
- [31] A. Makarov, B. Kaczer, P. Roussel, A. Chasin, M. Vandemaele, G. Hellings, A.-M. El-Sayed, M. Jech, T. Grasser, D. Linten, and S. Tyaginov, "Stochastic modeling of hot-carrier degradation in nFinFETs considering the impact of random traps and random dopants," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, to be published.
- [32] E. Bury, A. Chasin, K.-H. Chuang, M. Vandemaele, S. V. Beek, J. Franco, B. Kaczer, and D. Linten, "Array-based statistical characterization of CMOS degradation modes and modeling of the time-dependent variability induced by different stress patterns in the VG,VD bias space," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar./Apr. 2019, pp. 1–6. doi: [10.1109/IRPS.2019.8720592](https://doi.org/10.1109/IRPS.2019.8720592).
- [33] Y. Randriamihaja, V. Huard, X. Federspiel, A. Zaka, P. Palestri, D. Rideau, and A. Bravaix, "Microscopic scale characterization and modeling of transistor degradation under HC stress," *Microelectron. Rel.*, vol. 52, no. 11, pp. 2513–2520, 2012. doi: [10.1016/j.microrel.2012.04.005](https://doi.org/10.1016/j.microrel.2012.04.005).
- [34] M. Bina, S. Tyaginov, J. Franco, Y. Wimmer, D. Osintsev, B. Kaczer, and T. Grasser, "Predictive hot-carrier modeling of n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3103–3110, Sep. 2014. doi: [10.1109/TED.2014.2340575](https://doi.org/10.1109/TED.2014.2340575).
- [35] Z. Sun, Z. Yu, Z. Zhang, J. Zhang, R. Wang, P. Lu, and R. Huang, "Investigation on the lateral trap distributions in nanoscale MOSFETs during hot carrier stress," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 490–493, Apr. 2019. doi: [10.1109/LED.2019.2897728](https://doi.org/10.1109/LED.2019.2897728).