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An improved read-assist energy efficient single ended P-P-N based 10T SRAM cell for wireless sensor network

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ABSTRACT

In this paper, a novel single ended PPN based 10T static random access memory (SRAM) with high read stability is presented. The proposed cell is energy efficient with double ended write, and single-ended read decoupled circuit for wireless sensor networks. The proposed 10T SRAM cell has a significant improvement in READ and WRITE stability with the least energy consumption. To evaluate the performance of the cells static noise margin, delay, power dissipation, leakage current, and area are calculated using the cadence environment at a standard CMOS 45 nm process technology. The simulation results show that it has enhancement of 83.4%, 50.14%, 43.3%, 50.14% and 3.09% on read SNM when compared with the conventional 6T, ST11T, ST1, ST2, and PPN 10T respectively at 1 V supply voltage. The proposed cell also achieves write SNM of 1.29×, 1.12×, and 1.18× higher compared to 6T, PPN10T, and ST11T, respectively. For a better perspective, we have proposed a figure of merit considering all the performance parameters, and it is observed that the proposed cell has better the FOM as compared to all other considered cells.

1. Introduction

The increasing demand for portable battery operated devices has made energy efficient processors a necessity. System designing of many digital applications such as wearable computing devices, object tracking systems, wireless sensors, etc. requires the energy efficiency at the topmost priority [1]. These embedded systems require repeated charging of their batteries. The problem is more critical in the wireless sensor networks which are used for monitoring the environmental parameters. These wireless systems may not have regular access for recharging of their batteries. As we know, on-chip memories determine the power dissipation of the system on chip (SoC) designs. Therefore, the design of energy efficient and stable SRAM is the main concern these days as they are mainly used for on-chip memories and covers a maximum portion of the chip. In addition to energy saving in SRAMs, researchers are also taking care of the performance parameters such as static noise margin (SNM), delay, and area for better performance of the cell. But, achieving robust and reliable design is a difficult task because of the trade-off between several performance parameters of SRAM cell [2,3]. Interdependency of area and stability restricts to design a system that has low area and high stability. The trade-off between power and delay is another design challenge to have a system with low power and delay [4,5]. Therefore, to overcome these design challenges and to design a power efficient, stable and reliable SRAM cell, various architectures of SRAM cells have been proposed in recent years such as 8T [6], 9T [7], ST1 [8], ST2 [9], PPN10T [10] and ST11T [11].

From the given state-of-art SRAM cells, 8T, 9T, ST11T are single-ended (SE) while ST1, ST2, PPN10T are differential. The conventional 8T uses read decouple circuit (RD) for read mode operation. This RD circuit increases the read margin but also increases the leakage current in read path when compared with conventional 6T SRAM cell [6,12]. To decrease this leakage current 9T [7] SRAM cell has been proposed, which uses the separate read port configuration. This read configuration has three stacked transistors to decrease the amount of leakage current, but it increases the read access time. In Ref. [10], PPN10T SRAM cell is presented, which uses a modified version of the read path to reduce the leakage current of the read access path. This architecture has separate read path which increases the read stability but also has two series

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connected transistors in its write path, which degrades the write stability. For further improvement in SNM, two Schmitt trigger (ST) inverter based SRAM architectures ST1 and ST2 have been proposed. ST based inverter has a sharp transition due to the presence of the feedback path and offers high SNM [13]. ST1 [8] is a differential 10T cell with feedback transistor in its pull-down network, but there is read upset issue occurs due to the voltage division between the ST inverter and the access transistors. To overcome this issue, ST2 uses an additional control signal to get stronger feedback [9,14]. But this architecture has two access transistors connected to the same BLs, which increases the load capacitance on BLs. This higher load on BLs takes longer time to discharge the BL during the read operation, which increases the read-access time. All the above-mentioned architectures are differential in the write operation, and they have high leakage current and power hungry. Hence, to overcome these issues recently, a Schmitt trigger based single-ended ST11T SRAM cell is proposed [11]. This cell uses ST based inverter and read decouple circuitry, which effectively reduces power and leakage current, but this cell has a failure to write '1' operation. However, single-ended designs suffer from write access time. It needs to write assist circuits in minimizing write '1' access time. Hence to

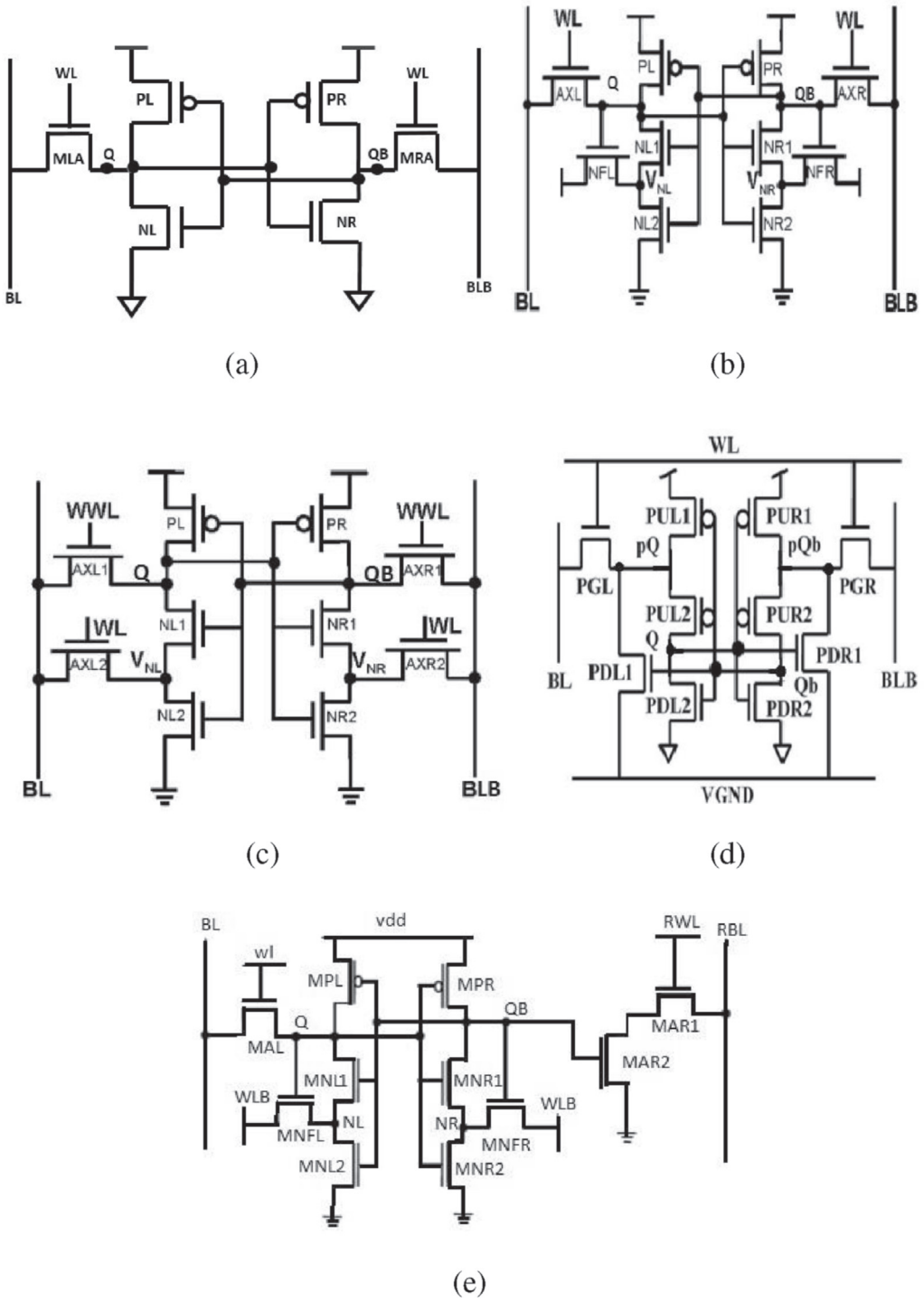


Fig. 1. Different SRAM cells (a) 6T SRAM cell (b) ST1 SRAM cell (c) ST2 SRAM cell (d) PPN10T SRAM cell (e) Single Ended ST11T SRAM cell.

improve these performance parameters up to a satisfactory value, we need to explore a robust, stable, and reliable SRAM architecture.

In this paper, we proposed a novel PPN based improved read assist energy efficient 10T SRAM cell which uses double ended for a write operation and read decouple (RD) circuit to improve the write and read stability, respectively. The proposed cell offers high RSNM, HSNM, WSNM, and lower PDP (power delay product). For the fair comparison, we have considered both single-ended and differential [8,10,14] SRAM architectures as shown in Fig. 1. Rest of this paper is organized as follows: section 2 describes the proposed SRAM cell and its working. Section 3 briefly presents the different performance parameters of SRAM design and comparative analysis, followed by a conclusion in section 4.

2. Proposed SE PPN based 10T SRAM cell design

Fig. 2 shows the proposed single ended PPN based 10T (SE PPN10T) SRAM cell. The proposed cell has double ended write, and single-ended read decoupled path. This cell is PPN based because it consists of two cross-coupled PPN inverters which have the hierarchy of PPN transistor from top to bottom. The cell uses three access transistors, one for read operation and the other two for the write operation. The controlling signal of these access transistors for different operating mode is shown in Fig. 3 which indicates that the read access transistor, i.e., NM4 is controlled by read word line (RWL) and the write access transistors, i.e., NM2 & NM3 are controlled by a word line (WL). NM4 and NM5 transistors are marked by thick lines which indicate that they are high threshold voltage (HVT) transistors to reduce the leakage current [15]. To design the proposed cell following transistor sizing has been considered i.e. PM0 & PM1 = 120n, PM2 & PM3 = 240n, NM0 & NM1 = 120n. Here to improve write static noise margin, write' access transistors NM2 & NM3 are three times more as compared to minimum size transistors. Transistors in read decouple circuit NM4 & NM5 are minimum sized, i.e., 120 nm. Fig. 4 explains direction of current flow and transistor activation for different modes of operation in the proposed SRAM cell.

2.1. Read operation

In the proposed SRAM cell, read operation is single-ended because of the read decoupled circuitry. The read operation is performed through the ultra-fast current mode sense amplifier [16]. In read mode, RBL is charged to VDD, WL is disabled, and RWL is enabled, which provides discharging path for read bit line (RBL) through NM4 & NM5 as shown in Fig. 4(a). For read '0', logic '0' is stored at node Q which turns ON the transistors PM0 & PM3 providing a voltage of around 1 V at node X. This turns ON the transistor NM5 and forms a discharging path through $RBL - NM4 - NM5$. The voltage difference, $\Delta V_{RBL} = V_{DD} - [V_{DD} - I_{READ} \times R_{NM4-NM5}]$ appears between RBL and VDD line, which is sensed by the sense amplifier. Where $R_{NM4-NM5}$ is resistance through NM4 and NM5. Fig. 4(a) shows a read '0' operation in which a discharging path takes place from RBL to ground (GND). While for read '1' operation, the logic stored at node Q is '1' which turns OFF the transistors PM0 & PM3, still providing a voltage drop of around 21.52 mV at node X. By selecting proper width size of PM0 and PM3, the voltage drop at node X can further minimize during read '1' operation. The node X voltage for read '0' an read '1' for different transistor width sizing is shown in Table 2. Results show that the node X voltage decreases during read '1' with the width of PM0 and PM3 increases whereas node X voltage increases with the width during read '0' operation. But this voltage drop at node X is not enough to turn ON the transistor NM5 because of its HVT characteristics. And hence no discharging path is formed from RBL to ground. During the read access, the disabled WL makes data storage nodes (Q and QB) isolate from BL and the value of RSNM approximately equal to the value of HSNM hence it enhanced the read stability of the proposed cell. Here we have used minimum sized transistors in read decouple circuit to reduce the leakage current with some read delay penalty.

Fig. 5 shows the 1000 Monte Carlo simulations for node X voltage during read '0' and read '1' operations. Results shows that the $\pm 3\sigma$ deviation is 45.26 nV and 7.628 mV for read '0' and read '1', respectively. It is observed that the deviation is very less for read '0' as compared to read '1' operation which indicate that the proposed cell has less effect of process variations.

2.2. Write operation

During write operation, WL is activated to transfer the data from BLs to storage node Q and QB as shown in Fig. 4(b). BLs whose value is high/low is set according to the data to be written in the memory cell. In this mode, RWL is disabled, whereas RBL is precharged to VDD. For Writing data into the cell the process is differential therefore for write '0' WBL is set to GND and WBLB is set to high with node Q and QB initialized to VDD and GND, respectively and vice-versa for write '1' operation.

2.3. Hold operation

During the hold operation, both read and write word lines are disabled that sets the access transistors to cut-off mode resulting in the isolation of cross-coupled PPN inverter from the BLs. In the proposed cell, the decouple circuit is used to mitigate the read disturbance conflict and to eliminate the requirement of large size transistors for proper read and write operation. The proposed SRAM cell design provides sev-

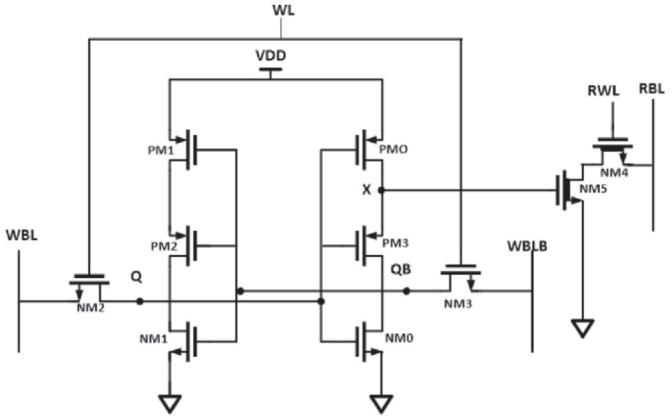


Fig. 2. Schematic of proposed SE PPN10T SRAM cell. Transistors with thick line are high threshold voltage (HVT) transistors.

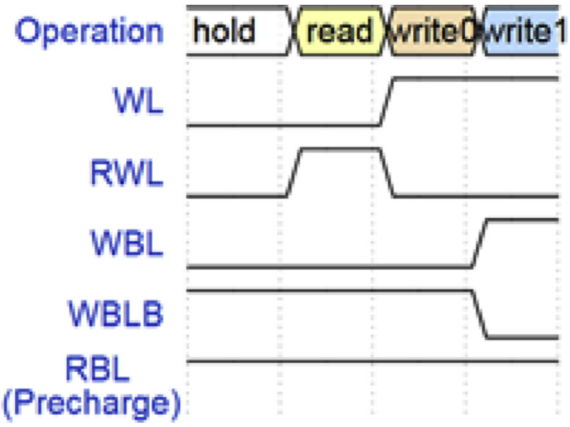


Fig. 3. Proposed SE PPN10T SRAM cell control signals.

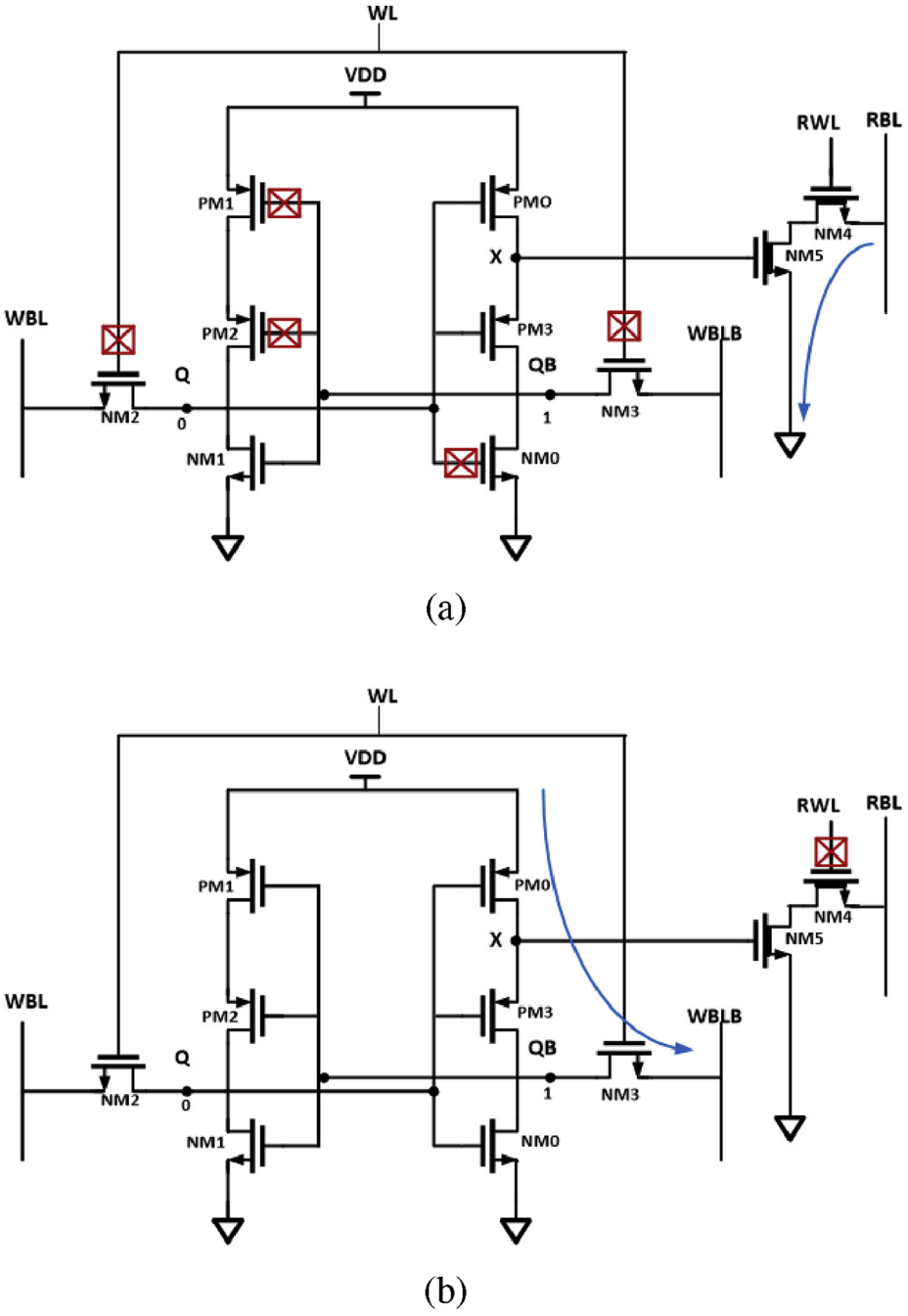


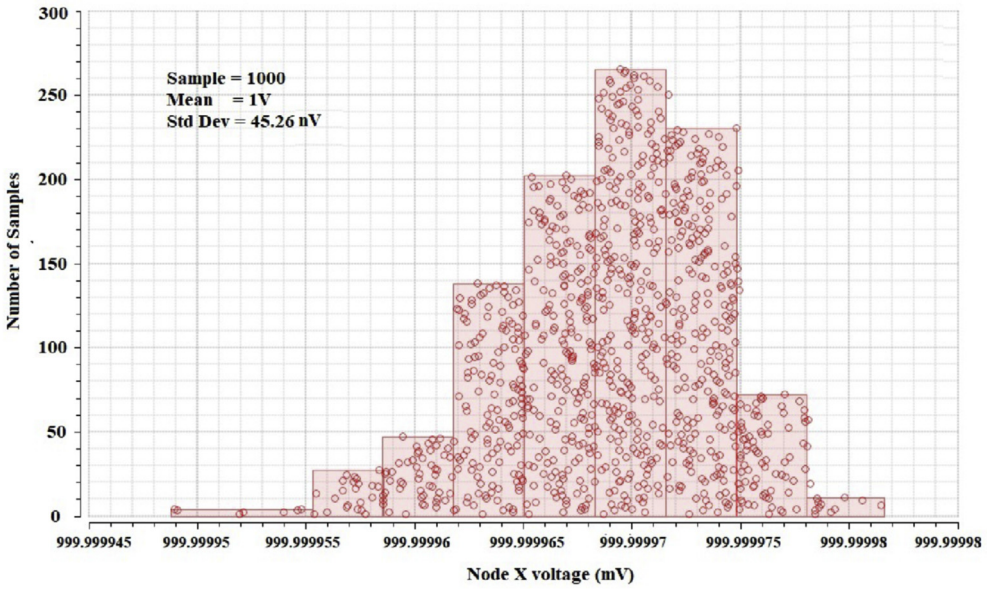
Fig. 4. Different mode of operations for proposed SRAM cell. Cross show the transistors are in cutoff condition (a) Read operation (b) Write operation.

eral advantages over the existing differential PPN based 10T SRAM cell [10]:

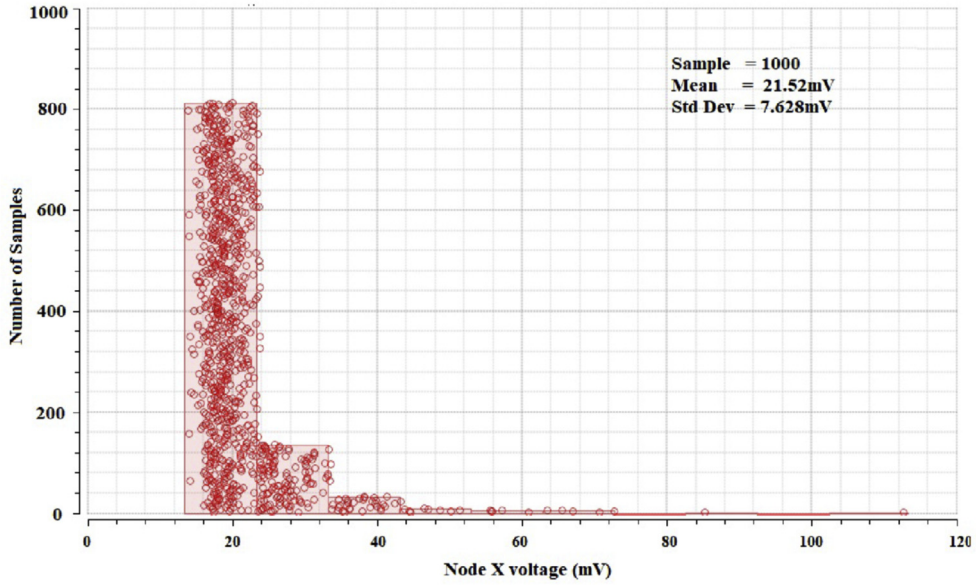
- In this work, NM4 & NM5 transistors are used for the read operation, and they are HVT (high threshold voltage) transistors, which is reducing the leakage current.
- Due to read decoupled circuit, storage nodes Q and QB get isolated. Hence RSNM is nearly equal to HSNM.
- Proposed cell eliminates the VGND control signal, which in turn has less number of control signals in an SRAM cell.
- By using differential write with two access transistors NM2 & NM3 and two BLs (WBL & WBLB), its write ability is improved and gives high WSNM value. It can be further improved by applying the existing RSCE (Reverse Short Channel effect) scheme or by enhancing the WL voltage [17].
- Its write '0' and write '1' delay is also less means writing data into memory is very fast as compared to differential PPN 10T SRAM cell. In fact, its write '0' delay is even less than the conventional 6T SRAM cell.

3. Performance parameter and comparison

In this segment, we obtain and compare several performance parameters of the proposed SRAM cell with previously presented SRAM cells. Here, all the SRAM architectures are designed and investigated using 45 nm gpdk CMOS technology in CADENCE EDA tool. Table 1 shows the feature comparison of different SRAM cells which are considered in this paper. For the purpose of detailed analysis, the performance parameters of the proposed SRAM cell is compared with



(a)



(b)

Fig. 5. Monto Carlo simulation for the voltage at the node X for (a) Read '0' (b) Read '1'.

different single ended and double ended SRAM cells like 6T [4], ST1 [8], ST2 [9,14], PPN10T cell [10] and ST11T [11]. The comparison of several performance parameters is presented in Table 2. All the performance parameters are evaluated at 1 V supply voltage and 27 °C operating temperature with typical process corner analysis.

3.1. Stability

The stability is conventionally computed as the static noise margin. The noise margin is gauged by tracing the overlapped VTC (Butterfly diagram) for the back to back connected inverters that form the memory cell. The diagonal of the largest square that can fit in the eyes of the butterfly diagram determines the noise margin.

3.1.1. Read static noise margin

Read SNM (RSNM) is the maximum DC noise voltage that an SRAM cell can tolerate without losing the data during the read operation. The RSNM is calculated using the method given in Ref. [18] at 1 V supply voltage. Here RWL is set as HIGH voltage, WL as LOW voltage and RBL is precharged. The decoupled read path through RBL-NM4-NM5-GND doesn't affect the Q and QB nodes of the SRAM cell, which would end up achieving improved RSNM.

The RSNM of all the SRAM cells have been calculated, as shown in Fig. 6(a). The RSNM of the proposed SRAM cell is 466 mV, which has 83.4%, 50.14%, 50.14%, 43.3% and 3.09% improvement as compared to 6T, ST2, ST11T, ST1, and PPN10T, respectively, at 1 V supply voltage. We also perform 1000 Monte Carlo simulation for RSNM at the supply voltage of 1 V as shown in Fig. 6(b). The result shows that the mean is at 0.382 V with a standard deviation of 0.02 V for RSNM dis-

Table 1
Features comparison of different SRAM cells.

Cell Features	6T [12]	ST1 [8]	ST2 [9]	PPN10T [10]	ST11T [11]	Proposed Cell
Reading/Writing	Diff/Diff	Diff/Diff	Diff/Diff	Diff/Diff	SE,SE	SE, Diff
Bitlines	2-BL	2-BL	2-BL	2-BL	1-BL 1- RBL	2-WBL 1- RBL
Control signal	1-WL	1-WL	1-WL 1-WWL	1-WL 1-VGND	2-WL 1-RWL 1- VGND	1-WL 1- RWL
No. of NMOS in read path	2	3	2	2	2	2

Diff-Differential, **SE**-Single Ended, **BL**-Bitline, **WL**-Wordline, **WBL**-Word Bitline, **RBL**-Read Bitline, **VGND**-Virtual Ground.

Table 2
Effect of PM0 and PM3 width variation on node X voltage during read operation.

W_{PM0}	W_{PM3}	Node X voltage	
		Read 1	Read 0
120n	120n	38.12 mV	1 V
	360n	35.23 mV	1 V
	600n	34.32 mV	1 V
240n	120n	36.88 mV	1 V
	360n	35.31 mV	1 V
	600n	34.48 mV	1 V
360n	120n	36.88 mV	1 V
	360n	35.51 mV	1 V
	600n	34.73 mV	1 V

tribution of the proposed cell. For the process variation analysis, RSNM at different process corners (FS = Fast NMOS and Slow PMOS; FF = Fast NMOS and Fast PMOS; SS = Slow NMOS and Slow PMOS; SF = Slow NMOS and Fast PMOS; TT = Typical) have been performed for proposed and 6T SRAM cells as shown in Fig. 6(c). Results show that the proposed cell has improved RSNM for all the process corners as compared to 6T SRAM cell. Results also show that the proposed cell has minimum RSNM value at worst case FS process corner, but the value of RSNM is still higher than 6T SRAM cell and hence better read stability.

3.1.2. Write static noise margin

The write static noise margin (WSNM) is defined as the minimum bit line voltage required to flip the state of the cell. During the write operation, the input data are sent to the BLs, and the word lines are activated to access the cell. There are two methods to calculate WSNM, first is the traditional butterfly SNM technique, and second is write margin technique [19]. In this paper, we have used the traditional butterfly approach to calculate WSNM of all the considered SRAM cells. Here for WSNM calculation, WL set as HIGH voltage and RWL as LOW voltage. The butterfly curve for WSNM of all the SRAM cells has been calculated, as shown in Fig. 7(a). From the simulation results, the WSNM of proposed SRAM cell has 29.5%, 18.9% and 12.8% improvement as compared to 6T, ST11T, and PPN10T SRAM cell, respectively at 1 V supply voltage. For the process variation analysis on WSNM, we have performed 1000 Monte Carlo Simulations, as shown in Fig. 7(b). From results, we observe that the proposed cell has a mean WSNM of 0.47 V with a deviation of 0.03 V at 1 V supply voltage.

3.1.3. Hold static noise margin

Hold static noise margin (HSNM) is the maximum DC voltage that SRAM cell can tolerate without losing data during the idle state. Hold noise margin is calculated when WL and RWL both pulled down to the ground (0 V). From Fig. 7(c) it is observed that the ST2 cell has the highest value of HSNM because of improved characteristics of ST based inverter. Our proposed cell achieves HSNM nearly equal to the ST2 SRAM cell. HSNM in the proposed cell is improved by 37.4%, and 3.09% compared to ST1 (ST1 and ST11T have similar values) and 6T (6T and PPN have similar values) respectively.

3.2. Access time or delay

It is defined as the average of the low-to-high (t_{PLH}) and the high-to-low (t_{PHL}) delay. These are two types of read and write access time.

3.2.1. Read delay

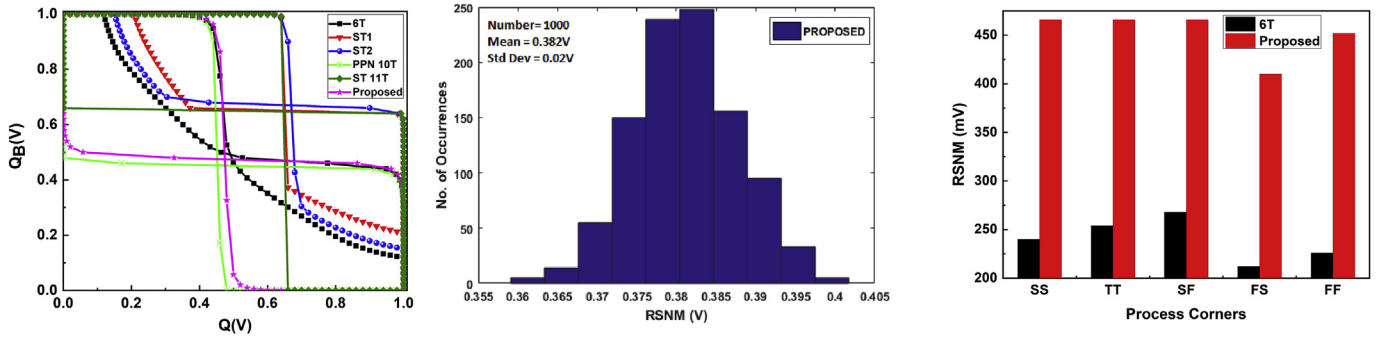
Various methods have been proposed by the researchers to calculate read access time for differential read and single-ended read as suggested in Refs. [8,20], respectively. As our proposed cell and ST11T are single-ended while others are differential, so we have used a method suggested in Ref. [21]. As stated in this method, the delay is measured as the time when the RBL discharges to [VDD - 50 mV] at that time; WL is set as high. Fig. 8(a) shows the read delay of the proposed cell with other existing SRAM cells. From results, it is observed that the 6T and ST1 cells have a smaller value of read access time. Results indicate the faster read operation, which is referred to the differential operation in read mode and small values on BLs capacitance of these cells. ST1 and 6T have approximately the same read delay. ST11T has a higher delay as compared with 6T and ST1 due to its single-ended read mechanism and larger value on BL capacitance. The read delay of the proposed cell is high because HVT transistors have been used to reduce the leakage current, but read delay is nearly the same as PPN10T.

3.2.2. Write delay

The write access time or write delay (t_{write}) for write '1' is considered as the period when the WL is initialized, and the node Q (initially at logic 0) attains 90% of the supply voltage value. Similarly, for write '0', it is the time when the node Q (initially at logic 1) reaches 10% of its initial value [22]. Fig. 8 (b and c) shows the simulation result of write delay at various supply voltages of different SRAM cells. Results show that the proposed cell has the lowest write '0' delay as compared with other considered SRAM cells. The reduced delay for the proposed cell architecture is due to the sizing of the access transistor is kept high. Moreover, PPN10T have highest write delay compare to other cells, because it includes voltage division between stacked pull-up transistors and the access transistor. Further, we have calculated write '1' delay for all the SRAM cell architecture and observe that the write '1' delay for 6T and ST2 have same values because they have identical pull-up network while write '1' delay of the proposed cell is same as ST1 and lower than PPN10T. For ST11T, Write '1' delay of ST11T is not calculated due to its single-ended structure.

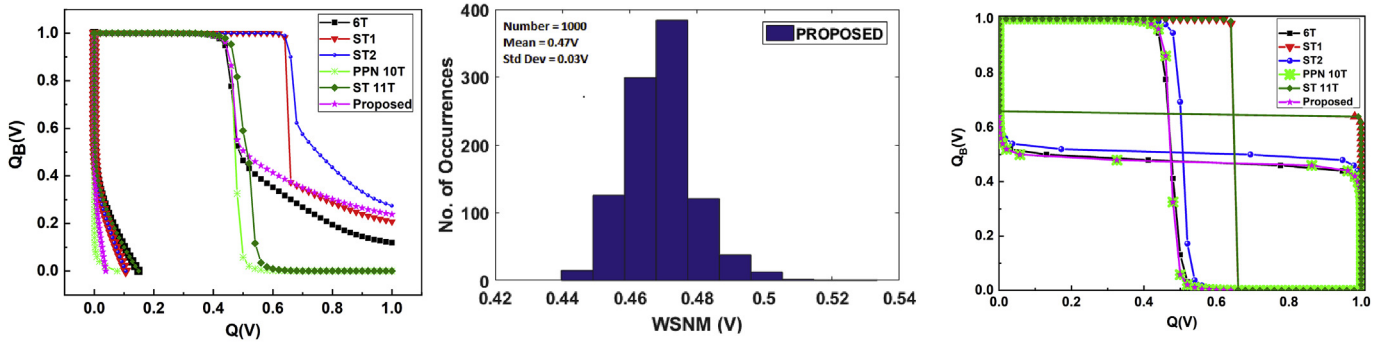
3.3. Read/write power consumption

The write/read dynamic power is measured as the product of voltage source and current drawn from it during the write/read access time. Fig. 9(a)–(c) shows the read, write '0', and write '1' dynamic power of considered SRAM cells at various supply voltages. From results, it is observed that the PPN10T consumes maximum power while 6T and ST2 have minimum and equal power during the read operation. The SRAM cell has a trade-off between delay and power consumption. Therefore, the proposed cell has high write '0' power and lower write '0' delay whereas, it has low write '1' power and higher write '1' delay. The results in Fig. 9(b) show that the proposed cell has a minimum write '1' power among all the considered SRAM cell at 1 V supply voltage.



(a) (b) (c)

Fig. 6. a) Read SNM of different SRAM cells @ 1 V supply voltage (b) Histogram for RSNM of proposed cell at 1 V supply voltage with 1000 Monte Carlo simulation (c) RSNM at various process corners for 6T SRAM and proposed SRAM cell.



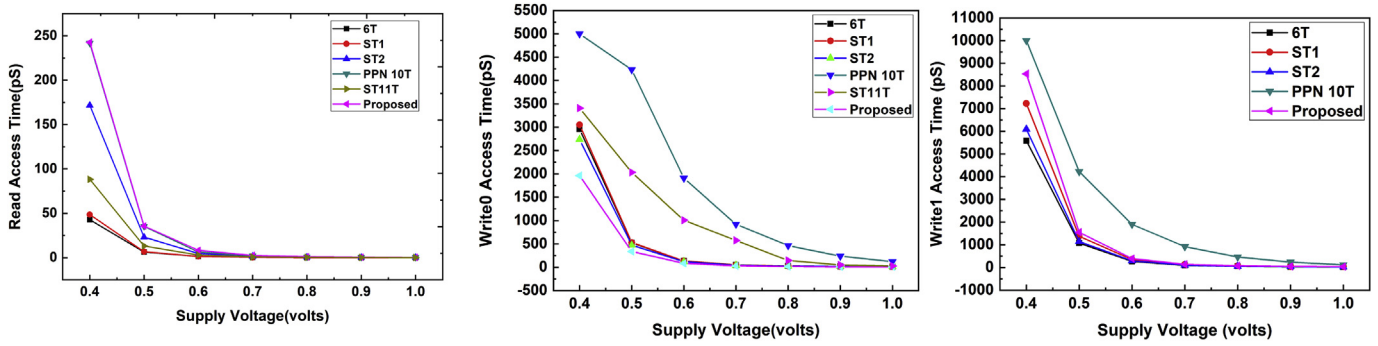
(a) (b) (c)

Fig. 7. a) Write SNM of different SRAM cells @ 1 V supply voltage (b) Histogram for WSNM of proposed cell at 1 V supply voltage with 1000 Monte Carlo simulation (c) Hold SNM of different SRAM cells @ 1 V supply voltage.

3.4. Leakage current

Leakage current is measured as the current drawn from VDD to GND when the SRAM cell is in static or hold condition. Fig. 10(a) shows the operating region of different transistors of proposed cell in the standby mode. The marked transistors are in cut-off mode. As we know that, due to HVT transistors in the read decoupled network, the proposed cell draw less leakage current. Fig. 10(b) shows the leakage current variations at different supply voltages for various existing and proposed SRAM cells. The proposed cell consumes 29% and 32% less leakage current as compared with PPN10T and ST1 cells at nominal supply voltage (1 V).

Further, we also observed that the proposed cell consumes 44% and 55% less leakage current as compared to PPN10T and ST1 at the supply voltage of 0.4 V. Also, the proposed cell consumes the same leakage current as 6T SRAM at 0.4 V of the supply voltage. For the evaluation of temperature stability of the proposed and 6T SRAM cell, we have also performed the simulation for the temperatures range of 25 °C–125 °C. As shown in Fig. 10(c), the proposed cell has less leakage current as compared to 6T SRAM cell at a higher temperature.



(a) (b) (c)

Fig. 8. Access time of different SRAM Cell (a) Read access time (b) Write 0 access time (c) Write 1 access time.

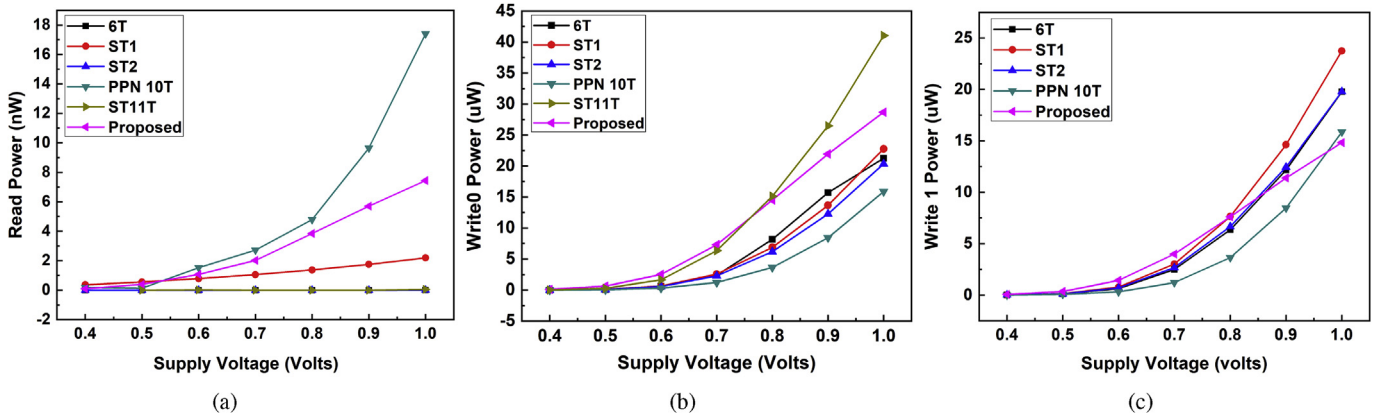


Fig. 9. Dynamic power dissipation of different SRAM cells (a) Write '0' power (b) Write '1' power (c) Read power.

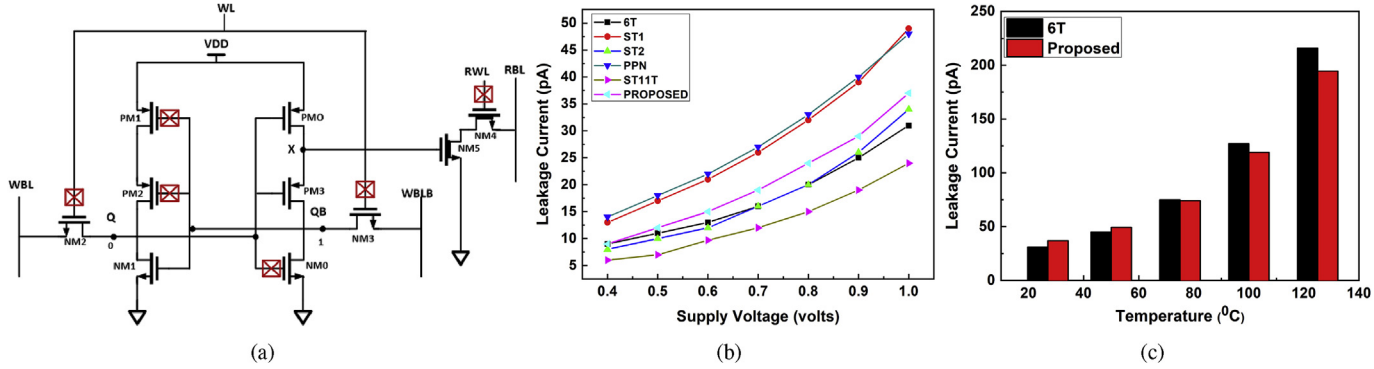


Fig. 10. Leakage current of proposed 10T SRAM Cell (a) Schematic of proposed SRAM cell in Hold mode. Cross represent the transistors with cutoff condition (b) Leakage current of different SRAM cells with supply variation (c) variation in leakage current of proposed and 6T SRAM cells with temperature.

3.5. Power delay product

The power delay product (energy consumption) of the SRAM cell is defined as the product of delay time and power dissipated during write or read operation. During charging and discharging of bit lines so much of SRAM energy is consumed. Here, to calculate energy consumption, we have considered the power dissipation and access time during write '0' operation. For the calculation of energy consumption, we have considered 2 *f*F capacitors at the bitlines [23]. Energy consumption during a write operation is more than the read operation because there is a full swing voltage of bit line. Hence it is required to reduce energy consumption during the write operation. Table 3 shows the energy consumption of various SRAM cells during write '0' operation. From results, it is observed that the energy consumption of the proposed cell is minimum compared to other considered SRAM cell. Here delay of the circuits is playing a major role while calculating the power delay product of the considered cells. The proposed cell has the lowest delay which significantly reduces the energy consumptions.

3.6. Area comparison

Fig. 11 shows the layout view of 6T and the proposed cells using 45 nm technology design rules. The cell areas are normalized to that of 6T SRAM cell. The proposed cell and PPN10T SRAM cell shows the area overhead of 1.77× and 1.47× as compared to 6T SRAM cell. Our proposed cell requires less area as compared to ST1 and ST2 even though these both the cells have the same number of transistors. The area requirement is higher due to increased transistor sizing to get comparable performance.

3.7. Figure of merit

To characterize and compare various SRAM cell architecture according to defined performance parameters are difficult. Because the required parameters values such as SNM, delay, power, and area are application dependent and all performance parameters have a trade-off between them. Thus, we introduce a figure of merit (FOM) to evaluate

Table 3
Comparison of various performance parameters of different SRAM cells @ 1 V supply voltage.

Performance Parameters	6T [12]	ST1 [8]	ST2 [9]	PPN10T [10]	ST11T [11]	Proposed Cell
RSNM (mV)	254	325	339	452	339	466
WSNM (mV)	480	763	791	551	523	622
HSNM (mV)	452	471	480	452	339	466
Write '0' Delay	13.76 ps	13.18 ps	11.8 ps	12.08 ns	27.2 ps	7.91 ps
Write '0' Power (μW)	21.25	22.78	20.3	15.87	41.04	28
Leakage Current (pA)	31	49	34	48	24	37
Write PDP	292 aJ	300 aJ	241 aJ	19.17 fJ	1.116 fJ	225 aJ
Area (Normalized to 6T)	1	1.89	1.89	1.47	1.31	1.84
Figure of Merit	1	0.494	1.374	0.0014	0.279	1.454

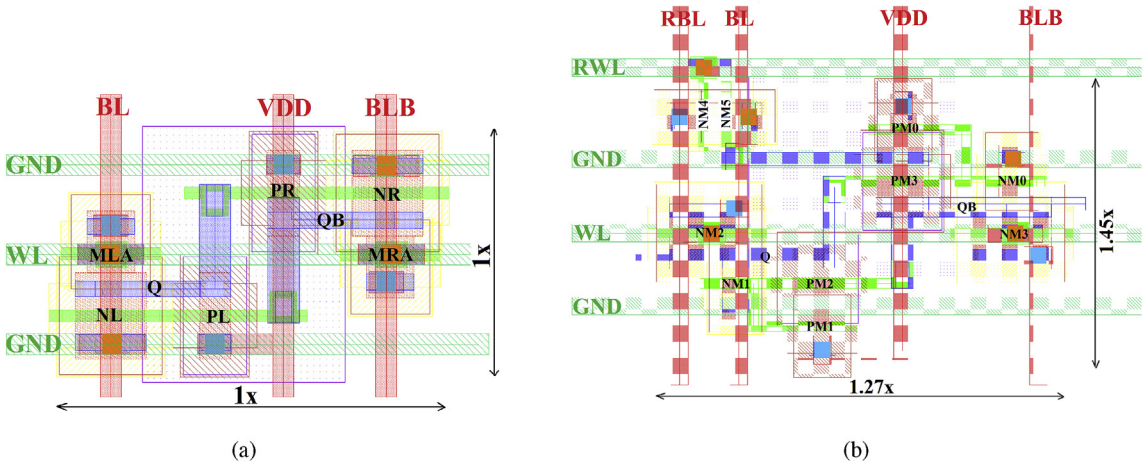


Fig. 11. Layout area (a) 6T SRAM cell (b) Proposed cell.

all the considered SRAM cell on common criteria [24].

$$FOM = \frac{RS\,NM_N \times WS\,NM_N \times HS\,NM_N}{PDP_N \times Leakage_N \times Area_N} \quad (1)$$

where $RSNM_N$, $WSNM_N$, $HSNM_N$, PDP_N, $Leakage_N$, and $Area_N$ are the normalized values for RSNM, WSNM, HSNM, PDP, Leakage current, and area with respect to 6T SRAM cell. From Table 3, we found that the proposed cell show the better FOM as compared to the other considered SRAM cell architecture designed for energy efficient memory design.

4. Conclusion

This paper present an improved read assist energy efficient single ended PPN based 10T SRAM cell. The proposed cell has improved noise margin and having least PDP (energy consumption) during the write operation. The proposed cell also have better RSNM compared to other structures. Because of the higher noise margin, the proposed SRAM cell provides better stability. Due to the stacking effect in the pull-up networks, the proposed cell offer low leakage power dissipation. For a better perspective, we introduce a FOM considering all the performance parameters. The FOM of the proposed cell is 1.513× higher as compared to 6T SRAM cell and also high as compared to all other cells. Because of higher FOM, the proposed SRAM cell is most suited for high performance, energy efficient wireless sensor nodes where the energy and performance is a major concern.

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Appendix A. Supplementary data

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