NH_3 and NO + NH_3 Annealing of 4H-SiC Trench MOSFETs: Device Performance and Reliability

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***Abstract*— As the gate oxide (GOX)-SiC interface of SiC MOSFETs is crucial for device performance, it requires special attention. To improve interface quality, device performance, and reliability, commonly, a postoxidation anneal (POA) is applied. Different gas compositions can be used to passivate the SiC interface and bulk oxide. We study the effects of ammonia (NH_3) and a new combined NO + NH_3 POA on 4H-SiC trench MOSFET test structures and compare them to the common nitric oxide (NO) POA. Our studies are not only limited to device performance represented by channel mobility but also contain reliability studies in the form of bias temperature instability (BTI), sweep hysteresis, Fowler–Nordheim (FN) tunneling and GOX breakdown. We find that both, NH_3 and NO + NH_3 result in higher mobility than NO annealed test structures. On the other hand, ammonia containing POAs deteriorate device reliability, e.g., leading to larger BTI and higher tunneling currents. As both can be detrimental in certain applications, they must be optimized. We show that NO + NH_3 anneals may offer an acceptable compromise between the characteristics of NO and NH_3 with regard to tunneling and device performance. However, it shows more positive BTI (PBTI) drift than NH_3 and NO. We will show that a full characterization of the GOX is essential to evaluate, optimize, and benchmark new annealing strategies.**

***Index Terms*— 4H-silicon carbide (SiC), ammonia (NH_3), bias temperature instability (BTI), hysteresis, mobility, MOSFET, nitric oxide (NO), NO + NH_3, postoxidation anneal (POA).**

I. Introduction

SILICON carbide (SiC) as a wide bandgap semiconductor is a promising material in the field of high-power electronics because of its outstanding material properties, such as high electron mobility, high thermal conductivity and high breakdown field [1]. Just as silicon (Si), SiC can form silicon dioxide (SiO_2) as a native oxide, which can be considered as one of the most important features of SiC compared to other promising wide bandgap materials. Additionally, it enables well controllable n- and p-doping so that it is well suitable for MOSFETs [1], [2]. However, currently achieved field-effect mobilities with up to 60 $cm^2/(Vs)$ in SiC MOSFETs are still far lower than the theoretically possible bulk mobility [2], [3], e.g., due to trapping at or near the SiC/SiO_2 interface [3]. In order to reduce the density of interface traps (D_{it}), a postoxidation anneal (POA) can be applied. Currently, nitric oxide (NO) is the preferred annealing gas because it leads to increased MOSFET performance and reliability [4]–[6]. However, recent studies suggest that a POA in ammonia (NH_3) ambient can lead to even higher mobilities [7]. Most research groups only focus on the channel mobility or the density of interface states (D_{it}) when studying different POAs, e.g., [8]–[11]. However, as will be discussed in detail in this article, not only the mobility and interface state density are important for SiC MOSFETs but also device reliability, i.e., hysteresis effects and bias temperature instability (BTI) [12]. Therefore, we compare the effect of different annealing ambients with regard to mobility, hysteresis effects, BTI, and gate oxide (GOX) tunneling/breakdown of 4H-SiC MOSFET test structures. We study the commonly known annealing gases, NO and NH_3, as well as, a new combined process with an initial NO and a subsequent NH_3 anneal (referred to as NO + NH_3). We will show that when choosing an annealing gas for postoxidation annealing, one might have to deal with certain trade-offs between performance (e.g., enhanced channel mobility) and reliability (e.g., good V_{th} stability). We focus on the recent trend for new SiC power MOSFETs toward trench technologies, as they allow for higher channel packing densities, leading to lower static losses and smaller ON-resistances [12].

II. Experimental

Trench nMOSFET test structures were fabricated on commercial Si-face 4H-SiC substrates with 4° off-axis with an industrial process. The p-doping was formed by aluminum (Al) implantation. The SiO_2 GOX was deposited by chemical vapor deposition. The conductive channel forms along the a-face ($(11\bar{2}0)$ crystal plane) on one side of the trench. A schematic

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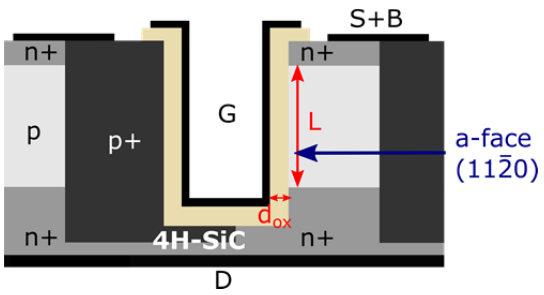

Fig. 1. Schematic cross section of the studied 4H-SiC trench MOSFETs. The channel forms along the a-face.

cross section of the test structures is shown in Fig. 1. In order to improve the interface quality, all MOSFETs received different POAs in either NO (time t_1 >100 min, temperature T_1 >1000 °C), NH_3 (t_1, $T_2 \approx T_1$) or a combined POA consisting of NO POA (t_1, T_1) followed by NH_3 POA ($t_2 < t_1$, $T_3 < 1000$ °C) (NO + NH_3).

The GOX and SiC/SiO_2 interface were characterized by current–voltage (I–V) and BTI measurements. For all measurements, we used an Agilent B1500 parameter analyzer with source measure units (SMUs) and a switching matrix. The apparent channel mobility was extracted from the transfer characteristics measured with 0.1 V steps and an integration time of 60 ms according to the method of Ghibaudo [14] at a drain voltage of $V_D = 0.01$ V. Furthermore, we extracted the threshold voltage (V_{th}) at $I_D = 1$ mA.

In SiC-based MOSFETs, a significant hysteresis between up- and down-sweep of I–V curves may exist when the device's gate terminal is charged in accumulation prior to a sweep started at negative gate voltages [15], [16]. We studied the subthreshold hysteresis of the different test structures to quantify this feature. First, the devices were preconditioned at −20 V for 5 s to make sure they all were in a comparable state. Then, a dual-gate-voltage sweep from −5 to +25 V and back to −5 V (V_D = 0.01 V) was performed during which the drain current I_D was measured. The difference in V_G required to reach the same I_D during the up and down sweeps is referred to as subthreshold hysteresis (extracted at $I_D = 1$ nA). Furthermore, the breakdown voltage of the GOX was extracted for all devices.

Room temperature preconditioned positive BTI (PBTI) tests were conducted as described in [17]. The readout values of JEDEC-like BTI patterns depend on the readout timing and the gate bias history. For receiving reliable results, it was suggested [17] to introduce a preconditioning pattern consisting of an accumulation and inversion pulse before each readout cycle. This ensures comparable interface conditions during each readout and minimizes the impact of readout timing. In our experiments, the devices were stressed at +25 V, which is significantly higher than needed for standard operation. The preconditioning voltages used are −15 and +15 V. We use two preconditioning pulses because this leads to a more stable readout value. The readout after each stress sequence was conducted in gated-diode (GD) configuration, i.e., the source (S) contact is grounded, and gate (G) and drain (D) terminals were shortened. A current I_D = 1 mA was forced and the resulting voltage V_G measured. Note that for low current

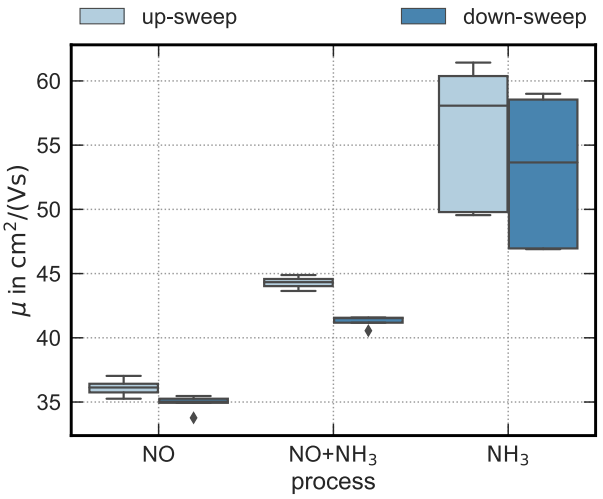

Fig. 2. Ghibaudo mobility of trench MOSFETs which were annealed in different ambients after oxidation. Due to the sweep hysteresis, the extracted values for both the up- (light blue, left box) and down-sweep (darker blue, right box) of the transfer characteristics are depicted.

TABLE I
SUMMARIZING COMPARISON OF GOX/INTERFACE CHARACTERIZATION FOR NO, NH_3, AND NO + NH_3 ANNEALED TRENCH MOSFETs

Characterization Method	NO	NO+NH_3	NH_3
Ghibaudo mobility [cm^2/(Vs)]	35	40-45	50-60
Hysteresis @ 1 nA [V]	3.2	2.8	2
PBTI @ 1444 s [mV]	30	100	60-70
GOX tunneling [MV/cm]	5	5*	3*
V_{th} @ 1 mA (down sweep) [V]	5.25-5.3	5.3-5.35	5.1-5.2

*additional trapping above 8 MV/cm

levels the drift extracted with this measurement configuration is equivalent to drift calculated from V_{th}-readout with fixed V_G and V_D (not shown).

III. RESULTS AND DISCUSSION

Fig. 2 shows the apparent mobility for all tested POA variations extracted from the characteristic curves as described in Section II. In accordance with the literature [7], we observe a mobility increase by the NH_3 treatment compared to the standard NO POA. The latter results in a mobility around 35 cm^2/(Vs) whereas NO + NH_3 results in μ = 40–45 cm^2/(Vs) and NH_3 in approximately 50–60 cm^2/(Vs). For the NH_3 annealed samples, a wider distribution in mobility is observed. The exact reason for this is unknown; however, in general, a larger spread is observed for this process. It is not clear if instable passivations with hydrogen might also play a role. In total, POAs containing NH_3 lead to SiC MOSFETs with increased mobility values compared to a POA in NO only, presumably because of the additional hydrogen content of the annealing gases. At the same time, the threshold voltage of all studied processes is nearly the same (see Table I).

From a mobility point of view, a POA in either NH_3 or NO+NH_3 seems to be very promising for commercial

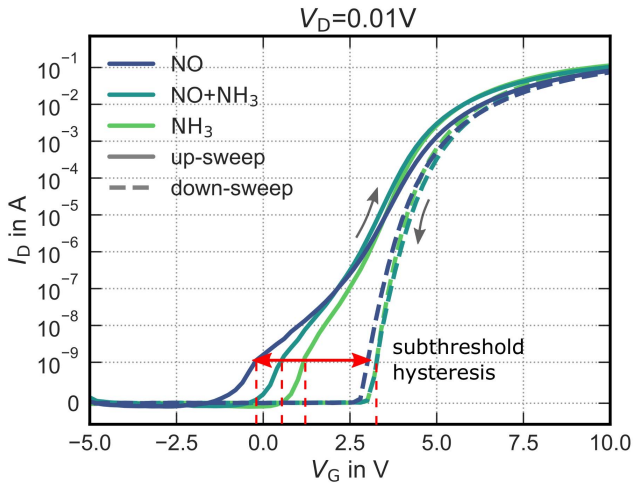

Fig. 3. Subthreshold hysteresis in SiC trench MOSFETs with different POAs. The transfer characteristics were measured by first sweeping the gate voltage from accumulation to inversion (up-sweep), directly followed by a sweep from inversion to accumulation (down-sweep). The subthreshold hysteresis is extracted at a current level of 1 nA (see red arrow) as the difference of V_{th} (red dashed lines) between up- and down-sweep.

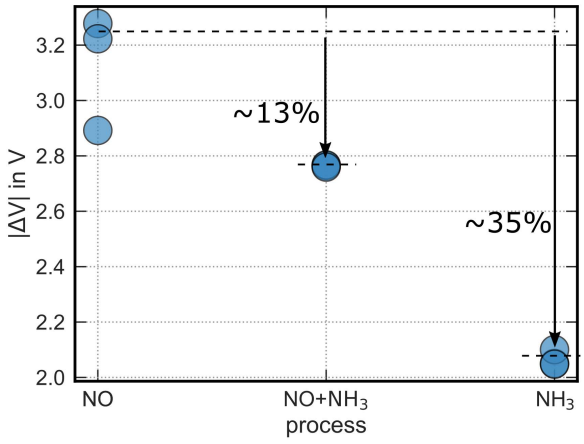

Fig. 4. Subthreshold voltage shift of differently annealed SiC trench MOSFETs extracted at a current level of 1 nA according to Fig. 3.

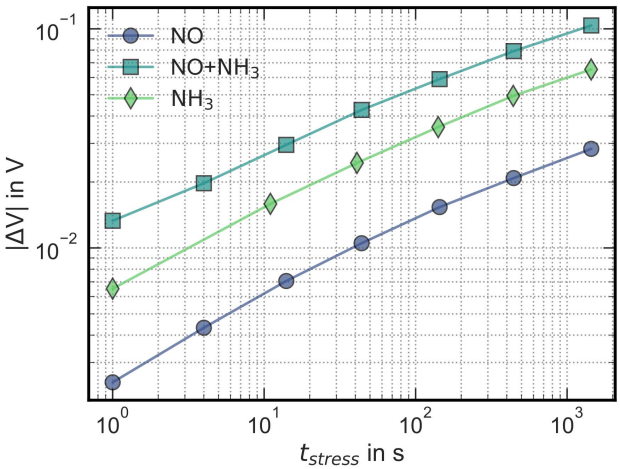

Fig. 5. PBTI of differently annealed trench MOSFETs. Devices were stressed at room temperature at a stress voltage of +25 V. The readout was performed in gated diode configuration at 1 mA after a preconditioning pulse.

high-performance SiC MOSFETs. However, as we will show, focusing on mobility improvements alone is not sufficient to assess device quality after applying a new POA process. This is especially the case from a device reliability perspective as different annealing atmospheres may not only chemically modify the interface but also the GOX. Regoutz *et al.* [18] have shown that during NO POA, nitrogen is only incorporated at the SiC/SiO_2 interface, whereas it is incorporated throughout the entire SiO_2 bulk for a POA containing NH_3. Furthermore, the hydrogen density within the GOX is also expected to be different. Since hydrogen has been linked to a number of reliability issues in Si technologies [19]–[22], we have conducted detailed GOX characterization with a focus on MOSFET reliability to evaluate the impact of the chemical differences in the SiC/SiO_2 system.

A. Sweep Hysteresis

We start by analyzing the impact of the various POA variations on the sweep hysteresis, which is a common phenomenon in SiC MOSFETs caused by hole capture and emission [15], [16]. While in applications this effect turns the MOSFETs earlier on and off and is, therefore, not considered crucial for normal device operation [16], it is of high interest in studies focused on a fundamental understanding of the SiC/SiO_2 interface. Fig. 3 depicts the transfer characteristics of the studied MOSFETs showing the sweep hysteresis. Because of preconditioning prior to the up-sweep, holes are trapped at the interface. During the up-sweep, the captured holes are slowly emitted and neutralized by recombination with electrons leading to the observed hysteresis effect [15]. Fig. 4 shows the maximum voltage shift due to the hysteresis in the subthreshold regime at a drain current of 1 nA. NO annealed MOSFETs show the largest hysteresis. With increasing NH_3 content during POA, a reduction in subthreshold hysteresis is observed. Therefore, we assume the additional nitrogen and/or hydrogen incorporation to reduce hole trapping at the interface. In total, we conclude that, compared to NO, a POA in NH_3 leads to more efficient passivation of hole traps which cause the sweep hysteresis. The combination of both POAs (NO + NH_3) lies in between the two single processes.

B. Bias Temperature Instability

The PBTI drift over time is shown in Fig. 5. In accordance with [23], we observe only small drifts, and therefore, relatively stable threshold voltages for the three different nitrided interfaces. The lowest PBTI drift with approximately 30 mV after 1444 s of stress is observed for NO annealed MOSFETs. In NH_3 and NO + NH_3 annealed devices the drift is twice and thrice as large, respectively. In contrast, these samples show less subthreshold hysteresis than the NO samples. Since the preconditioning sequence minimizes the hysteresis components, i.e., the influence of fast recoverable shifts, it indicates a different ratio of fast and slow recovering traps in NO, NH_3 and NO + NH_3 annealed samples. NO leads to less long-term degradation than the two presented NH_3 containing

POAs. NH_3 containing POA seems to either reduce defects responsible for PBTI drift less efficiently than NO POA, or to create new defects because of nitrogen incorporation in the bulk oxide, or to passivate more defects which, however, become depassivated during stress. In the combined process, we expect that NH_3 POA after NO POA leads to an interaction of NH_3 with the already NO-passivated interface. We suggest that either new defects are created during the second annealing step or the resulting combined passivation with NO and NH_3 is less stable under PBTI than the single annealing processes by themselves. In total, we conclude that even though NH_3 POA is beneficial for the apparent channel mobility, it leads to a higher drift under positive gate bias.

In applications, BTI drift can be critical, and therefore, needs to be minimized. V_{th} drift comes along with an increased ON-resistance, and therefore, increased static losses. This may result in a decrease in efficiency, current crowding, and reduced reliability of the transistor [16], [24], [25]. Therefore, NH_3 and NO + NH_3 POA may have a negative effect on the reliability of SiC MOSFETs with applications in power electronics although they provide better channel mobilities. This makes the NO sample more appealing from a reliability point of view.

C. GOX Breakdown and Tunneling

A gate voltage sweep to determine the breakdown voltage of the devices was performed, see Fig. 6, where the curves end at the breakdown of the oxide. As a reference, we added an N_2 annealed sample from a different lot (measurement stopped before breakdown). This sample was barely affected by the applied POA, and its behavior is, therefore, similar to not annealed MOSFETs. All GOX break around 10 MV/cm or higher. The differences in GOX breakdown fields are within the normal GOX thickness variations across a wafer. The breakdown fields observed in our NH_3 annealed MOSFETs are slightly lower than those reported in [26] for MOS capacitors with thermal oxides, however, in good agreement with the theoretical breakdown field of SiO_2. In contrast to [26], for NH_3 and NO + NH_3, the slope of the gate current decreases for electric fields exceeding 8 MV/cm. Simultaneously, a gate current sweep hysteresis (voltage up-sweep is stopped before the breakdown and the voltage swept back down to 0 V) is observed for NO + NH_3 and NH_3 when exceeding 8 MV/cm. Below 8 MV/cm, no significant hysteresis is observed in the region of Fowler–Nordheim (FN) tunneling currents (not shown here). Therefore, we conclude that the ledge in the gate current is related to electron trapping in the GOX. In NO samples, only small hysteresis is observed. This might be related to the fact that for NO annealed oxides, the nitrogen is only incorporated at the SiC/SiO_2 interface whereas it is incorporated throughout the bulk oxide in the case for NO + NH_3 and NH_3 (see [18] for X-ray Photoelectron Spectroscopy (XPS) results). Thus, we assume that the presence of nitrogen in the GOX might lead to electron trapping, which, in turn, causes the decreased gate current before breakdown. However, we cannot exclude hydrogen as a possible cause.

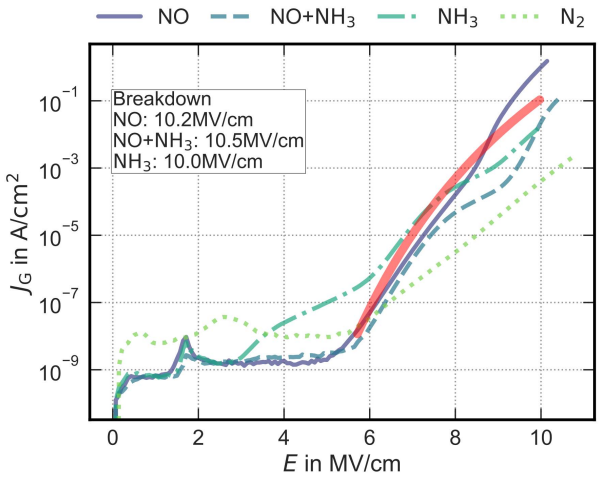

Fig. 6. GOX breakdown characteristics of differently annealed 4H-SiC Trench MOSFETs. The last point of each curve corresponds to the final breakdown voltage (see inlet), excluding the N_2 sample. Red line: calculated ideal FN tunneling current for our device parameters.

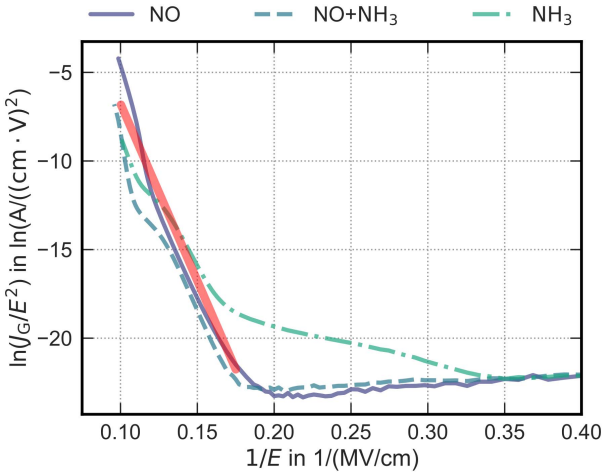

Fig. 7. FN plot of the studied trench devices. Red line: calculated ideal FN tunneling characteristic for our device parameters. NO and NO + NH_3 annealed devices follow FN characteristics whereas NH_3 does not fit to FN tunneling for moderate electric fields.

Additionally, different tunneling characteristics were found for the tested POAs. Fig. 6 clearly shows that tunneling starts around 3 MV/cm for the NH_3 sample, whereas it starts around 5–5.5 MV/cm for NO and NO + NH_3, respectively. Therefore, NH_3 POA results in a much leakier GOX at low electric fields compared to the standard NO process. This observation is not described in [26], where only $E > 5$ MV/cm is presented. Fig. 7 shows the FN plots of the tested devices. Generally speaking, tunneling of the tested devices in most parts of the I–V characteristics is in good agreement with the theoretical FN curve. NO annealed samples show the typical exponential increase of FN tunneling current known from [27], resulting in a straight line in the FN plot. NO + NH_3 also results in the typical straight line in the FN plot, as long as the electric fields stay below 8 MV/cm where trapping starts. For NH_3, a straight line can be fit to data in the FN plot for high electric fields ($1/E < 0.15(\mathrm{MV/cm})^{-1}$), suggesting FN tunneling to occur. For low or moderate fields, however, the current signal does

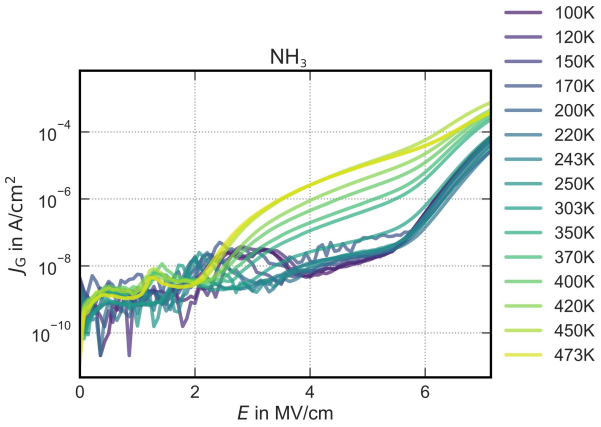

Fig. 8. J_G versus V_G characteristics at various temperatures.

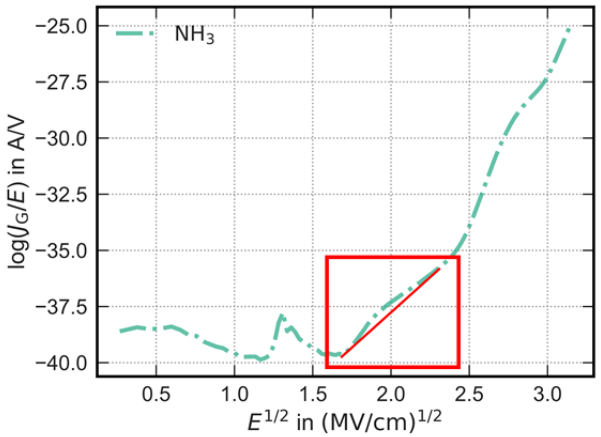

Fig. 9. PF plot of NH_3 annealed sample. The low-field tunneling cannot be fit to a straight line.

not follow the FN characteristics. The higher the temperature, the stronger the low-field tunneling current becomes (Fig. 8). This clearly suggests that a different tunneling mechanism dominates at low fields. Pool–Frenkel-effect (PFE) [28] and trap assisted tunneling [29] would offer a distinct temperature dependence as observed here. We could exclude PFE because the measurement data for low-field tunneling do not result in a straight line in the PF-plot (Fig. 9). Therefore, trap assisted tunneling currently seems the more likely cause for the observed tunneling behavior.

IV. Conclusion

4H-SiC MOSFET test structures with NO, NO + NH_3, and NH_3 POA were characterized and compared in order to evaluate their suitability for reliable and high-performant SiC MOSFETs. It was found that both, NH_3 and NO + NH_3 lead to a channel mobility improvement with respect to the NO reference [35 $cm^2/(Vs)$]. NH_3 POA almost doubled the mobility [50–60 $cm^2/(Vs)$] compared to the reference anneal in a NO containing atmosphere. At the same time, subthreshold hysteresis is reduced when introducing an NH_3-containing annealing ambient.

On the other hand, we observed increased PBTI drifts in NH_3, and NO + NH_3 annealed samples compared to the standard NO test structures.

For the NH_3 sample, we also observed a decreased tunneling threshold. Trap assisted tunneling and FN tunneling were observed in different bias regions. Both, NO + NH_3 and NH_3 show a distorted tunneling characteristic due to trapping. An overview of the results described above can be found in Table I.

In conclusion, we show that the typically employed simple analysis of the channel mobility or density of trap states in MOSFET test structures is not sufficient for a complete and reliable evaluation of the applicability of a new process. As our results show, some annealing gases, such as NH_3 and NO+NH_3 may lead to improved channel mobility at the expense of reduced reliability; for example, increased BTI and increased tunneling through the GOX. Especially the BTI drift can be detrimental in high power applications with several SiC MOSFETs in parallel. Oxide tunneling at low fields may reduce the intrinsic GOX lifetime.

The discussed POA variants reveal an obvious tradeoff between channel mobility and device reliability. From a device manufacturer point of view, excellent reliability is indispensable to achieve extremely low failure rates in the ppm range and to guarantee stable device characteristics over the entire product lifetime. Therefore, no compromises can be made with respect to reliability. High channel mobility, and therefore, better area efficiency, on the other hand, is the main driver for costs. For this reason, it is, of course, desirable to improve the channel mobility of next-generation SiC MOSFETs. This, however, must not be at the expense of reduced reliability. Therefore, we conclude that NH_3 containing POAs offer an interesting option for future device performance improvements; however, only if the reduction of reliability can be resolved.

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