On the Impact of the Gate Work-Function Metal on the Charge Trapping Component of NBTI and PBTI

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***Abstract*—We investigate bias temperature instability (BTI) charge trapping trends in high-*k* metal gate (HKMG) stacks with a variety of work function metals (WFMs). Most BTI models suggest charge trapping in oxide defects is modulated by the applied oxide electric field, which controls the energy barrier for the capture process, irrespective of the gate work function. However, experimental data on capacitors show enhanced or reduced charge trapping at a constant oxide electric field for different WFM stacks. We ascribe this to a different chemical interaction of the metals with the dielectric, which yields different defect profiles depending on the process thermal budget, and not to the gate work function *per se*. This observation is confirmed by comparing BTI degradation in nMOS and pMOS replacement gate planar transistors with three selected WFM stacks (representative of high-, standard-, and low-V_{th} device flavors), and two different process thermal budgets. Furthermore, by employing the imec/T.U. Wien physics-based BTI simulation framework "Comphy," we also show that, on top of the unavoidable chemical interaction of different metals with the underlying SiO_2/HfO_2 dielectric stack, different gate work functions within a typical range of relevance (4.35–4.75 eV) can yield a different charge state of the deep high-*k* defects, and can therefore have an impact on charge trapping kinetics during BTI stress, particularly in nMOSFETs.**

***Index Terms*—NBTI, PBTI, multi-V_{th}, replacement gate, CMOS, BTI models, aging simulations.**

I. Introduction

SYSTEM on Chip (SoC) application designs require the fabrication of MOSFETs with different threshold voltages (V_{th}) on the same wafer to best fulfill a range of system functions (e.g., high performance vs. low power). In recent Replacement Gate CMOS technologies, multiple device V_{th} flavors (up to six different ones [1]) are realized, typically by depositing different work function metal stacks. It is hence of interest to investigate whether a different metal work function can affect the reliability of a given dielectric stack.

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Most Bias Temperature Instability (BTI) models consider this aging mechanism to be primarily accelerated by the applied oxide electric field [2]. One would therefore expect a similar degradation to be observed in devices with different work function metals (WFM), if the gate stress test voltage is adjusted to maintain a given gate overdrive ($V_{ov} = V_G - V_{th0}$). While this expectation is confirmed in some literature reports [3]–[5], others have reported unexpected BTI trends: e.g., [6] reported that high-V_{th} pMOS and nMOS, with metal work function close to Si mid-gap, can withstand larger operating overdrive voltages.

The recently proposed "hydrogen-release" model for the permanent component of NBTI [7] predicts an inherent impact of the metal work function on the pMOS degradation: interstitial hydrogen can be trapped in dielectric defect sites in different configurations, e.g., protons can bind to bridging oxygens in SiO_2 with a wide distribution of energy levels; a fraction of such defect levels, particularly in the vicinity of the gate, might move below the gate Fermi level—which therefore plays a crucial role—due to the application of an electric field; in this case the proton can be neutralized by a gate electron, and the hydrogen can be released as a neutral specie; the released hydrogen quickly migrates due to diffusion (an extremely fast process; note the mechanism is assumed to be *reaction*-limited, and controlled by the activation energy of the hydrogen neutralization step) and gets trapped at the channel side where it either forms a new defect site or passivates a pre-existing defect, or induces the depassivation of a Si-H bond at the channel/oxide interface through a hydrogen dimerization process, Si-H+H $\rightarrow$ Si°+H_2, where Si° denotes a dangling bond at the interface. Note that dimerization is the only reasonable mechanism to explain how the strong Si-H bond could break during normal pMOS operation, as a direct H-removal would require an excessive energy of ~2.5eV [8]–[10].

While this model foresees a direct impact of the gate work function, at least on NBTI, this mechanism concerns mostly the permanent component of the degradation, which has been suggested to be smaller than the charge trapping component (i.e., the so-called 'recoverable' component) across the entire device lifetime [7]. In this work, we compare the BTI-induced V_{th} shifts (ΔV_{th}) measured after a short stress (i.e., focusing only on the 'recoverable' component of BTI) at fixed oxide electric field in HKMG capacitors with a variety of metal stacks, covering a work function range of ~0.4eV. Contradicting trends are observed depending on the thermal budget applied after the deposition of the gate

metal: e.g., for the as-deposited gate stacks, improved reliability is observed in low-V_{th} devices; in contrast, if a post metal anneal (PMA) is performed, high-V_{th} nMOS gate stacks show the smallest trapped charge density. We ascribe this to *different chemical interaction of the considered metal stacks with the dielectric, which yields different defect profiles depending on the process thermal budget*.

To corroborate this observation, we compare PBTI and NBTI degradation in nMOS and pMOS planar transistors fabricated with a Replacement Gate flow, with three selected WFM stacks representative of high-, standard, and low-V_{th} device flavors, fabricated with two different process thermal budgets. In order to systematically compare BTI degradation in the device with different V_{th} flavors at fixed stress gate voltage, gate overdrive, and oxide electric field, we calibrate a simple semi-empirical BTI model to experimental stress/recovery data recorded in a variety of stress conditions. This analysis confirms that different metal/dielectric chemical interaction results in widely different oxide defect properties, which in turn control the BTI reliability, instead of the gate work function *per se* which in principle should control only the relation between gate voltage and oxide electric field. In particular, the combination of a TiN gate metal and a high process thermal budget is identified as extremely beneficial for both NBTI and PBTI.

Furthermore, to isolate the pure impact of a different gate work function on charge trapping, we perform simulations with the imec/T.U. Wien BTI modeling framework Comphy ("Compact Physical" [11]). We observe that *a different gate work function can induce a different charge state of the deep high-k defects, and therefore affect charge trapping during stress, particularly in nMOSFETs.*

II. Experimental Results on Capacitors

We fabricated *n*- and *p*-type MOS capacitors comprising a ~0.6nm SiO_2 interfacial layer, ~1.8nm HfO_2 high-k dielectric, and various TiN- and TiAl-based WFM stacks. A variety of work functions within a ~0.4eV range were obtained by employing different metal thicknesses and different bottom adhesion layers (TiN, TaN, TiSiN, TiTaN; stack composition and layer thicknesses in nm are noted in the data labels in Figs. 1-2, note "a.b." stands for "air-break"). For each gate stack, two set of capacitors were fabricated: one received only a 400°C-5' hydrogen anneal after metal deposition ('as-deposited'), while the other received also a 450°C-2h Post Metal Anneal (PMA) in nitrogen.

BTI charge trapping measurements were performed for increasing stress voltages at room temperature. To compare the various gate stacks, we evaluated the BTI-induced flatband voltage shift (ΔV_{fb}) after 1s of stress at an equivalent oxide field of 5MV/cm. To account for slight EOT differences across the gate stacks, the ΔV_{fb} values were converted into an equivalent charge sheet $\Delta N_{eff} (= \Delta V_{fb} * C_{ox}/q)$.

Experimental data in Fig. 1 show contradictory trends: in the 'as-deposited' capacitors, a low metal work function (i.e., nMOS low-V_{th}, LVT, and pMOS high-V_{th}, HVT) is associated with a reduced PBTI trapping, and an enhanced NBTI trapping. In contrast, on the capacitors subject to a PMA, a low metal work function (i.e., nMOS LVT) is generally associated with an enhanced PBTI trapping. These results suggest that *the impact of a different WFM on charge trapping might*

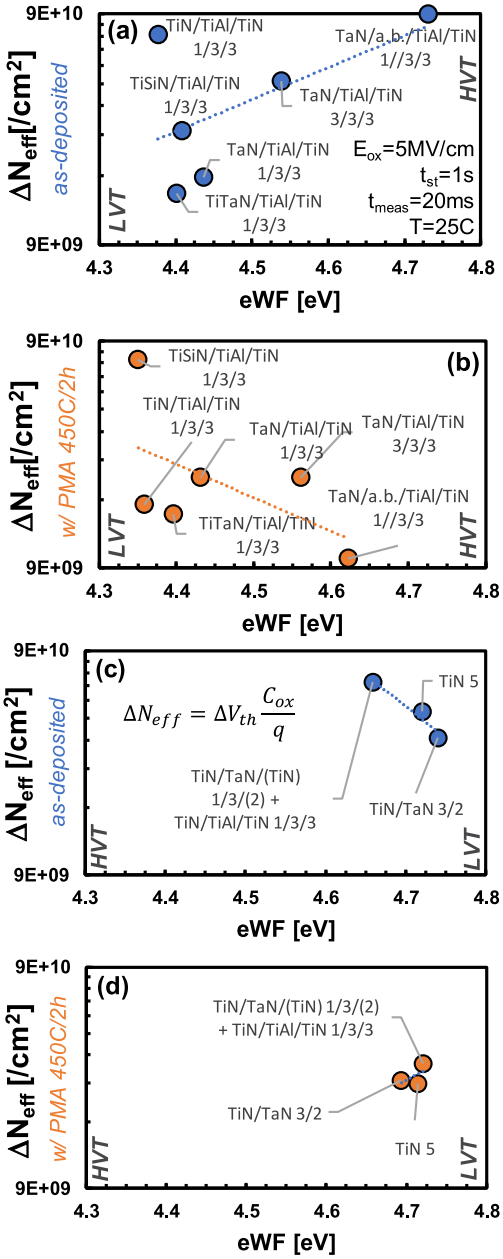

Fig. 1. Charged oxide defect density estimated from BTI trapping measurements (ΔN_{eff} defined as $\Delta V_{fb} * C_{ox}/q$, where ΔV_{fb} is the flatband voltage shift measured after 1s stress at equivalent oxide field $E_{ox} = V_{ov}$/CET=5MV/cm, at room temperature) in **(a,b)** *n*-channel and **(c,d)** *p*-channel $Si/SiO_2/HfO_2$ MOS capacitors with various metal stacks (indicated by the data labels, which also report the thickness of each metal layer in nm), as-deposited **(a,c)**, and after 450°C-2h PMA **(b,d)**. At low thermal budget, the stacks with lower WF (i.e., nMOS low V_{th}, pMOS high V_{th}) show reduced ΔN_{eff} in PBTI stress condition and increased ΔN_{eff} in NBTI stress condition. In contrast, after a 450°C-2h PMA the stacks with lower WF show increased ΔN_{eff} in PBTI stress condition and slightly decreased ΔN_{eff} in NBTI stress condition. These contrasting trends suggest that the oxide reliability is controlled by the chemical interaction of a given metal stack with the underlying dielectrics, as a function of the process thermal budget, instead of the metal work function *per se* (note: the latter is supposed to have a negligible impact when benchmarking at constant oxide electric field).

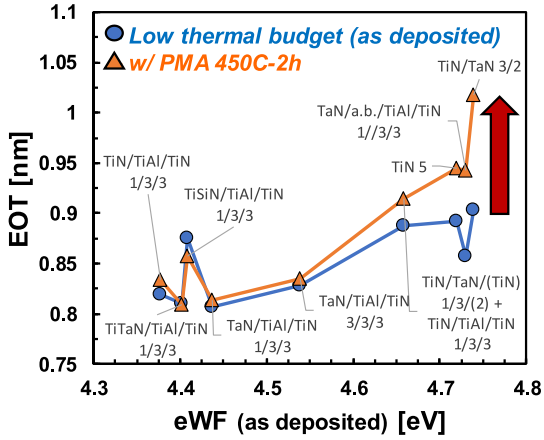

Fig. 2. EOT and effective work function estimated from C-V measurements of $Si/SiO_2/HfO_2$ MOS capacitors with various metal stacks, as deposited and after 450°C-2h PMA. While the low WF (TiAl-based) stacks show similar EOT before and after the PMA, the high WF (TiN-based stacks) show an EOT increase after PMA, possibly due to SiO_2 regrowth induced by oxygen movement within the gate stack favored by metals with higher electron affinities. These different trends suggest that different metals may interact differently with the dielectric stack during the fabrication steps following gate stack deposition, inducing different dielectric defect properties.

be controlled by the chemical interaction of the metal stack with the underlying dielectric stack [e.g., i) oxygen dynamics affected by the different metal electron affinities; ii) diffusion of metal species as Al in the dielectrics which might modify the defect properties], *yielding different oxide defect distributions as a function of the process thermal budget*, instead of by the work function itself. This hypothesis is qualitatively supported also by the different EOT increases measured after PMA in the stacks with different metals (Fig. 2). Note that the high work function metal stacks seem to systematically induce larger EOT increase (possibly by favoring oxygen atoms movement within the gate stack due to their high electron affinity).

III. Experimental Results on Transistors

In order to further investigate the impact on BTI of the chemical interaction of the gate metals with the underlying dielectric stack, we fabricated planar nMOS and pMOS transistors in a Replacement Gate (RMG) flow using three selected metal stacks from the previously discussed capacitor experiments. To represent a sufficient diverse WF range, we selected a 5 nm TiN gate as an example of high WFM (i.e., for nMOS HVT, and pMOS LVT), a TiN/TiAl/TiN (1/3/3 nm) metal stack as an example of low WFM (i.e., for nMOS LVT, and pMOS HVT), and a TaN/TiAl/TiN (2/4/2nm) metal stack, where the 2nm TaN bottom layer is intended to serve as a barrier for the potential diffusion of Al- toward the dielectric [12], which resulted in a ∼ midgap WF (i.e., referred to as nMOS and pMOS standard-V_{th}, SVT, in the following). The obtained 'as deposited' device V_{th}'s are shown in Fig. 3 (a-b). Note that the WF were not carefully tuned to obtain realistic HVT, SVT, or LVT values in all cases (in particular the TaN/TiAl/TiN stack resulted in an SVT nMOS and an HVT pMOS, possibly due different interface state profiles); nevertheless, we will use this simple nomenclature in the following for convenience. Similar

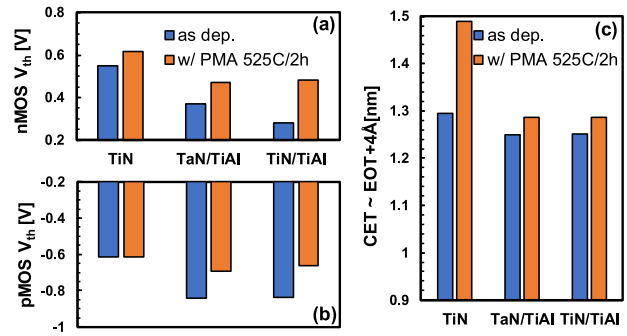

Fig. 3. **(a-b)** Measured nMOS and pMOS transistor V_{th} with three different work function metal stacks, without or with a 2h PMA at 525°C in nitrogen. **(c)** Measured Capacitance Equivalent Thickness (CET) of the different transistor gate stack. Note the larger CET increase after PMA for the TiN-based gate stack (see Fig. 2).

to the capacitor experiments reported in Section II, we fabricated two sets of transistors: the first one did not receive any high temperature step after metal deposition ('as deposited', which received only a sintering anneal at 400°C in hydrogen; note: the lack of the so-called 'reliability anneal' is expected to yield severe BTI shifts [6], [13]), while the second set received a 525°C-2h PMA in nitrogen, intended to investigate the impact on BTI of the enhanced chemical interaction between the metals and the dielectric stack at higher thermal budgets. Note that the long PMA results in a shift of the lower effective work functions (eWF) towards midgap, as observed by the lowered pMOS V_{th} and increased nMOS V_{th} values in Fig. 3 (a-b). The high WF TiN gate instead induces a larger EOT increase during the PMA compared to the other two metal stacks [Fig. 3 (c)], consistent with the capacitor experiments (see Fig. 2). These differences in the eWF and EOT sensitivity to thermal budget can be responsible to some extent of the contradictory trends reported in literature [3]–[6] when comparing BTI degradation for different WFM at fixed gate stress voltage (V_G), instead of compensating for the different V_{th}'s by comparing at fixed gate overdrive (V_{ov}), and for the different EOT by comparing at fixed oxide electric field (E_{ox}, defined here as V_{ov}/CET).

We measured BTI degradation in all the nMOS and pMOS transistors illustrated in Fig. 3 for various stress voltages, for increasing stress times (∼1s to ∼1ks), at 25°C and at 125°C; the stress was interrupted from time to time to sense the induced ΔV_{th}, and the recovery was monitored each time from 1ms to ∼10s before resuming stress (Fig. 4; note only the last recovery trace at end of stress is shown). In order to be able to easily compare the BTI-induced ΔV_{th} at various degradation stages, for either a fixed V_G, V_{ov}, or E_{ox}, across the different gate stacks, we calibrated a simple BTI empirical model to the experimental data, which allow us to rescaled the BTI-induced ΔV_{th} to any given test condition (note: the simple model is used only to interpolate the experimental data, and not to extrapolate beyond the measured range). To capture the dependences on stress temperature (T), stress E_{ox}, stress time (t_{st}) and recovery time (t_{rel}), we used the following expression:

$$\Delta V_{th}(T, E_{ox}, t_{st}, t_{rel}) = A\ e^{\left(\frac{-E_a}{k_B T}\right)} E_{ox}^{\gamma} t_{stress}^{n} \frac{1}{1 + B E_{ox}^{-\gamma_B} \left(\frac{t_{rel}}{t_{st}}\right)^{\beta}}, \quad (1)$$

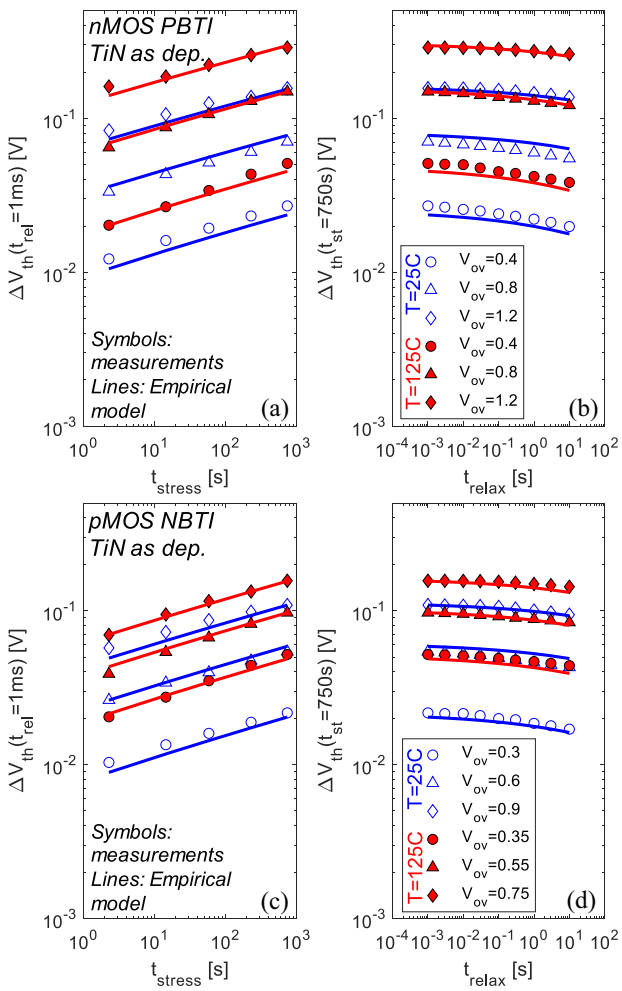

Fig. 4. BTI stress and recovery traces measured in the **(a-b)** nMOS and **(c-d)** pMOS devices with the 'as-deposited' TiN-based gate stack, at three different stress voltages and two different stress temperatures (only the recovery traces after the last stress phase is shown). The experimental data (symbols) are used to calibrate a simple semi-empirical degradation model (lines, see Eq. (1)). A similar calibration was performed for the other five transistor gate stacks discussed in Section III (see Table I).

where A is a pre-factor (referred to an E_{ox} of 1MV/cm), E_a is the apparent BTI activation energy [14], [15], k_B is the Boltzmann constant, γ is the BTI field acceleration exponent, n is the time exponent, B and β are the universal relaxation function scale and shape parameters [16], and γ_B is an exponent meant to capture the slower fractional recovery following harsher stress conditions which results from the (weak) correlation of oxide defect capture and emission activation energies [14]. An example of the model fitted to the experimental data is shown in Fig. 4 for the TiN-gate nMOS and pMOS transistor 'as-deposited', while the calibrated model parameters for each of the studied gate stacks are reported in Table I. Notice how the PMA results in a significant change of virtually all the model parameters (and particularly A, E_a, and γ), further suggesting that the main impact of the gate metal on BTI is related to the different oxide defect properties resulting from the chemical interaction of different metal stacks with the underlying dielectric stack as a function of the process thermal budget, more than by the gate work function *per se*.

TABLE I
PARAMETERS OF THE CONSIDERED SEMI-EMPIRICAL BTI DEGRADATION MODEL (SEE EQ. (1)) AS CALIBRATED ON THE EXPERIMENTAL DATA OF THE SIX DIFFERENT NMOS AND SIX DIFFERENT PMOS TRANSISTOR FLAVORS

		as dep.			w/ PMA 525C/2h		
		TiN	TaN/TiAl	TiN/TiAl	TiN	TaN/TiAl	TiN/TiAl
nMOS	A [mV]	23.4	10.3	3.8	0.2	3.4	0.5
	Ea [meV]	66.5	66.5	75.3	-1.7	78.9	77.5
	γ	1.68	2.06	2.50	2.29	2.45	3.09
	n	0.12	0.11	0.12	0.12	0.13	0.15
	B	1.94	3.02	3.01	1.04	1.02	0.77
	γ_B	0.604	0.898	-0.780	0.189	0.330	0.221
	β	0.194	0.250	0.215	0.141	0.192	0.189
pMOS	A [mV]	33.4	82.0	79.2	2.6	30.0	9.6
	Ea [meV]	64.9	94.3	117.9	35.4	91.8	99.7
	γ	1.51	1.58	1.93	2.01	1.66	2.33
	n	0.13	0.12	0.13	0.10	0.11	0.13
	B	1.04	0.85	1.05	1.48	0.66	0.85
	γ_B	0.389	0.348	0.302	0.136	0.000	0.000
	β	0.187	0.154	0.156	0.146	0.133	0.132

In order to compare the BTI induced ΔV_{th} at various relevant degradation stages, we picked three representative stress conditions: 1s of stress at room temperature (similar to the capacitor data of Section II, but arguably less representative of long term reliability) with a fast sensing (1ms delay) as a representation of the fast trapping oxide defects (Fig. 5); 1ks of stress at 125°C with a fast sensing (1ms delay) as a representation of the slow trapping defects (Fig. 6); and 1ks of stress at 125°C with a slow sensing (10s delay) as a representation of the slow trapping and de-trapping defects (Fig. 7). For each degradation stage, we compare the ΔV_{th} induced by a stress at fixed V_g (1.3V), a fixed V_{ov} (0.7V) or a fixed E_{ox}(= V_{ov}/CET=5MV/cm).

The following observations can be made by comparing Figs. 5-7. For the 'as-deposited' gate stacks, when comparing ΔV_{th} at fixed stress V_g, the HVT flavors result in (apparently) best PBTI and NBTI reliability at all the three considered degradation stages. This is due to the lower E_{ox} in the HVT stacks for a given stress V_g. After the long PMA, the HVT nMOS (TiN gate) continue to show the best PBTI reliability at fixed V_g; similarly, the same gate metal (i.e., pMOS LVT) shows also the best pMOS NBTI reliability at fixed V_g (Fig. 6-7), despite bearing the largest V_{ov} due to the lowest pMOS V_{th}. This surprising observation seems related to an extremely beneficial impact on the oxide defect density of the TiN metal at high thermal budget, as suggested by the dramatic reduction of the pre-factor A upon application of the PMA (see Table I: for NBTI, 33.4mV 'as-deposited' and 2.6mV after PMA; for PBTI, 23.4mV 'as-deposited' and 0.2mV after PMA).

To take into account the impact of different V_{th}'s on the oxide field resulting from the application of a given gate voltage, we argue that the intrinsic BTI degradation of different device flavors should be compared at fixed gate overdrive, or

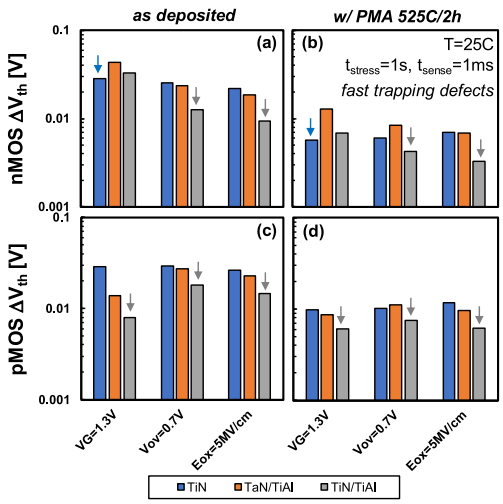

Fig. 5. PBTI- and NBTI- induced ΔV_{th} in the **(a-b)** nMOS and **(c-d)** pMOS transistors with three different work function metal stacks, **(a,c)** as-deposited, or **(b,d)** after 2h long PMA at 525°C in nitrogen. The BTI shifts are compared at fixed stress $|V_g|$ (1.3V), fixed stress $|V_{ov}|$ (0.7V), or fixed stress E_{ox} (= V_{ov}/CET=5MV/cm). The arrows highlight the gate stack showing the smallest BTI-induced ΔV_{th} in each case. To reflect the BTI contribution of fast trapping oxide defects, the following test conditions are considered in this case (see Fig. 6-7): room temperature, 1s stress time, 1ms recovery time (i.e., sense delay).

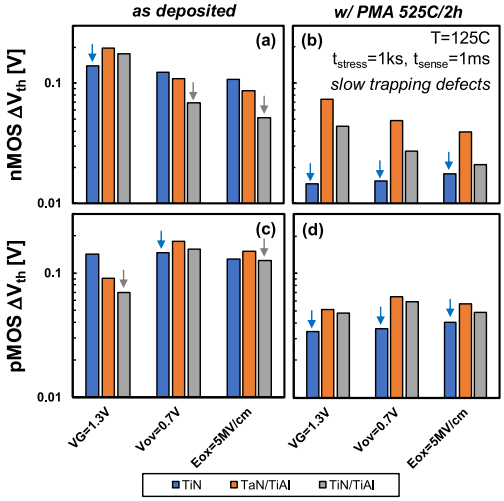

Fig. 6. Same as Fig. 5, now for test conditions reflecting the contribution of slow trapping oxide defects: 1ks stress time at 125°C, 1ms recovery time.

even at fixed V_{ov}/CET to account also for the possible differences in EOT resulting from the different metal/dielectric chemical interactions [see Fig. 2 and 3 (c)]. When comparing the different gate stacks at fixed stress E_{ox}, different observations can be made. On the 'as-deposited' gate stacks, the nMOS LVT (TiN/TiAl/TiN metal) show the best PBTI reliability. Similarly, this metal stack results in best 'as-deposited' NBTI reliability, suggesting a beneficial combination of this metal stack with the underlying dielectric stack at low thermal budget. Note however that at low thermal budget the NBTI-induced ΔV_{th} is only marginally larger in HVT pMOS (Figs. 6-7). When considering instead the gate stacks after PMA, the TiN gate (i.e., pMOS LVT and nMOS HVT) induces the best NBTI and PBTI reliability (Figs. 6-7), ascribed above

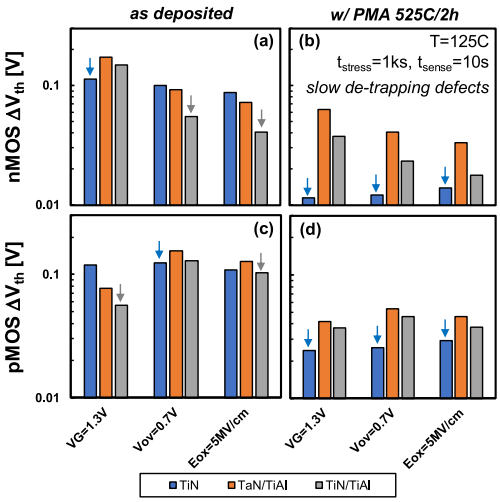

Fig. 7. Same as Fig. 5-6, now for stress conditions reflecting the BTI contribution of slow de-trapping oxide defects: 1ks stress time at 125°C, 10s recovery time.

to a reduced oxide defect density resulting from the beneficial interaction of TiN with the dielectric stack at high thermal budget. Interestingly, the midgap WFM stack, which comprises a 2 nm thick TaN diffusion barrier bottom layer under the TiAl instead of the 1 nm TiN bottom layer used for the low eWF stack, never yields the best PBTI nor NBTI reliability, which is probably due to the suppressed chemical interaction between TiN or TiAl with the dielectric stack, which apparently can be beneficial for the oxide defect properties, provided a good combination of metal stack and post-metal thermal budget is selected.

We conclude that the oxide defect properties of a gate stack reflect the chemical interaction of the metal stacks with the underlying dielectric stack upon application of a given process thermal budget. While the thermal budget considered here ('as-deposited' vs. PMA 525°C-2h) were chosen explicitly as extreme cases, and they are not representative of a realistic RMG technology, the observation here reported are exemplary of the chemical interaction which could take place during the post-metal so-called 'reliability anneal', customary in any commercial technology (typically in the range of 850-900°C for a few seconds), and during the thermal steps required for the Back-End-Of-Line (BEOL) fabrication. In a future study we plan to use Comphy to calibrate defect parameters to the BTI traces measured on the gate stacks with different metal stacks: this will allow to further describe the impact of different metals on the underlying SiO_2/HfO_2 dielectric stack in terms of defect densities and energy levels distribution (we discussed already the impact of the 'reliability anneal' on the oxide defect properties of a TiN-based gate stack in [17]). In the following Section we discuss Comphy simulations aimed at assessing the pure impact of a different work function on the oxide defects occupancy, neglecting any modification of the defect properties related to the metal/oxide interaction.

IV. Comphy Simulations (Ideal Case)

To investigate the issue from a theoretical standpoint, we performed BTI simulations with Comphy. We considered the

Table II

		Foundry 28 nm
Shallow SiO_2	N_t [/cm³]	1.5 x10¹⁹
	$\langle E_t \rangle \pm \sigma_B$ [eV]	1.13 ± 0.15
	$\langle S \rangle \pm \sigma_S$ [eV]	3.82 ± 1.36
	R [1]	0.407
Shallow HfO_2	N_t [/cm³]	5.52 x10²⁰
	$\langle E_t \rangle \pm \sigma_B$ [eV]	1.2 ± 0.156
	$\langle S \rangle \pm \sigma_S$ [eV]	3.19 ± 0.77
	R [1]	0.587
Deep SiO_2	N_t [/cm³]	1.42 x10²⁰
	$\langle E_t \rangle \pm \sigma_B$ [eV]	-1.26 ± 0.25
	$\langle S \rangle \pm \sigma_S$ [eV]	5.63 ± 2.67
	R [1]	1.8
Deep HfO_2	N_t [/cm³]	2.95 x10²⁰
	$\langle E_t \rangle \pm \sigma_B$ [eV]	-0.17 ± 0.14
	$\langle S \rangle \pm \sigma_S$ [eV]	6.5 ± 1.99
	R [1]	0.514

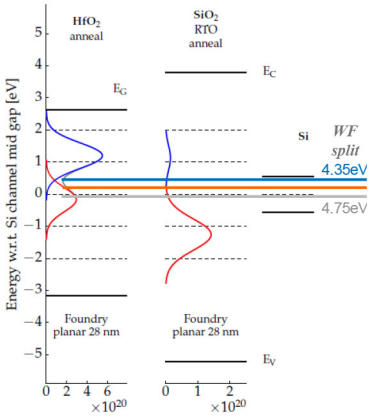

Fig. 8. Sketch of the SiO_2 and HfO_2 shallow and deep defect bands as calibrated in [11] to model the PBTI and NBTI kinetics of a commercial 28 nm HKMG technology. The defect parameters are reported in the inset Table II. This defect model is used here to explore the intrinsic impact of a different metal work function on BTI kinetics by using the imec/T.U. Wien BTI simulation framework Comphy.

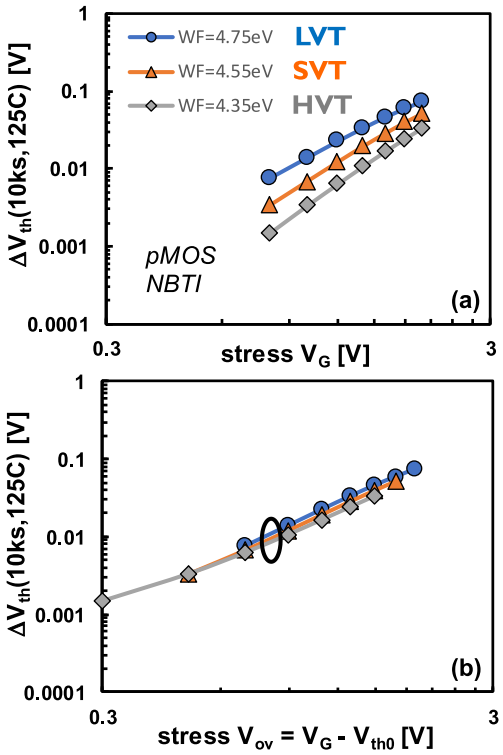

Fig. 9. NBTI-induced ΔV_{th} after 10ks stress at 125°C simulated in Comphy using the defect model calibrated on a commercial 28nm technology (see Fig. 8), for three different metal work functions [4.75, 4.55, 4.35eV, corresponding to pMOS Low V_{th} (LVT), standard V_{th} (SVT), and high V_{th} (HVT) flavors, respectively], **(a)** for increasing stress V_G, or **(b)** replotted vs. the overdrive stress voltage ($V_{ov} = V_G - V_{th0}$) instead.

oxide defect band model calibrated in [11] on a commercial 28nm HKMG technology (Fig. 8), and calculated the expected V_{th} shifts (t_{stress} = 10ks, T=125°C) for increasing stress V_G, for three different gate work function values commonly adopted in real technologies (4.75, 4.55, 4.35eV). For pMOS NBTI, while a larger ΔV_{th} is obviously observed at a given stress V_g for low V_{th} devices, the same ΔV_{th} is obtained

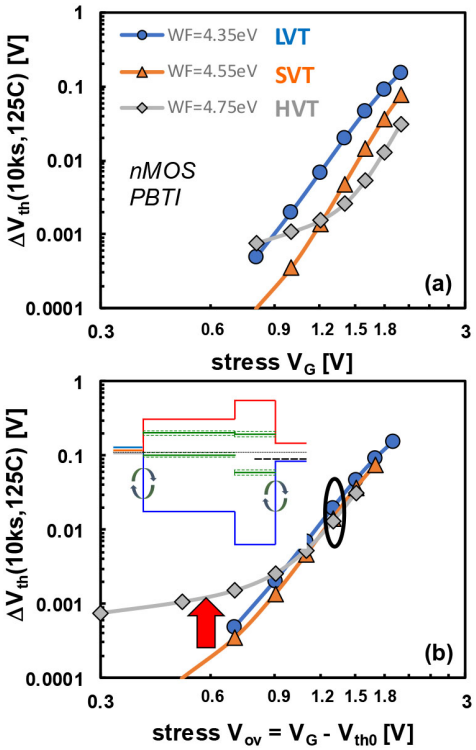

Fig. 10. PBTI-induced ΔV_{th} after 10ks stress at 125°C simulated in Comphy using the defect model calibrated on a commercial 28nm HKMG technology (see Fig. 8), for three different metal work functions [4.35, 4.55, 4.75eV, corresponding to nMOS Low V_{th} (LVT), standard V_{th} (SVT), and high V_{th} (HVT) flavors, respectively], **(a)** for increasing stress V_G, or **(b)** replotted vs. the overdrive stress voltage ($V_{ov} = V_G - V_{th0}$) instead.

when comparing at same stress V_{ov} (i.e., compensating for the different initial V_{th}, Fig. 9), as expected from an electric field-driven charge trapping mechanism. In contrast, for nMOS PBTI a constant ΔV_{th} at same V_{ov} is obtained only for high stress voltages (Fig. 10): at low V_{ov} of relevance for logic operation [~0.6V, Fig. 10 (b)], a larger ΔV_{th} is calculated when assuming a high WFM (nMOS HVT).

We ascribe this unexpected behavior to the deep defect band in HfO_2, which is located only ~0.17eV below Si midgap (see Fig. 8; i.e., aligned to the Fermi level of a metal with work function 4.52eV). For a low or midgap WFM, this deep defect band is filled with electrons already at V_{fb}. However, when using a high WFM, some of these deep states can release their electron to the gate at equilibrium condition, and therefore become available to trap a channel electron during PBTI stress, contributing additional ΔV_{th}. In agreement with this interpretation, the same ΔV_{th} at same V_{ov} can be almost perfectly re-established in the simulations [Fig. 11 (a)] by removing the deep oxide defect bands from the model (see Table II in Fig. 8), suggesting that the gate work function has almost a negligible impact on the occupancy of the shallow defect bands. If instead the gate interaction with the oxide defects is deactivated altogether in the simulations, the same ΔV_{th} at same V_{ov} is perfectly re-established, irrespective of the presence of the deep oxide defect bands [Fig. 11 (b-c)], confirming that the root cause of the different ΔV_{th} at same (low) V_{ov} shown in Fig. 10 (b) originates mainly from the impact of the gate Fermi level on the deep defect band occupancy.

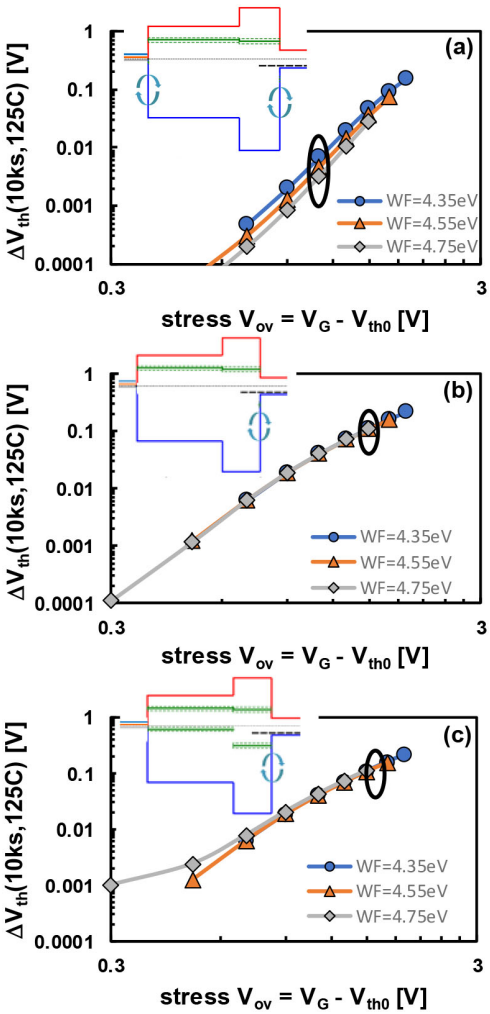

Fig. 11. PBTI-induced ΔV_{th} after 10ks stress at 125°C simulated in Comphy using the defect model calibrated on a commercial 28nm technology (see Fig. 3), for three different metal work functions [4.35, 4.55, 4.75eV, corresponding to nMOS Low V_{th} (LVT), standard V_{th} (SVT), and high V_{th} (HVT) flavors, respectively], plotted vs. the overdrive stress voltage ($V_{ov} = V_G - V_{th0}$). The various interactions between oxide defects bands and charge reservoirs are selectively considered: **(a)** only shallow defect bands in SiO_2/HfO_2 interacting with both the channel and gate reservoirs; **(b)** only shallow defect bands interacting only with the channel; **(c)** shallow and deep defect bands interacting only with the channel.

V. Conclusion

We investigated BTI charge trapping trends in high-k metal gate (HKMG) stacks with a variety of work function metals. Most BTI models suggest charge trapping in oxide defects is modulated by the applied oxide electric field, which controls the energy barrier for the capture process, irrespective of the metal work function. However, experimental data on capacitors and planar transistors showed enhanced or reduced charge trapping at constant oxide electric field for different work function metal stacks, at different process thermal budgets. We ascribed this to a different chemical interaction of the metal stack with the dielectric, yielding different defect profiles depending on the process thermal budget. In particular, the combination of a TiN gate metal (i.e., pMOS LVT and nMOS HVT) and a high post-metal process thermal budget is identified as extremely beneficial for both NBTI and PBTI reliability. Furthermore, by employing the imec/T.U. Wien physics-based BTI simulation framework "Comphy", we have also shown that a different gate work function can yield a different occupancy of the deep high-k defects, and can therefore have an impact on the charge trapping kinetics during BTI stress, particularly in nMOSFETs at low operating voltage of relevance for logic applications.

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