Border Trap Based Modeling of SiC Transistor Transfer Characteristics

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***Abstract*—We experimentally and theoretically study the impact of interface and border traps on the transfer characteristics of 4H-SiC transistors measured over a wide temperature range of 200-350 K. Quite apparently, the experimental current-voltage characteristics have drain currents which are much lower than those obtained from simulations performed without traps. Moreover, currents increase with temperature over the entire gate voltage range, while the threshold voltage shifts towards lower values as temperature increases. We show that although interface traps can explain $I_d - V_{gs}$ curves measured at room temperature with good accuracy it fails for lower temperatures. Inclusion of border traps, on the other hand, results in good agreement between experimental and simulated current-voltage characteristics over the entire temperature range. For the first time we were able to successfully represent transfer characteristics of a 4H-SiC transistor at temperatures substantially below 300 K. Therefore, we conclude that border traps are responsible for the complicated behavior of $I_d - V_{gs}$ characteristics.**

I. Introduction

Silicon carbide (SiC) is recognized as a promising material for high-voltage, high-temperature, and high-frequency applications. SiC possesses a number of unique properties including a wide band gap, higher (compared to silicon) breakdown electric field, good thermal conductivity, and a high saturation velocity, as well as a decent bulk mobility [1–3]. SiC has more than 200 polytypes but the polytype of choice for electronic applications is 4H-SiC due to its higher carrier mobility and shallower dopant ionization energies (as compared to other polytypes), as well as weak electron mobility anisotropy in the directions parallel and perpendicular to the crystallographic c-axis [4–6].

Although SiC was suggested as a perfect candidate for power electronics more than 25 years ago [7], SiC based MOSFETs are only starting to become commercialized currently. One remaining issue with SiC MOSFETs is its limited surface/channel mobility which is substantially lower than that of the bulk material [8, 9]. This mobility reduction is attributed to a high concentration of traps at the SiC/SiO_2 interface. Among other aspects, these traps result in a severe distortion of transfer ($I_d - V_{gs}$, where I_d is the drain current and V_{gs} - is the gate voltage) and output ($I_d - V_{ds}$ with V_{ds} being the drain bias) characteristics [10, 11].

Several attempts to model experimental transfer and output characteristics of SiC transistors have been undertaken by various groups [12–17]. All these models assume that the perturbation of current-voltage characteristics is driven by interface traps. Although those papers can represent experimental curves with reasonable accuracy, these model verifications have been performed for room and elevated temperatures only (basically, in the range of 300-500 K). Therefore, to the best of our knowledge, modeling of $I_d - V_{gs}$ curves for lower temperatures has not been addressed so far. We will show that the peculiar features are revealed particularly at lower temperatures which can be consistently explained through the impact of border traps.

The authors of the aforementioned methodologies often propose that different types of traps and/or physical mechanisms are responsible for the abnormal behavior of the current-voltage characteristics and for another detrimental phenomenon, the bias temperature instability (BTI). For instance, the U.S. Army Research Lab group, which was involved in interface trap based modeling of current-voltage characteristics [12, 13], has suggested that BTI includes two processes: activation of oxide traps and oxide trap charging via direct tunneling [18–21]. However, our experience with modeling reliability issues in Si MOSFETs [22, 23] suggests that perturbation observed in current-voltage characteristics and BTI should have a common microscopic origin and that these two parasitic phenomena stem from border oxide traps.

Based on this reasoning, we expect that *border rather than interface traps* are the *origin of the strong distortion of transfer characteristics* of SiC transistors as compared to idealized, defect free, devices. In order to increase the requirements of the model and provide additional information on the trapping dynamics, we attempt to model the transfer characteristics of a SiC transistor over a temperature range of 200-350 K (i.e. focus on lower temperatures) and determine whether the intricate behavior of $I_d - V_{gs}$ curves is related to interface or border traps.

II. Devices and Experiment

Lateral 4H-SiC MOSFET test structures with a gate length of 5.3 μm were fabricated on the Si-face of n-doped substrates using an industrial process. A silicon dioxide layer was grown by chemical vapor deposition followed by post oxidation annealing in an NO ambient. A set of $I_d - V_{gs}$ curves (depicted

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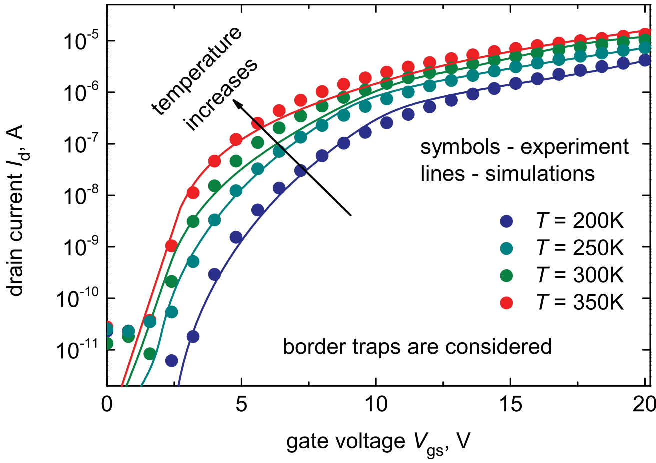

Fig. 1. Transfer ($I_\mathrm{d}-V_\mathrm{gs}$) characteristics of the SiC transistors: experimental data vs. simulation results obtained with the nonradiative multiphonon model applied to describe charging of border traps.

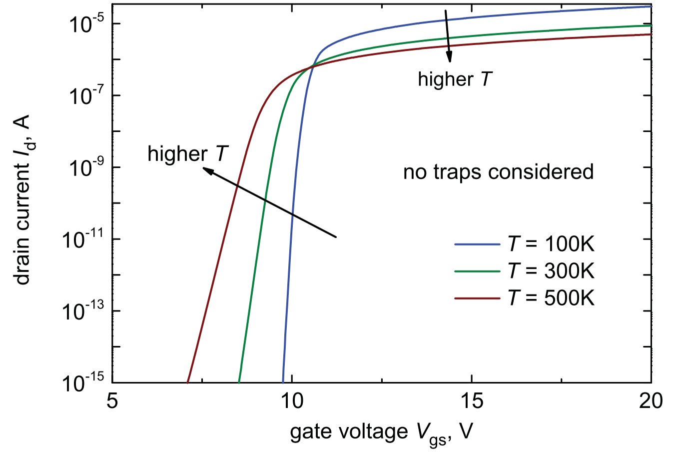

Fig. 2. $I_\mathrm{d}-V_\mathrm{gs}$ characteristics of the SiC transistor simulated disregarding any type of traps. Data are shown for three different temperatures: T = 100, 300, and 600 K.

in Fig. 1) was measured over a wide temperature range $T =$ 200-350 K at a fixed drain voltage of $V_\mathrm{ds} = 0.1\,\mathrm{V}$ and V_gs varying within the range of 0-20 V with a step of 0.8 V. The sweeping rate was (250 ± 20) ms per step.

From Fig. 1 one can see that the drain current substantially grows in the entire gate voltage range as temperature increases. Moreover, the $I_\mathrm{d}-V_\mathrm{gs}$ curves shift by $\sim 2.5\,\mathrm{V}$ and substantially change the shape and the slope as one switches from $T = 350\,\mathrm{K}$ to $T = 200\,\mathrm{K}$. In other words, the device becomes more positively charged and this means that either electron traps become less populated or hole traps capture more charge carriers.

III. Simulation Setup and Results

To model $I_\mathrm{d}-V_\mathrm{gs}$ characteristics of the SiC transistor we employed the device and circuit simulator MINIMOS-NT [24] in the GTS framework [25]. All simulations have been performed using the drift-diffusion scheme. MINIMOS-NT incorporates a number of models crucial for adequate simulations of transistors based on wide band gap materials which include band gap narrowing, incomplete ionization of impurities, and mobility models [26].

A. Transfer characteristics of the idealized device

An example of transfer characteristics simulated without the effect of any traps is presented in Fig. 2. In order to see typical trends in greater detail, the $I_\mathrm{d}-V_\mathrm{gs}$ curves were calculated over a wider temperature range, namely for T = 100, 300, and 600 K. One can see that in contrast to experimental $I_\mathrm{d}-V_\mathrm{gs}$ characteristics (see Fig. 1) the drain current at higher gate voltages appears to be lower if evaluated at higher temperatures. This is due to the strong temperature dependence of scattering mechanism rates which lower I_d. As for the drain current values at low V_gs, they appear to be higher at elevated temperatures due to thermogeneration. This tendency is qualitatively rather different to what is observed in

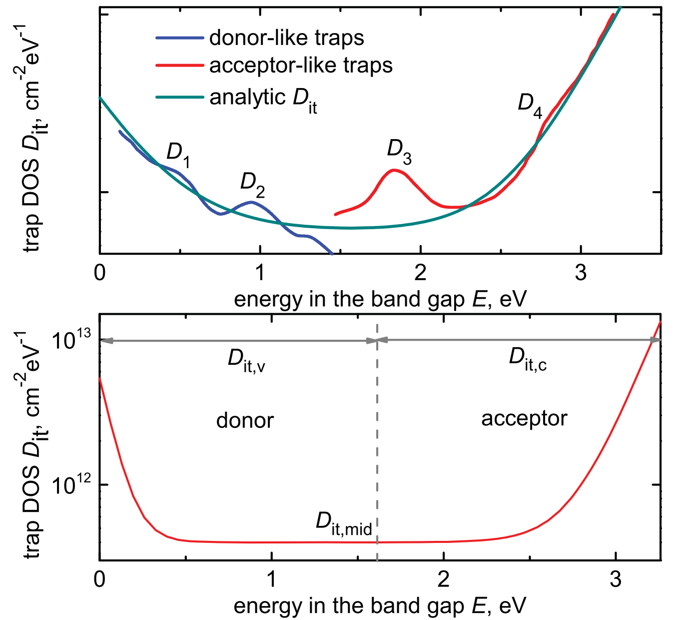

Fig. 3. A schematic representation of the density-of-states employed in interface trap based modeling of current-voltage characteristics in SiC devices. Upper panel: mimicking the experimental D_it by an analytical expression. Lower panel: a sketch of the D_it given by an analytic expression.

experiments, where one can see that the transfer characteristics obtained neglecting the effect of traps produce a rather steep increase in current at low and moderate voltages followed by a very sloping current dependence at higher V_gs.

B. Impact of interface traps

To check the effect of interface traps on transfer characteristics we consider the methodology developed and used by other groups [12–17]. The main idea behind all these models is related to using an analytic expression to mimic experimental behavior of the trap density of states (D_it) reported in the classical paper by Afanas'ev *et al.* [8], see Fig. 3, upper panel.

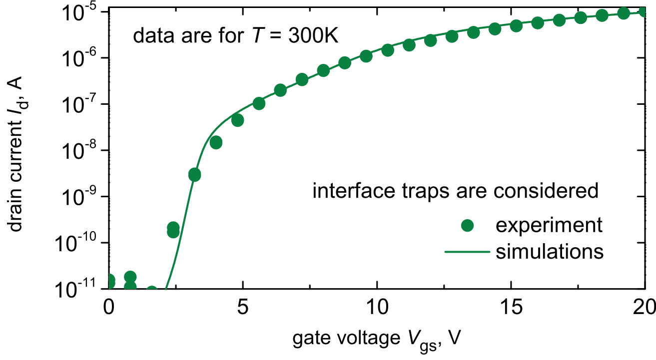

Fig. 4. The experimental $I_d - V_{gs}$ curve measured at room temperature and the simulation which includes the effect of interface traps on transfer characteristics.

The experimental $D_{it}(E)$ dependence (where E is the trap position in the SiC band gap) can be represented near the edges of valence and conduction bands by exponential tails with corresponding broadenings, while in the middle of the SiC band gap D_{it} is set constant (see Fig. 3, lower panel):

$$D_{it}(E) = D_{it,c} \exp\left(\frac{E_c - E}{\sigma_c}\right) + D_{it,mid} + \\ + D_{it,v} \exp\left(\frac{E - E_v}{\sigma_v}\right), \quad (1)$$

where $D_{it,c}$ and $D_{it,v}$ are the DOS values at the conduction and valence band edges (E_c and E_v, respectively), $D_{it,mid}$ determines the DOS values in the middle of the band gap, while the parameters σ_c, σ_v control the steepness of the $D_{it}(E)$ tails. Traps lying in the upper half of the band gap are assumed to be acceptor states while those situated in the lower half of the gap are donor states. Note that some versions of this model (see [14]) consider only the contribution to the DOS given by acceptor traps which is modeled by the first term in (1), while the excluded donor states are compensated by introducing positive fixed charges [14]. The charging/discharging behavior of interface traps is described using Shockley-Read-Hall theory [27].

With the DOS of interface traps modeled in the fashion of (1) we were able to represent the experimental $I_d - V_{gs}$ curve obtained at $T = 300$ K with good accuracy, see Fig. 4. The peak DOS values used in our simulations were $D_{it,c} \sim 1.3 \times 10^{13}$ cm^{-3}eV^{-1}, $D_{it,v} \sim 6.7 \times 10^{12}$ cm^{-3}eV^{-1}, $D_{it,mid} \sim 4.0 \times 10^{11}$ cm^{-3}eV^{-1}, while σ_c and σ_v were chosen to be 0.08 eV and 0.15 eV, respectively. Note that these parameter values are close to those reported in [14].

However, simulations of $I_d - V_{gs}$ curves performed over the same temperature range as experimental data plotted in Fig. 1 show that for higher values of the gate current this model results in the opposite temperature trend for the drain current than the experimental one, see Fig. 5. In addition, one can see that the curvature of $I_d - V_{gs}$ characteristics simulated for lower temperatures at lower V_{gs} is different.

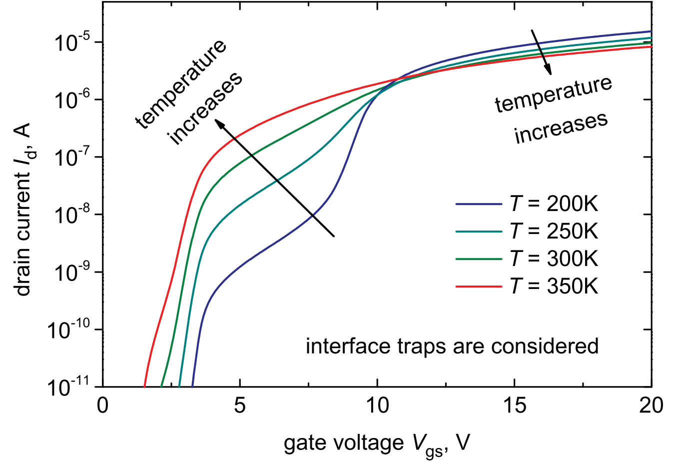

Fig. 5. A family of $I_d - V_{gs}$ curves simulated with interface traps at four different temperatures: T =200, 250, 300, and 350 K.

C. Impact of border traps

To model the effect of border traps we employ the nonradiative multiphonon model which was successfully applied to describe BTI and random telegraph noise in Si devices [22] as well as current-voltage characteristics of transistors based on 2D materials [28]. For the sake of simplicity we used a 2-state version of this model (details are given in [23]). Simulations have been carried out in a non-self-consistent manner, i.e. the charge captured by traps was taken into account as a perturbation of the gate voltage.

Deep donor traps with a concentration of $N_{bt,d} \sim 1.2 \times 10^{20}$ cm^{-3} were placed at ∼3.0 eV above the valence band edge (i.e. ∼0.3 eV below the conduction band edge; the band gap of 4H-SiC is 3.265 eV), see Fig. 6. These traps are distributed over energy according to a Gaussian function with a standard deviation of $\sigma_d = 0.19$ eV. These parameters have been obtained by verification of the model against experimental $I_d - V_{gs}$ characteristics depicted in Fig. 1. At higher temperatures these donor traps become more populated (at the same gate voltage), thereby bending the current-voltage curves and resulting in less steep subthreshold slopes, as can be seen from Fig. 1.

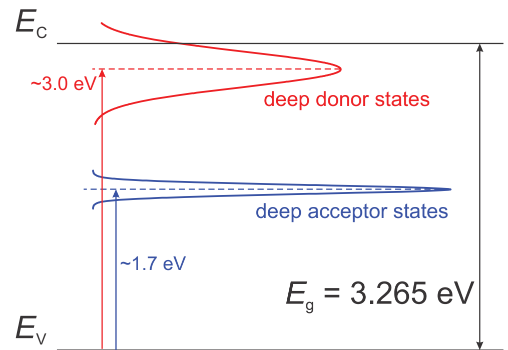

Fig. 6. A sketch of distributions of deep donor (red line) and deep acceptor (blue line) border traps.

However, such a high concentration of donor traps resulted in an excessive shift of current-voltage curves towards lower V_{gs} values. To compensate this shift we also introduced deep acceptor traps with an energy level position of $\sim 1.7\,\mathrm{eV}$ above the valence band edge with a concentration of $N_{\mathrm{bt,a}} \sim 4.4 \times 10^{19}\,\mathrm{cm}^{-3}$ (Fig. 6). The distribution of these traps is narrower than that for donor traps and has a standard deviation of $\sigma_{\mathrm{a}} = 0.04\,\mathrm{eV}$.

It is important to emphasize that extensive efforts have been applied to investigate the microscopic properties of traps typical for the 4H-SiC/SiO_2 system using density functional theory (DFT) [29, 30]. Although a consensus on microscopic properties of states located in the lower half of the band gap (marked as D_1 and D_2 in the upper panel of Fig. 3) has been reached, the main discussion was devoted to the properties of defects in the upper half of the band gap (D_3 and D_4). In Refs. [29, 30] different defect candidates have been examined and conclusions on the most probable defect configuration have been drawn. It was shown that the best candidates can indeed have energy transition levels located close to the SiC conduction band edge but these levels correspond to 0/-1 charge states, i.e. these traps are acceptor states. However, in our recent publications [31, 32] we presented DFT results which suggest that in devices fabricated using the same technological process as our transistor most possible defect candidates are (*i*) a nitrogen atom which substitutes a carbon atom adjacent to a silicon vacancy ($N_C V_{Si}$) and (*ii*) a nitrogen atom which substitutes a silicon atom in the vicinity of a carbon vacancy ($N_{Si} V_C$). The energy formation diagram calculated for the latter defect shows that this defect has a charge transition +1/0 level situated $\sim 0.6\,\mathrm{eV}$ below the conduction band edge and this position roughly corresponds to the position of the deep donor trap employed in our calculations.

Finally, using these two trap distributions we were able to represented experimental $I_{\mathrm{d}} - V_{\mathrm{gs}}$ characteristics over the entire temperature range with good agreement, see Fig. 1. It is important to emphasize that for the first time we can *capture transfer characteristics* of SiC transistors for temperatures substantially below room temperature by considering *border traps*.

IV. Conclusion

Measurements of transfer characteristics of 4H-SiC transistors over a wide temperature range of 200-350 K demonstrate that the drain current increases in the whole gate voltage interval as temperature grows and the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves shift towards lower gate voltages, i.e. the threshold voltage decreases with temperature. This means that at elevated temperatures either the negative charge captured by traps decreases or the positive charge increases. To capture these trends we employed two modeling approaches, i.e. the standard Shockley-Read-Hall model which describes the current-voltage characteristics considering the interface traps and an extended model which takes only the border traps into account.

Although interface traps alone can represent the experimental $I_{\mathrm{d}} - V_{\mathrm{gs}}$ measured at $T = 300\,\mathrm{K}$ with good accuracy, this model is not capable of capturing the transfer characteristics over the entire temperature range. For instance, the model predicts that the drain current at higher V_{gs} should decrease with temperature while experimental curves show the opposite trend. Moreover, the simulated characteristics feature a substantially different curvature as compared to the simulated results.

In order to better describe the experimental data, we introduced border traps into simulations, namely deep donor and acceptor traps with energies of $\sim 3.0\,\mathrm{eV}$ and $\sim 1.7\,\mathrm{eV}$ above the valence band edge, respectively. The distribution of donor traps determines the slope of the $I_{\mathrm{d}} - V_{\mathrm{gs}}$ curves, while the acceptor traps compensate the very large threshold voltage shift due to the positive charge stored on donor traps. This description allowed us to represent experimental $I_{\mathrm{d}} - V_{\mathrm{gs}}$ data with good accuracy over the entire temperature range. We finally note that modeling of transfer characteristics of SiC transistors for temperatures significantly below room temperature has been carried out for the first time. One of the most important results is that we showed that border (not interface) traps are responsible for the behavior of transistor transfer characteristics.

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